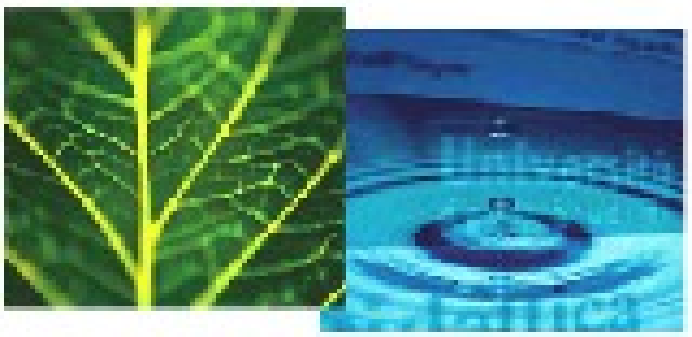
PhD Dissertation



International Doctorate School in Information and Communication Technologies

DIT - University of Trento

Multilayer Micromachined RF MEMS Filters at Ka and L/S Band For On-Board Satellite Communication Systems

Abdul Qader Ahsan Qureshi

Advisor:

Dr. Benno Margesin

Head of MEMS Group

Fondazione Bruno Kessler (FBK)

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Dedicated to

To the memories of my grandmother (1920 – 16th Nov, 2012) who was always in my thoughts on this journey. I hope she would have been proud.

To my family.

Acknowledgements

"A journey of a thousand miles begins with a single step"

Lao Tzu (604-531BC)

A long term goal cannot be achieved without taking steps or measures to achieve it and this thesis is the first step in my journey.

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Abdul Qader Ahsan Qureshi
Trento, Italy
April 2013

"Good process design is a creative art, supported by careful engineering analysis and experiment"

(*StephenD.Senturia*)

Abstract

This doctorate thesis focuses on the application of micromachining fabrication technologies for the realization of Radio Frequency (RF) bandpass filters. The work has been inspired and supported by the European Space Agency (ESA) Contract No. 22706/09/NL/GLC of the ARTES 5 Workplan 2008 "Micromachined Filters in Multilayer Technology for Satellite Onboard Communication Systems" (MIGNON Project). The main purpose of the project is the design and realization of high performance bandpass filters in the Ka and L/S band for on board applications. The use of modern micromachining technologies should allow for space and weight reduction as well as for a cost effective realization of these devices. In addition the tight tolerances obtained with micromachining techniques facilitate an industrial fabrication of filters with high yield. The thesis proposes novel concepts to accomplish this task and provides also the fabrication processes suitable to realize the devices. In addition this work gives also a deeper insight into critical fabrication steps like wafer to wafer thermocompression bonding using gold (Au) and silver (Ag) as an intermediate layer and fabrication of Through Silicon Vias (TSV).

Keywords:
[RF MEMS, Bandpass Filters, Microwave, Micromachining, Thermocompression bonding, Through silicon via].

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Chapter 1

Introduction

The last two and a half decades have seen a stunningly rapid growth of the so-called Micro-Electro-Mechanical-System (MEMS) and the related micromachining technologies. These devices, which typically involve some sort of mechanical movement or are truly tree dimensional structures, are a branch of the great family of microelectronic devices, which has seen a tremendous growth both in performance and numbers mainly due to their applications in the Information and Communication Technology (ICT). Microelectronic circuits have been characterized by an amazing reduction in feature size from micron level at the end of the eighties to less than 50 nm today, following exactly Moore's law. At the same time the integration capability, both on a single chip or as a system in package has grown by different orders of magnitude leading the way to the powerful microprocessors and memory devices we are using now. With essentially the same technologies integrated with a few techniques specific to the micromachining it was possible to extend this evolution beyond the electronic circuits to the MEMS and create sensors and actuators that exploit miniaturized movable structures to sense electrostatic, magnetic, fluidic and Electromagnetic (EM) signals. Compactness, cost effectiveness, reliability and ease of integration were the key factors for successful market products like inkjet print heads, accelerometers and digital

micro mirrors that nowadays are ubiquitous in the many consumer products we use everyday.

In the market forecasts for the near future one most promising new application area for MEMS technology is related to the broad field of microwave and RF communications circuits and devices. MEMS technology applied in these fields is referred generally as RF MEMS. As in the case of IC's first and MEMS later also for the RF MEMS the consumer market will be the biggest playground but in addition the field has a large number of specialized applications ranging from industrial applications to telecommunication either ground based and airborne or satellite based which represent rich high added value niche markets.

1.1 Micromachining Technologies

In recent years several different technologies have been developed for the fabrication of the MEMS devices, which integrate and complement the traditional planar technology. One of the earliest technologies developed is the **Bulk micromachining** of silicon and in some minor extend of quartz. This technique rely on the anisotropic etching characteristics of the different crystallographic planes of the silicon crystal. Typically the etchant is a strong basic solution based e.g. on Potassium hydroxide (KOH), Tetramethylammonium hydroxide (TMAH) or organic salts like Ethildiamine. The technique allows to realize three-dimensional (3D) structures with high aspect ratio based on pyramidal cavities.

More or less at the same time **Surface micromachining** has been developed. In this technique the 3D structure is obtained by the combined use of structural and sacrificial layers. At the beginning mostly polysilicon was used as a structural layer and silicon oxide as a sacrificial layer. In time also thick poly silicon (epi-silicon) or SOI (silicon on insulator) have been used

as well as various metals deposited by electroplating. The success of this technique rely on the ability to etch the sacrificial layer without damaging the structural layers and therefore depends on the selectivity of the etching on the materials employed.

In the nineties the ability to define structures in very thick Photoresist (PR) layer using X-ray lithography, developed initially for submicron lithography, led to the development of the so called **LIGA** (**Lithographie**, **Galvanoformung**, **Abformung** = **Lithography**, **Electroplating**, **and Molding)** technique. The technique allows to build high aspect ratio structures directly in thick **Poly-methyl-methacrylate** (**PMMA**) layers. In alternative the precisely defined PMMA structures can be used as a negative mold for the realization of metallic structures by galvanoplastic. This technique is able to provide structures with higher aspect ratio than optical lithography and on large numbers can result in an inexpensive fabrication technology.

At the same time when the LIGA technique was developed also bulk silicon micromachining with **Deep Reactive Ion Etching (DRIE)** based on the Bosch process became popular. This technique is based on plasma etching using fluorine based gases (CF4) and allows to create extremely high aspect ratio holes in silicon with an unprecedented flexibility in features and size. Since the introduction this technique has seen an enormous growth in use and it is now one of the most widely used fabrication technique for MEMS in the world.

Another important technique in the field of MEMS is the **galvanic deposition** of metals. Metal deposition by electroplating has become a standard process in Integrated Circuit (IC)fabrication with the introduction of the Copper based Double Damascene process now generally used for most of the many metal layers present in modern IC circuits. In combination with the ability to define thick PR layers this technique can also become interesting for

MEMS applications as it allows to build truly 3D high aspect ratio structures above the wafer surface. In time many different metals have been explored like Nickel, Tungsten and Gold.

Another more drastic 3D integration technique is the **wafer bonding** process. In this case two or more wafers are bonded together in order to build up a 3D structures beyond the limitation imposed by the wafer thickness. The bonding can be achieved in many different wayss. It can be a physical bonding of the silicon itself (called fusion bonding) or of the silicon oxide but also bonding through a intermediate layer is possible. This can be either a polymer layer (adhesive bonding) or a metal layer (eutectic or thermocompression bonding).

In the years all these techniques have been used successfully in creating new types of devices and it has been shown that the combination of these techniques with the planar technology allow the realization of new and unexpected devices.

1.2 Radio Frequency MEMS and Microwave Filters

The last ten to fifteen years have seen a widespread use of mobile communication devices which in turn required new wireless communication standards and put more challenges in the design of the hardware. From a device point of view important requirements are low power consumption, high linearity and large bandwidth, while at system level flexibilityx z in circuit design and the capability to be highly reconfigurable are important features.

RF MEMS devices allow to realize miniaturized basic components like resonators, varactors, inductors and switches which can be integrated in complex circuits. The potential application ranges from mobile phone terminals, base stations, phase array antennas, radars to complex satellite payloads.

RF MEMS devices in general exhibit superior performance in terms of

losses, linearity, power consumption and cut-off frequency with respect to solid-state devices such as PIN diodes or other active devices. For this reason the last ten years have seen a huge development e.g. of the RF MEMS switch technology which allows the realization of complex circuits like switching matrixes and phase shifters. While this is an ongoing activity, which will access the market very rapidly, also other RF devices have been realized in micromachining technology. One of these are the RF MEMS filters which aim to replace the conventional filters in many applications especially in smart phones where usually 3 to 7 RF-filters are used, which means up to 2 billion pieces per year [1]. The distinguish characteristics of RF MEMS filters which provide an edge on its traditional counter parts are small size, high Q-factor, low radiation, and low dispersion loss. The demand of cost effective and small RF components has therefore provoked a huge R&D activity that opens-up the possibility of considering them in novel applications in a wide range of applications where the MEMS technology is capable to extend the operation to higher frequencies, e.g. gigahertz (GHz) range, for satellite communication.

The above mentioned micromachining technologies in combination with the planar technology are certainly capable to build small and complex mechanical structures with tight tolerances, easy to integrate with standard printed circuits. Indeed they have been recently utilized to build so-called membrane-supported transmission lines and high Q-factor monolithic resonant structures.

1.3 Motivation

These general trends and the early results obtained by the research community pushed actors like the ESA to issue specific tenders for the realization of Bandpass Filter (BPF)s in multi layer technology. One of the granted

projects is the MIGNON project (22706/09/NL/GLC), a joined research activity involving FBK, and two companies i.e. RF μTech and ELITAL.

The primary scope of this research activity is to investigate the potentialities of the combination of micromachining techniques with multilayer structures for the realization of microwave filters in Ka (30 GHz) and L/S (4 GHz) bands. The expectation is that the combination of different micromachining technologies should result in an attractive overall performance of the filters, i.e. good RF characteristics, high Q-factor, small mass and footprint, and an easy integration with printed circuits.

In particular the high precision of the micromachining techniques and the ability to produce truly 3D structures on a small space are considered as key factors for a successful realization together with the potential cost reduction possible by the high volume production capability provided by these technologies.

1.4 Structure of the Thesis

The thesis is organized as follows. **Chapter 2** is dedicated to an analysis of the state-of-the-art on the application of micromachining techniques for the realization of microwave Bandpass Filters. It reviews the major trends in the literature including also non-silicon based techniques.

Chapter 3 introduces the design of the Ka band filters and describes in detail the developed novel process architecture, the different process runs and an auxiliary study on the thermocompression bonding.

Chapter 4 is dedicated to the design of the LS band filters. It also provides a detailed description of the process and the different fabrication runs.

Chapter 5 offers a detailed structural analysis aimed at the assessment of the sensitivity of the structures to vibrations. **Chapter 6** describes the

assembly of the devices.

Chapter 7 is dedicated to the fabrication methods for Through Silicon Via (TSV), a basic element for all the presented filter concepts. The results of the three years work are summarized in **Chapter 8** and final conclusions are drawn in **Chapter 9**.

Chapter 2

State of the Art

2.1 Introduction

This chapter reviews the micromachining and multilayer technologies used for the realization of RF MEMS filters both in Ka and L/S band applications together with different methodologies and process architectures proposed in the recent and past literature. The micromachining technology has also been adopted for the realization of filters at other frequency bands but this thesis focuses on Ka and L/S band filters. Therefore, this discussion on state-of-the-art is partitioned into two main sections, namely, literature review of Ka band filters and literature review of L/S band filters. This is done to complement the current state of affairs with the core issues in multiple stack micromachined filter topology to appreciate the necessity and importance of a research work on this particular topic.

2.2 Literature Review of Ka Band Filters

Numbers of fabrication techniques and materials have been proposed for the realization of low loss, high Q-factor micromachined filters over the last years. The most common topology on which Ka band filters are realized is the resonant cavity. Resonators made by low-loss micromachined cavities

are relatively easy to integrate with monolithic circuits, smaller in size and weight, and provide high Q-factor (i.e. >3500). On the other hand Ka band filters have also been realized in microstriplines [2], dielectric membranes [3], coaxial transmission lines or waveguides [4] which are only some of the alternative approaches by using micromachining techniques [5, 6] for obtaining high Q-factor. In the millimeter and sub millimeter wave range planar technology can be adopted to reduce weight and size, as well as to make the integration with monolithic circuits easier. Despite their advantages, conventional planar solutions show relatively high losses (i.e low Q-factor) with respect to 3D structures (e.g waveguide filters), mainly due to the losses in the substrate. Micromachining techniques can allow for realizing innovative structures presenting a good trade-off in terms of resonators Q-factor, size and integrability with monolithic or printed circuits. Most relevant topologies of filters realized by using both surface and bulk micromachining techniques, along with multilayer approach, are reported and compared in this section.

i Microstrip and Membrane Supported Filters

ii Micromachined Cavity and Resonator Filters

iii Inverted Microstrip Filters

iv Surface Integrated Waveguide (SIW)Filters

v Low Temperature Cofired Ceramics (LTCC)

Among these, the membrane-supported filters are most promising and demonstrate great potential in terms of the compatibility with existing integrated circuit (IC) technologies and ease of implementation with common micromachining techniques. Main scope of this review is to identify and analyze in some detail the fabrication technologies that have been proposed in the literature and to identify those compatible with the capabilities of FBK. As it will be seen the first three topologies mentioned above are those which can

be tagged as topologies compatible with FBK MEMS fabrication technology while the fourth and fifth topologies are incompatible with FBK MEMS fabrication capabilities.

2.3 Compatible Topologies

2.3.1 Microstrip and Membrane Supported Filters

The technology of membrane supported circuits for millimeter wave applications using silicon micromachining was firstly implemented by Rebeiz et al in 1990 [7, 8]. Membrane supported filters using silicon bulk micromachining have not only been realized in the Ka band but also in bands like Ku (12-18 GHz) [9], K (18-26.5 GHz) [10] [11], Q (30-50 GHz) [12], E (60-90 GHz) [13], W (75-110 GHz) [14–16], and higher frequencies [17].

An interesting example of suspended microstrip lines on thin dielectric membranes is presented in [18]. Where a typical micromachined suspended microstrip transmission line is composed by three wafers as shown in Fig. 2.1. The membrane is a three layered structure of $SiO_2/Si_3N_4/SiO_2$ deposited on high resistivity (HR) 525 μm thick silicon substrate and the circuit is patterned on the topside of the middle wafer (i.e. circuit wafer) and via holes are formed by etching the back side membrane with a Reactive Ion Etching (RIE) process. With this type of structure typical Q-factor of 190 could be obtained with a coupling of -4.6 dB and an extracted unloaded

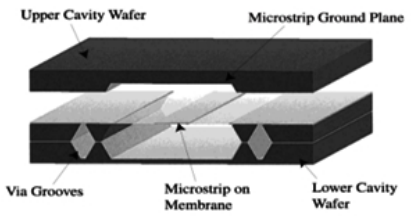


Figure 2.1: Transverse section of microstrip structure suspended on membrane [18].

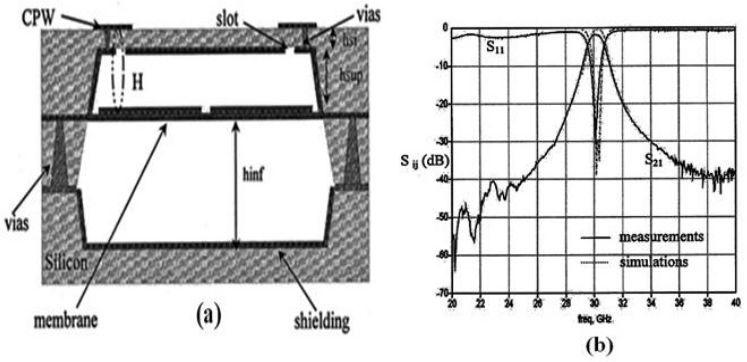


Figure 2.2: (a) Cross sectional view of a filter. Top wafer contains CPW line to feed the filter using a slot in the shielding of the upper cavity. Magnetic field provides input-output coupling of the resonators through slots. (b) Experimental results of the filter [3].

Q-factor of 460 at 28.7 GHz.

Another good example of a micromachined planar filter at 30 GHz fabricated on thin dielectric membranes is reported in [3]. Three high resistive (HR) silicon wafers have been used for making up the structure which is similar to the one presented above. A coplanar waveguide (CPW) is built on the upper wafer to keep the input/output couplings on the top of the structure thus making the device compatible with printed circuit technology as presented in Fig. 2.2.a. Experimental results have shown a Q-factor of 602 and an insertion loss of 1.8 dB for a two pole filter with 4% bandwidth around 30 GHz as illustrated in Fig. 2.2.b.

In [19] two types of membrane supported filters one with microstripline, the other with CPW are reported. In the first case a 1 μm thick Silicon Nitride (Si_3N_4) membrane was fabricated on 525 μm thick silicon substrate then the gold was deposited on top of membrane and the circuit was patterned. The suspended metalized membrane was obtained by etching away the silicon underneath the membrane area. Another metalized silicon wafer was bonded with the device wafer to form the ground plane and provide support to the structure as illustrated in Fig. 2.3

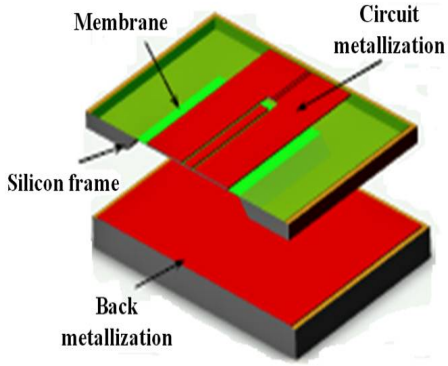


Figure 2.3: Membrane supported filter in coplanar line configuration [19].

2.3.2 Micromachined Cavity Filters

Filters at Ka band have also been realized by micromachined cavity technology, because they are easy to integrate with surface mounting devices (SMD). A good comparison between waveguide cavity filters and micromachined cavity filters is presented in [20] where a two-port micromachined cavity resonator filter is fabricated by using silicon micromachining because micromachining provide tighter mechanical tolerances. The cavity is formed by KOH wet etching (due to its high selectivity), and the two wafers were bonded together to form a filter as depicted in Fig. 2.4. The unloaded Q-factor measured (by using the formula mentioned in [21]) is $Q_u = 1410$, which is comparable with the theoretically calculated Q = 1515 of the equivalent

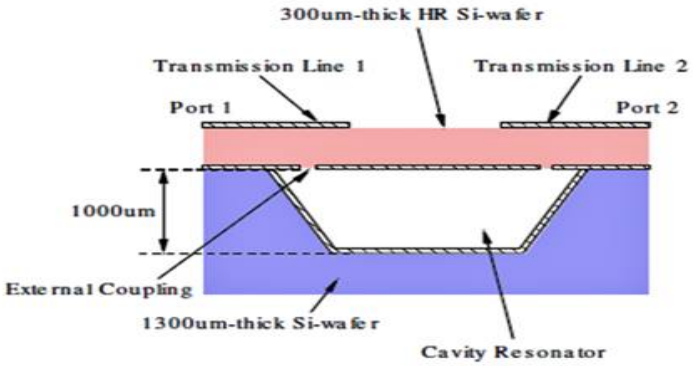


Figure 2.4: Cross sectional illustration of cavity resonator [20].

waveguide cavity resonator. The calculated resonance frequency of the cavity resonator is 19.88 GHz, which is 0.36 % less than the required resonance peak specified at 19.95 GHz.

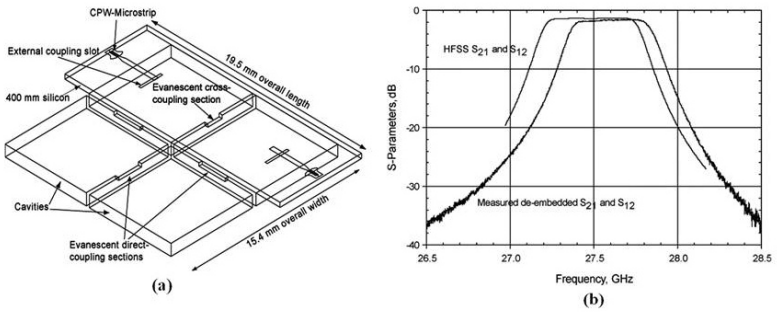


Figure 2.5: (a) Cross-sectional schematic of a four-pole linear phase filter. (b) Comparison of de-embedded measured and HFSS insertion loss [22].

A notable work on micromachined cavity filters has been reported by L. Harle et al that proposes two novel solutions, a horizontally integrated [22] and a vertically integrated [23] micromachined filter. In the first case, two silicon substrates have been etched, metalized and then bonded one on top of the other to realize the cavity. Four cavities have been coupled in order to obtain a four pole linear phase filter which dimensions are 20 mm x 15 mm as depicted in Fig. 2.5.a. The measured unloaded Q-factor is 1456, the bandwidth is 1.9% and the de-embedded insertion loss is 1.6 dB at 27.6 GHz as illustrated in Fig. Fig. 2.5.b.

A similar approach with a rather unique concept has been presented in [24] where 14 silicon double-sided etched wafers are width stacked in order to avoid convex corners to the etching process as shown in Fig. 2.6.a. However, the proposed arrangement of stacking the cavities makes it difficult to integrate it with Monolithic Microwave Integrated Circuits (MMICs) and its length is pretty large, about 40 mm. Due to deep etched cavities the measured quality factor $Q_0 \sim 4500$ at 29.7 GHz.

In [24], a 10GHz three-pole band pass cavity filter is realized in a multilayer

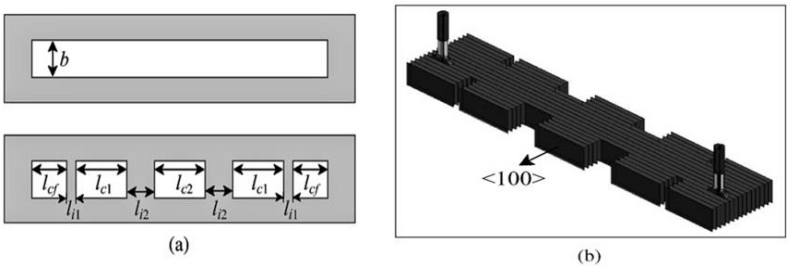


Figure 2.6: (a) Layout of etched silicon wafer pieces. (b) perspective view of width stacked filter design in [24].

micromachining techniques by combining four 500 μm thick, three 100 μm thick and one 400 μm thick high resistive (HR) Silicon (Si) wafers. The wafers are properly etched, metalized and vertically stacked in order to create a three cavity as shown in Fig. 2.7.a.

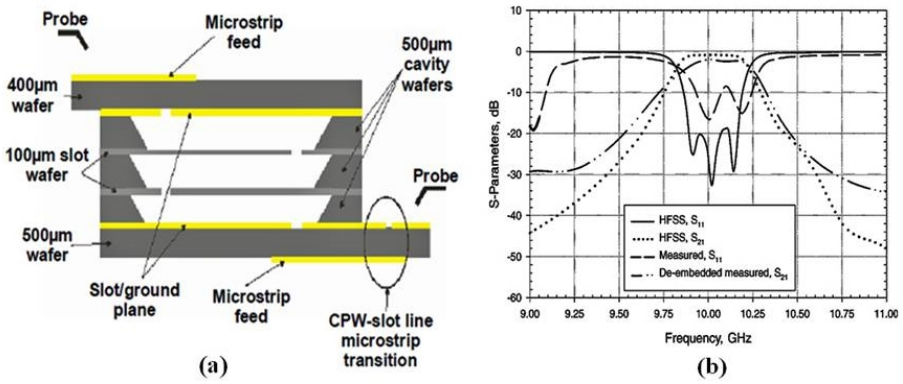


Figure 2.7: (a) A vertically stacked 3 cavity filter. (b) HFSS simulation of three cavity filter [23].

The cavities are slot coupled to each other and microstrip slot coupled transmission lines have been implemented as feeding line. The unloaded Q-factor has been calculated to be theoretically equal to 565, whereas simulated insertion loss is 0.9 dB at 10.02 GHz for a 4% bandwidth as shown in Fig. 2.7.b. Measured insertion loss is 2 dB, worsened by CPW to microstrip transition and some process misbehavior. The filter is very compact, resulting in total dimensions of 16 x 10 x 2.7 mm^3. It is also notable that the design depicted in Fig. 2.7.a does not allow a surface mountable configuration,

since the input and output ports are on different layers. However, the design could be in principle be modified, in order to have both the input and the output ports on the same layer allowing for surface mounting compatibility.

The same concept could be applied at higher frequencies (such as Ka band frequencies) where micromachined cavities have demonstrated excellent performances as described in [22] in terms of size reduction and Q-factor improvement. Furthermore both vertical and horizontal multilayer approach provides significant reduction in footprint. External transmission lines on top of the first layer (e.g. microstrip) can feed input/output filter cavities by means of coupling slots in the common ground plane as depicted in Fig. 2.2, Fig. 2.4, Fig. 2.5.a, Fig. 2.7.a.

Another example of filter realized by employing etched cavities is reported in [25] where micro-machined, multilayer cavity resonators and filters at 38 GHz are demonstrated. Each layer is made of gold-coated silicon, structured by deep reactive etching. Two external coupling structures by coaxial feeding lines are proposed to suit the fabrication process. The measured resonator gives an unloaded Q-factor of 343 at 38 GHz. The structure is depicted in Fig. 2.8. In order to increase the Q-factor the authors suggest to improve the quality of the metallic shielding process as well as increasing the cavity height. The measured insertion loss of the second-order filter is 1.01 dB; the 3 dB bandwidth is from 36.53 to 39.13 GHz.

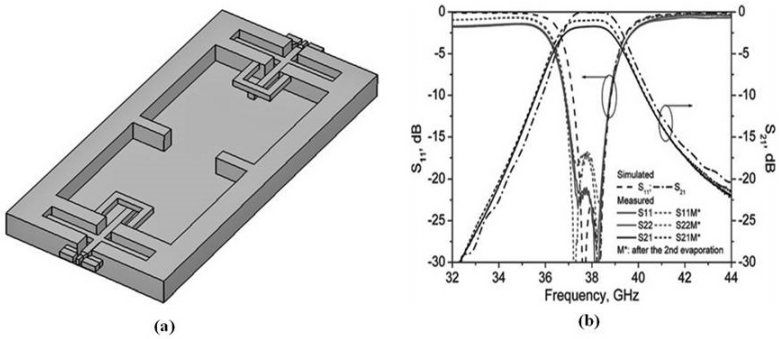


Figure 2.8: (a)Perspective view of cavity filter.(b) Measurements of a two cavity [25].

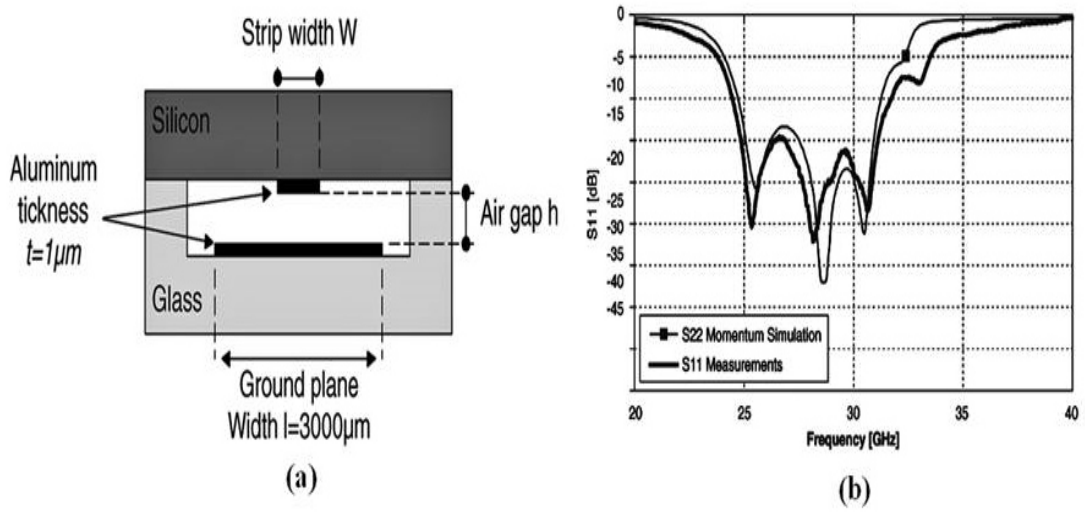


Figure 2.9: (a)Cross sectional view of inverted line on Silicon. (b) S parameters measurements [26].

2.3.3 Inverted Microstrip Filters

The concept of inverted microstrip lines has already been used in antennas and transmission line applications and in [26] this is proposed for the realization of low cost filter in Ka-band at 30 GHz. Both, glass and silicon substrates, were etched and bonded at 380° under a 400-V polarization by using anodic bonding. To realize an inverted line on Silicon, a cavity was formed in a glass substrate by glass wet etching and then metalized with sputtered aluminum for defining the ground plane and RF access. With the help of lithography and DRIE Coplanar Waveguide (CPW) was created for measurement purposes, For lines on glass the fabrication process is similar to that of silicon the only difference is that the line is design at the bottom of cavity while high resistivity silicon (HRS) $>$ 4000 Ω.cm substrate is used as ground plane. In this type of configuration the air gap plays an important role in attenuation loss measurement which increase and decrease with the variation of the air gap and also in defining the good resolution for the line geometry in the bottom of the cavity as depicted in Fig. 2.9.a.

Finally it is worthwhile to show the pretty interesting concept presented in [27]. Where 8 μm thick microstrip gold resonators are electroplated on the silicon substrate which are afterwards removed from the backside by DRIE etching. The resonators are fixed at the substrate in correspondence of hollow support posts realized in their central part as anchored cantilever beams. A top capping made of a etched and metalized silicon wafer is then used to cover the resonators and realize the top ground plane of the microstrip, providing an inverted-microstrip cantilevers filter. A three-pole filter, depicted in Fig. 2.10, has been fabricated by using such a technique. As a result, a minimum insertion loss of 2.95 dB and a 9.8% bandwidth are achieved at 59.7 GHz. Despite this technology can be easily adapted for tunable RF MEMS applications, manufacturing problems may arise as free standing beams can suffer from gradient stress and mechanical failure. Moreover, insertion loss of such a structure is not so low (i.e. Q-factor < 100), if compare with membrane or micro-machined cavity filters.

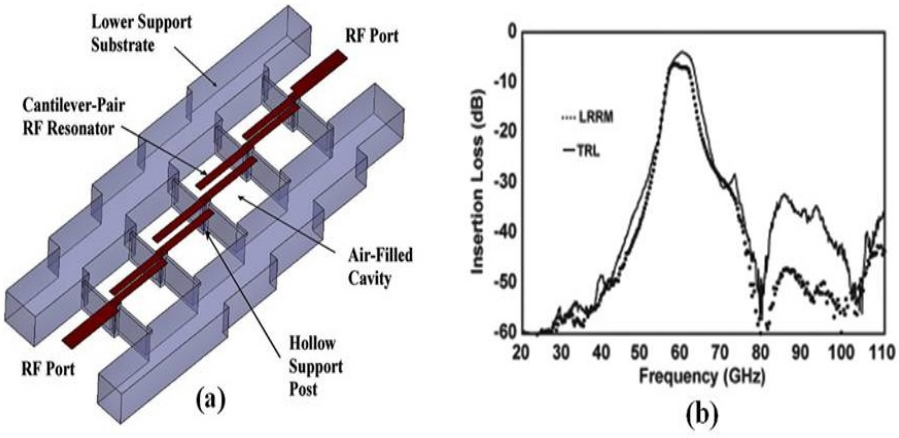


Figure 2.10: (a) Inverted microstrip filter. (b) Broadband measurements [27].

2.4 Incompatible Topologies

2.4.1 Surface Integrated Waveguide (SIW) Filters

The SIW is another interesting application of silicon micromachining and sufficient literature is available on microwave circuits based on SIW [28]. Micromachining techniques have also been used in combination with SIW filter designs [29], which up to now have been commonly realized by using standard Printed Circuit Board (PCB) or LTCC techniques [30]. In this case a 400 μm-thick silicon substrate is used as dielectric inside the cavity. Metallic via holes along with gold layers on the top and on the bottom of the structure act as metallic walls of a rectangular waveguide, as depicted in Fig. 2.11. The unloaded Q-factor is 341, whereas the insertion loss for the manufactured four - pole filter is 0.5 at 30 GHz for a bandwidth of 6.5%. Employment of dielectric material in the whole filter volume reduces the footprint, but increases the insertion loss.

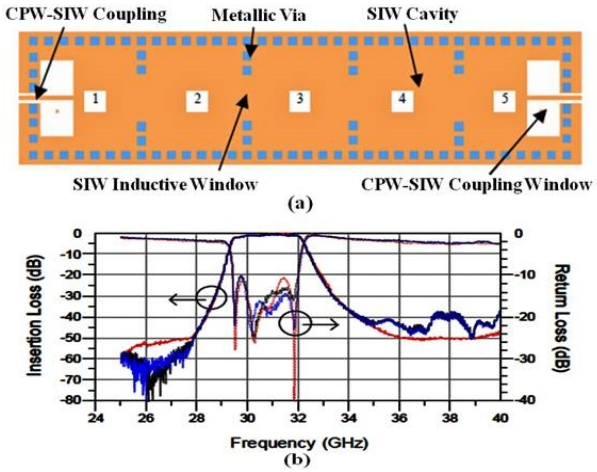


Figure 2.11: (a) Configuration of the micromachined SIW filter.(b) measurements [29].

A similar concept is reported in [31], where a two-pole filter has been realized based on resonant dielectric-filled cavities made in a 100 μm thick silicon substrate in Multi-Chip Module technology (MCM), as shown in Fig.

2.12. In this case, via holes are not completely filled with metal but only

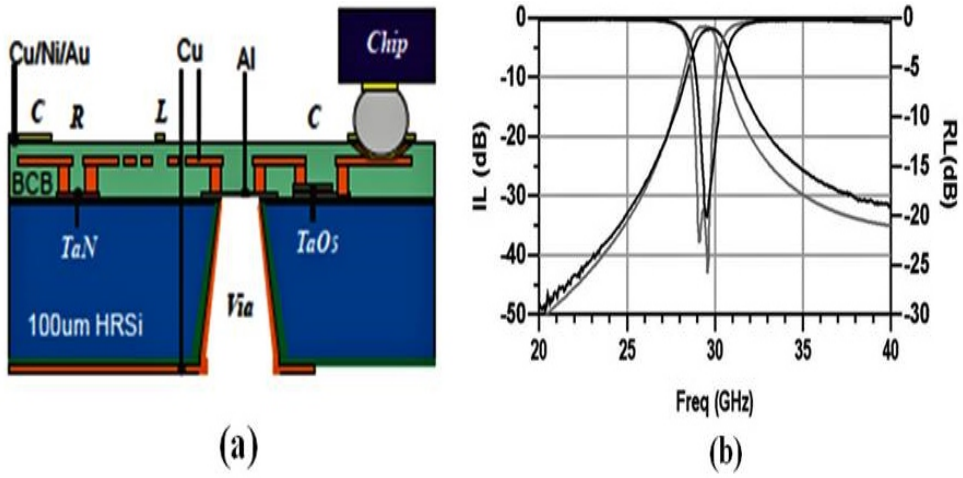


Figure 2.12: (a) MCM technology with TSV. (b) Measurements [31].

their internal surface has been metalized. No wafers stacking are required and smaller dimensions are achieved with respect to air-filled cavities. However, as expected, the presence of the dielectric and the small height of the guide lead to increased insertion losses: the simulated unloaded Q-factor is relatively low (about 176 at 29 GHz) when compared with solutions obtained by using micro-machined cavities. The measured insertion loss is 1.85 dB at 29 GHz, which is quite high for a two poles filter. At present FBK cannot easily realize metalized via holes through silicon or quartz substrate that's why this topology is not suitable for the current work.

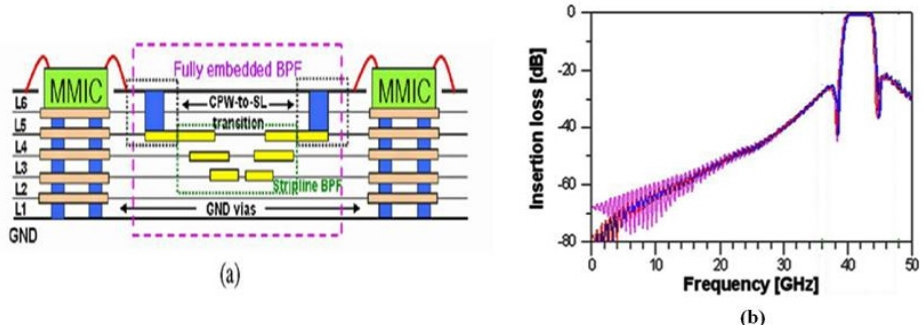


Figure 2.13: (a) LTCC structure with embedded filter. (b) measurements [32].

2.4.2 Multilayer Filters on Low Temperature Co-Fired Ceramic (LTCC)

LTCC is a multilayer technology and it has been recently adopted in [32] to embed distributed Ka band elements filters in a multi-layer structure, where also mixers and amplifiers can be mounted in an efficient way, as shown in Fig. 2.13. In this case, coupled resonators are placed over different dielectric layers, in order to realize a complete embedded band-pass filter and minimize the space occupation. Very good performances have been observed for four poles filters with 1.9 dB insertion loss and 10.5% bandwidth at 41 GHz. However, such a solution does not offer advantages with respect to previously described micro-machined cavity filters, in terms of Q-factors and feasibility. Similar results have been obtained also in [33] at 20 GHz. Therefore due to unavailability of both SIW and LTCC technology in FBK these technology concepts have not been considered further.

2.5 Literature Review of L/S Band Filters

In literature several methods have been adopted for integrating high Q-factor resonators using micromachining technology at lower frequencies especially at L and S bands. Recently suspended resonators or cavity based designs are emerging for lower frequencies such as L/S band but in L/S band cavity filters cannot be easily implemented despite of their Q-factor as they would result extremely bulky, heavy and space consuming devices [34]. Typical dimension of a rectangular resonant cavity at 2 GHz are about 10 cm x 5 cm x 10 cm. Such a cavity allows for Q-factor above 14000. Therefore, microstrip and coplanar waveguide are the most common topologies used for the realization of smaller filters in the L/S band applications such as Wireless area network (WLAN) and Bluetooth [35].

In [36] a L/S band two-pole filter is presented, where coupled planar res-

onators are patterned over HR silicon substrate in a very small area (7.5 x 4 mm^2). The filter shows a measured Q-factor of 150, leading to an insertion loss of 1.5 dB at 5.15 GHz. This is one of the best results in terms of unloaded Q-factor achievable in conventional planar technology. As it is for high frequency applications, micromachining technology can improve the performances of these consolidated designs by providing lower losses with respect to standard IC technology. Some of the most common topologies used for the realization of lower frequency band filters are: :

i Lumped Element Filter on Membrane

ii Semi Lumped Element Filters

iii Multilayer Filters

iv Lumped Element Filters on LTCC

v Planar Filter on Low-Loss High Permittivity Substrate

vi Substrate Integrated Folded-Waveguide Filter

The above mentioned topologies in case of L/S band filters can further be defined as topologies compatible with FBK's MEMS fabrication technology and topologies incompatible with FBK fabrication technology.

2.6 Compatible Topologies

2.6.1 Lumped Element Filters on Membrane

Compact wireless applications require miniaturized planar tunable filters based on MEMS, and lumped elements technology is most often the best solution at low frequencies. Micromachining lumped-element filters in general show higher performance with respect to standard integrated circuits

due to both the high tolerances of the process and the lower loss of the substrates, especially in case of membrane filters. Normally standard integrated inductors on Complementary Metal Oxide Semiconductor (CMOS) and SiGe substrates show Q-factor of about 12 - 18 at 2 GHz and in case of ferrite material approximately 20 at 1 - 2 GHz [37], while most of the micromachined inductors have a Q -factor greater than 30 [6] and micromachined Metal insulator metal (MIM) capacitors can reach the value of 100 at 2 GHz [10]. In general, lumped element circuits are widely used in the lower frequency band for size reduction where also the parasitic couplings are very low. In [38] the measurements of some lumped capacitors and inductors on membrane show significantly reduced loss compared to standard thin film technology. A very small size lumped element membrane filter has been developed in [39] by exploiting FBK MEMS technology, as shown in Fig. 2.14. The filter consists

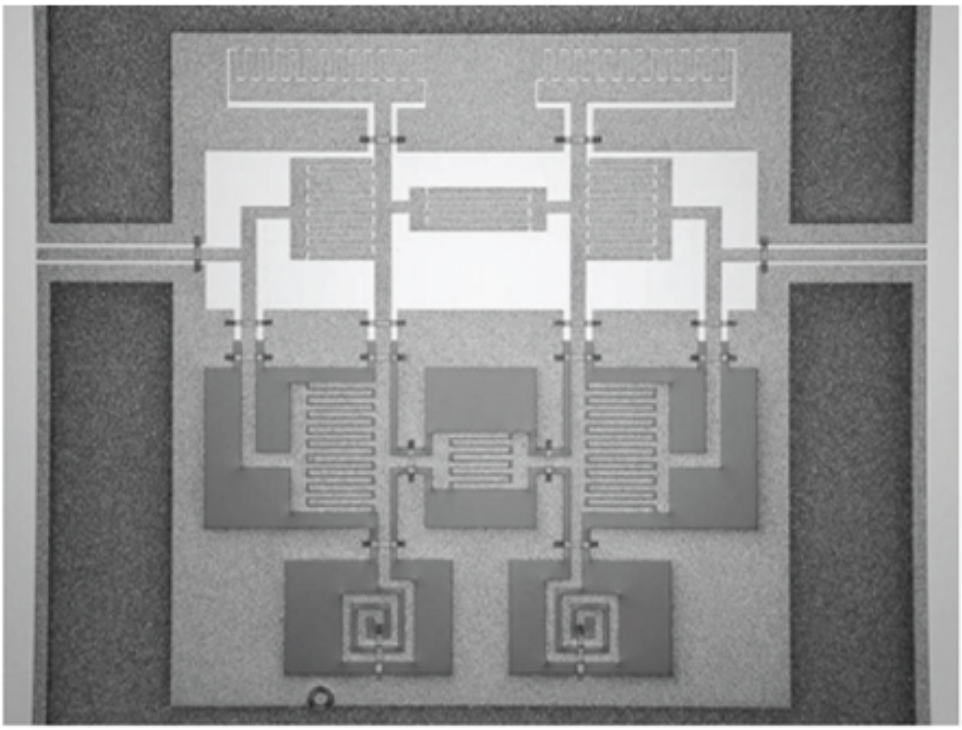


Figure 2.14: FBK's membrane filter [39].

of interdigitated capacitors and inductors on a membrane. The membrane is

made of a $SiO_2/Si_3N_4/SiO_2$ layers and shows high flatness and high mechanical stability. Nonetheless the results of solutions based on lumped elements on membrane prove that their employment is not acceptable when the desired resonator Q-factor is above 200.

2.6.2 Semi-Lumped Elements Filters

Semi-lumped element filters for the L/S band are proposed in [40], where thin dielectric layers are disposed in alternation with gold conductive layers as depicted in Fig. 2.15.

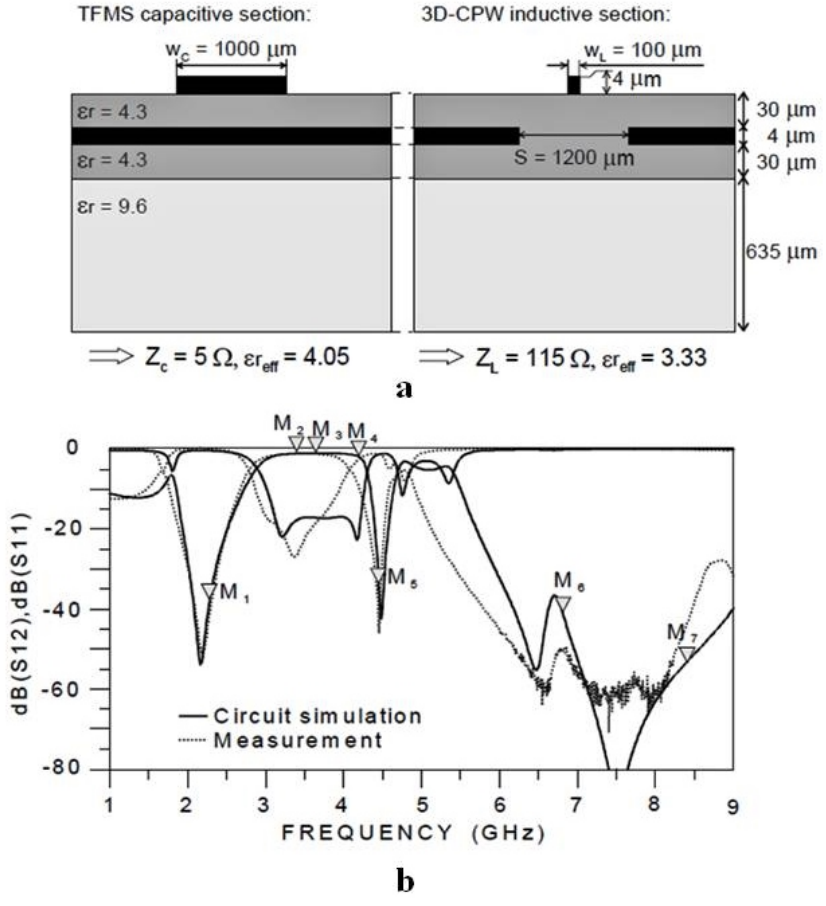


Figure 2.15: (a) 2 multilayer configuration. (b) measurements of 2nd order filter [40].

Two line configurations, namely thin film microstrip and 3D-CPW, have been implemented, allowing for the design of a second-order semi-lumped

element filter. The overall size is 11.4 x 13.2 mm^2. Good performances are achieved showing insertion loss 1.03 dB at 3.65 GHz, but with 28% relative bandwidth and an estimated unloaded Q-factor below 50.

2.6.3 Multilayer Filters

The multilayer approach is a good trade-off in order to reduce the size without degrading the Q-factor of a BPF (BPF) at L/s band. A multilayer structure is presented in [41], providing a four pole filter consisting of two folded quarter-wavelength resonators in U shape patterned on the top dielectric layer and two other quarter wavelength folded resonators on the bottom dielectric layer as shown in Fig. 2.16.

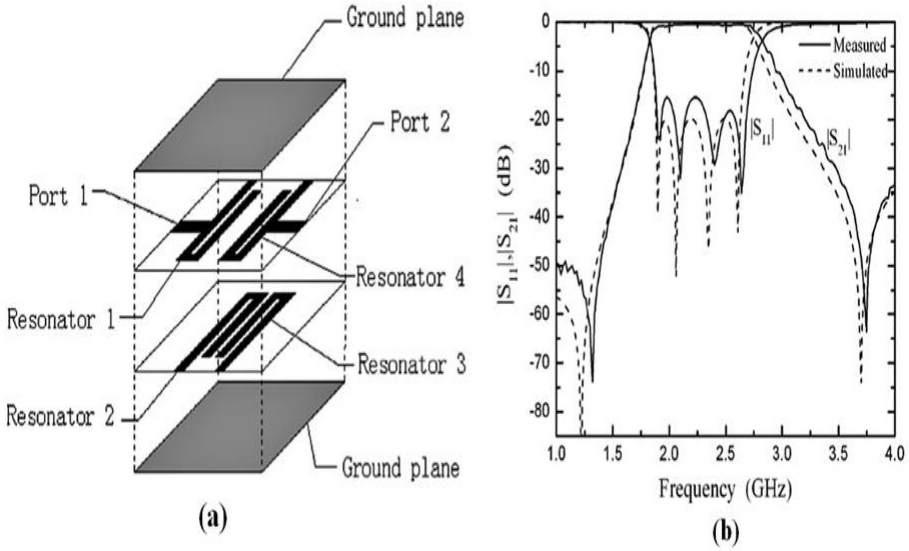


Figure 2.16: (a) Scheme of multilayer filter. (b) measurements [41].

The overlapping between the resonators leads to reduced filter size and provides wide band and cross coupling between nonadjacent resonators. A bandwidth of 31% at 2.25 GHz is obtained, with 1 dB insertion loss at the central frequency. The final dimensions of the filter employing substrate with 2.55 relative permittivity are 10 x 13 mm^2. Similar structures with

comparable results are also reported in [42]. Improvements in terms of Q-factor (> 400) can be obtained by realizing the quart-wavelength resonators on a micro-machined membrane, so as to reduce the loss due to the dielectric substrate. Such a solution will lead to an increase of the filter size due to the air-like substrate. However introducing additional folds of the resonators could reduce the footprint further.

Also [43] presents a new compact two-layer microstrip BPF using multi-layer cross-coupled improved interdigit-loop resonators Fig. 2.17. The filter

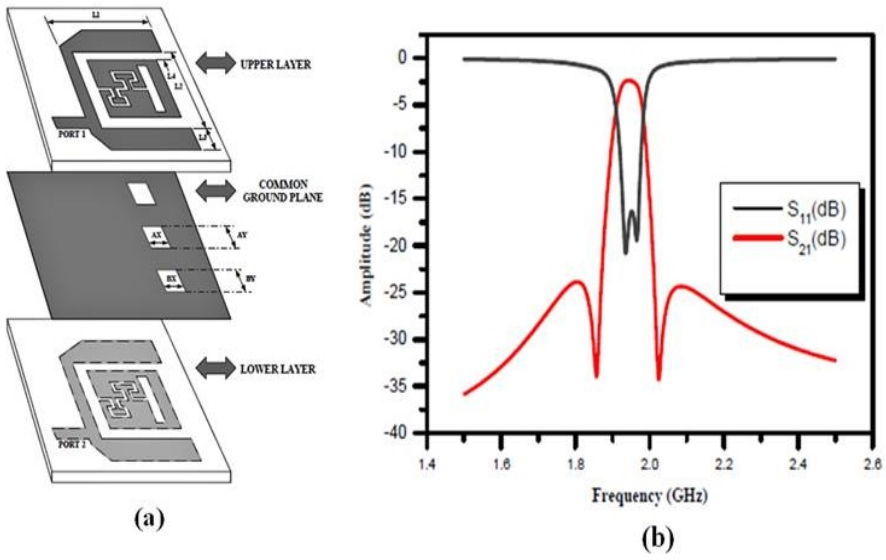


Figure 2.17: (a) Schematic of multilayer filter. (b) measurements [43].

structure consists of four resonators placed on two microstrip stack layers. The coupling between the resonators on the upper layer and the lower layer is obtained by using three coupling apertures on the common ground plane. The filter has been optimized in order to achieve low passband insertion loss (< 3 dB) at the central frequency (around 2 GHz) with 3% relative bandwidth. By using this two-layer technique in the microwave filter design, a filter size reduction of about 50% is obtained.

In [44] the resonator coupling in a similar multilayer structure is investigated. Different types of apertures in metallic sheets are used as coupling el-

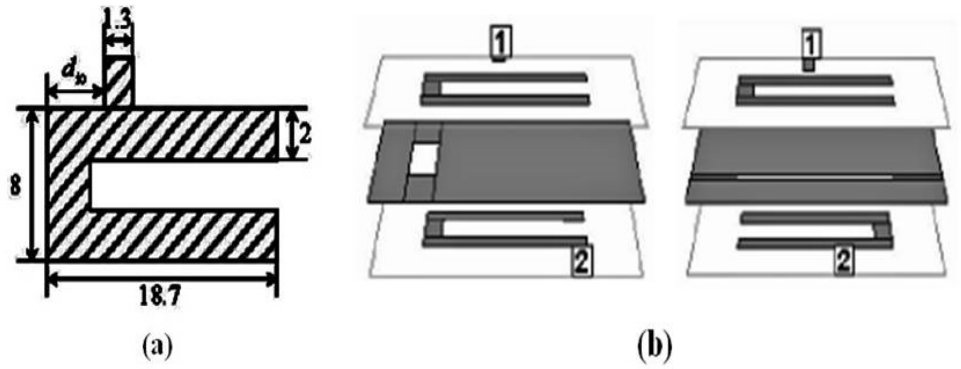


Figure 2.18: (a) Coupling of first resonator with its feeding line. (b) Internal ouplings by slots [44].

ements between resonators located on different layers, allowing very compact filter designs. The couplings between resonators are obtained by cutting one or two rectangular slots, with different lengths and widths, in the common ground plane between resonators. Due to their small sizes, these apertures exhibit resonant frequencies far above the filter's passband, with almost no influence on the electrical responses in the band of interest. Regarding the input/output couplings, the configuration of a resonator coupled to its 50 Ω microstrip feeding line is shown in Fig. 2.18. The position of the feeding line with respect to the folded resonator defines the input/output filter couplings.

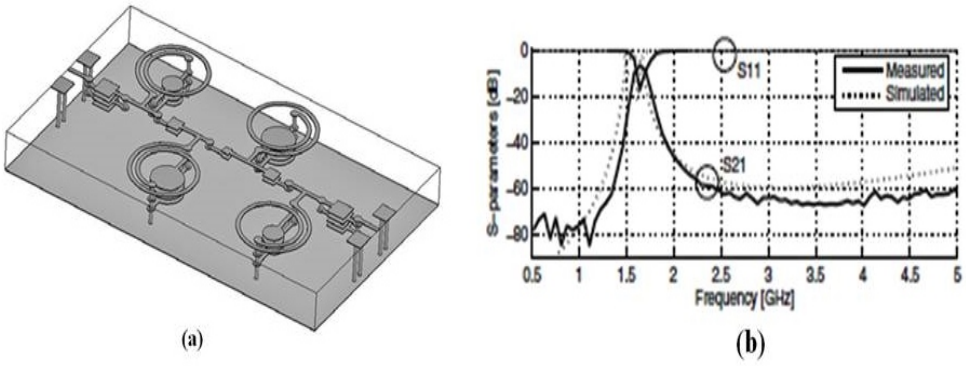


Figure 2.19: (a) 3-D lumped element filter structure. (b) measurements [45].

2.7 Incompatible Topologies

2.7.1 Lumped Element Filters on LTCC

LTCC is a multilayer 3D technology and recently it is widely used in RF circuits due to its merits (i.e. high integration density high reliability and high performance). Filter based on LTCC technology is presented in [45], where a very small size (5.5 x 9 x 0.8mm^3) lumped element BPF is reported. In this case parallel plate capacitors and spiral-shaped have been used as shown in Fig. 2.19.

The filter is designed to have insertion loss of 6.7 dB at 1.64 GHz and a Q-factor of 45.65. Due to the low LTCC process tolerances there is a significance mismatch between simulation and measured Q-factor. The simulated Q-factor is 50% is higher than the measured one. A similar type of filter based on spiral shape inductors, having Q-factor 86, and with comparable results is presented in [46]. LTCC technology has also been used to implement a lumped-element BPF design as presented in [47, 48]. Such a filter demonstrates a 4.2 dB insertion loss at 2.4 GHz for 4.6% bandwidth. Also in this case lower tolerances lead to mismatch between simulation and measurements. Another novel approach of tunable microwave filter based on LTCC has been adopted in [49] where a tunable bandpass filter has been developed by using LTCC processing of DuPont 951 Greentape^{TM} with permittivity of 7.8 and a loss tangent 0.002. The overall dimension of final device is 12x7mm^2 and the centre frequency of filter can be tuned from 0.8 to 2.4 GHz with an insertion loss of 7 to 3 dB throughout the tuning range. The filter design has been optimized to minimize the air gap inside piezoceramic tunable capacitor and all microstrip coupled lines are placed on top of the LTCC substrate at equal level resulting in wider tuning in controlled fashion as shown in Fig. 2.20.

In the proposed filter screen printing is performed to metalize the top and

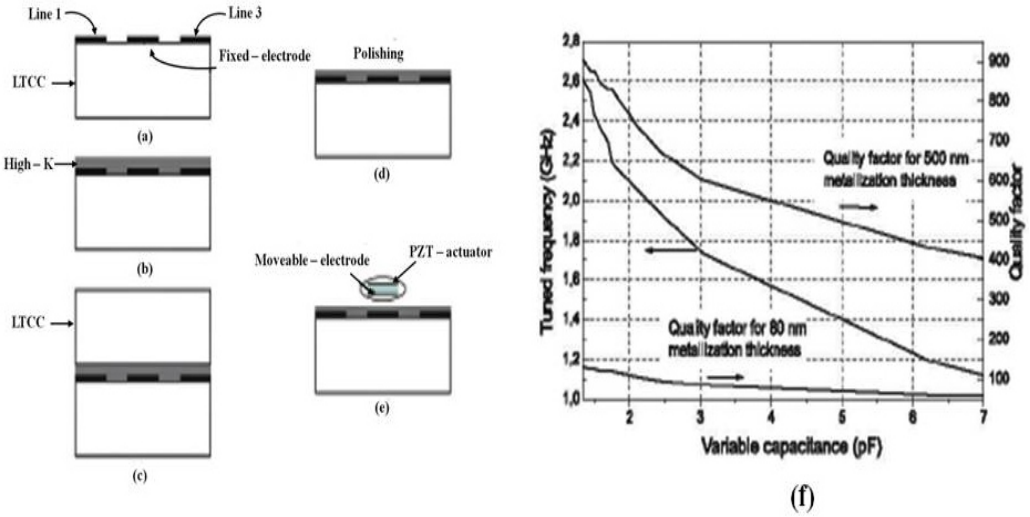


Figure 2.20: Different process steps (a - e). (f) experimental results [49].

bottom surfaces of the LTCC substrate, see Fig 20(a). The high-K tape is used to provide dielectric layer between the capacitor electrode, Fig. 20(b). Additional tape was stack on top to stabilize the sintering process effects Fig. 20(c), next polishing was performed to remove the tape until the high-K tape surface appeared, Fig. 20(d) and finally the cantilever was placed as shown in Fig. 20(d) and Fig. 2.21.

2.7.2 Microwave Filters on High Permittivity Ceramics

Another topology of filters employed in L/S band applications deals with the use of low loss high dielectric permittivity substrates. For instance, two filters one at 5.2 GHz and other at 2 GHz frequency range based on this approach have been reported in [50, 51]. In the first case a 5.2 GHz stripline filter consists of two ceramic tiles substrate with a transmission line circuit printed on a thin, low permittivity substrate and is crammed between the two ceramic substrate as shown in Fig. 2.22.a. The transmission line is 3 mm wide with a measured relative permittivity of 38 and characteristic impedance of 12.5 and an unloaded Q-factor of 300. The insertion loss of

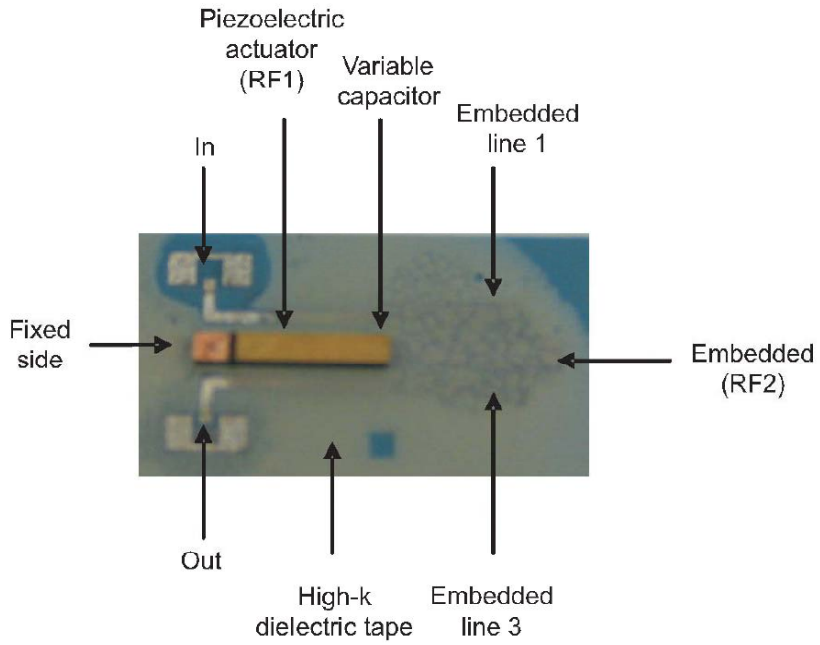


Figure 2.21: Photograph of fabricated tunable bandpass filter [49].

the SiO_2/Si_3N_4 pole filter with 200 MHz of bandwidth at 5.2 GHz is 1.5dB as depicted in 2.22.b. The input and output terminals are formed at the extended end of the low permittivity substrate, while the grounding can be obtained by a conductive coating of the outside face of the structure. In the second case a 2 pole bandpass Chebychev filter with centre frequency of 2 GHz and with a bandwidth of 500 MHz using end-coupled filters has been designed. The measured mid-band insertion loss of this filter is 3dB. Half of this is caused by the reflection.

2.7.3 Substrate Integrated Folded-Waveguide (SIFW) Filter

SIFW resonators can be employed in order to reduce the filter encumbrance because both, resonator topology and dielectric substrate are key parameters in determining the volume of the microwave filter. An example of a novel

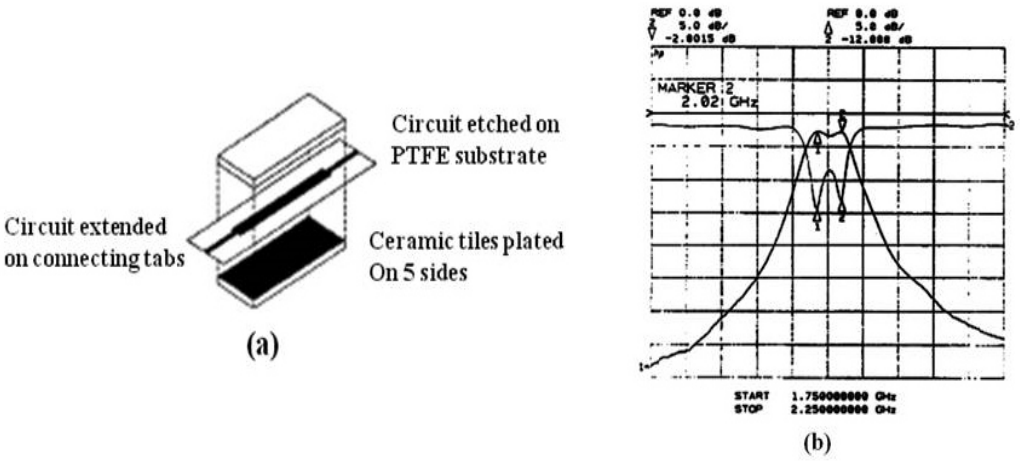


Figure 2.22: (a) Design of ceramic stripline filter. (b) measurements [50].

two-pole SIFW filter is presented in [52]. The filter is based on multilayered direct and cross-coupled folded quarter-wavelength resonators. The SIFW filter with two folded SIW cavities was designed and fabricated from a two-layer PCB substrate with a dielectric constant of 3.2 and a substrate thickness of 0.762 mm. The filter is composed of two identical portions which are separated by a 0.03556 mm thick copper wall. The coupling between cavities is controlled by a aperture "G" between the resonators as shown in Fig. 2.23. The center frequency and bandwidth of the designed filter are 4.7 GHz and 210 MHz, respectively. The diameter of the via holes is 0.7 mm and the distance between metallic vias is 1.5 mm. The overall dimension of the device along with two sides for the stripline transitions is 25x12.5 mm. Fig. 2.23 presents measured and simulated results of the two-pole BPF. The proposed filter can also be fabricated by employing LTCC and Liquid Crystal Polymer (LCP) technologies.

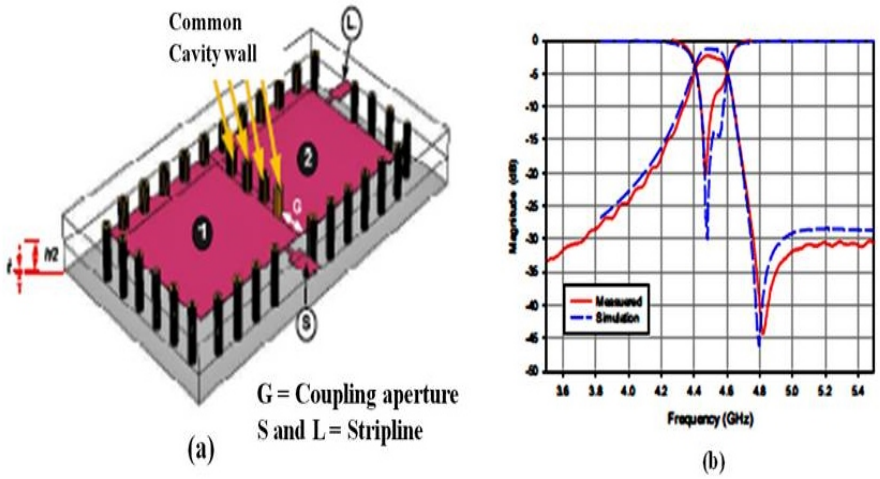


Figure 2.23: (a) 3D structure of proposed SIWF. (b) comparison of simulated and experimental results [52].

2.8 Conclusion

Ka Band Filter

The filters so far fabricated are just a small number of examples that show the performance potentialities of this micromachining technology. These micromachined filters are CMOS technology compatible and can be produced in large number in a batch process and are cost effective. The open thin film structures suffer from radiation and ohmic losses. However, closed structures such as coaxial cables do not suffer from radiation losses and with the correct design they have low losses. Both coaxial and planar structures are well suited for microfabrication, where the design of the devices is largely limited in two dimensional (2D). For this reason, MEMS filters have gained attention from researchers.

At Ka band frequencies the best RF performances are obtained with metallic cavity structures, where unloaded Q-factors of 4500 can be reached [53]. They can be realized in traditional waveguide or coaxial technology as well as by using micromachining techniques. Typically the latter allow an easier integration of the filter with off-chip MMIC especially when sur-

face mountable designs are developed. A multilayer approach, which implies both a vertical and horizontal development of the filter structure, can also allow a significant size reduction as presented in [22, 23]. Planar or substrate supported filters mainly rely on substrate thinning or removal.

At Ka Band frequencies planar filters have been realized and in this case the removal of the substrate has increased the Q-factor of the filter due to almost negligible dielectric membrane loss. Membrane supported resonators could reach a Q-factor of around 1000, i.e. ten times higher than analogous devices on standard RF substrates. Membrane supported filters have usually a large footprint that can in principle be reduced by adopting multilayer micromachining techniques, but the application of membrane filter at Ka band in a more sophisticated stacked structure has not been fully proven yet. Therefore, so far, multilayer filters employing micro-machined cavities can be considered the best trade-off in terms of Q-factor (i.e. insertion loss) and size reduction. The surface mounting compatibility can be obtained by properly designing both input and output ports on the same layer. The filter feed can be realized by using transmission lines on the top layer (e.g. microstrip or coplanar) slot-coupled to the filter cavities. In this kind of transition, the input/output access and the filter input/output coupling mechanism are coincident. Such input/output filter couplings have proved acceptable and reliable for narrow band filters, as those reported in [22].

L/S band filter

On the other hand, high performances L/S band filters are generally designed in lumped or semi-lumped element topologies allowing for size and footprint reduction, especially when implemented in multilayer configuration. However, such solutions do not allow for reasonable high Q-factor (> 200). Recent works show a widespread use of multilayer passive circuits realized in LTCC to minimize radiation losses and dispersion and to achieve a high ca-

pability of integration with off-chip MMIC. However the achievable Q-factor of lumped and semi-lumped resonators is not so high and typically comprises between 30 and 150 [6]. The filter quality factor can be improved by adopting micromachining technology and in particular membrane components, at the expenses of higher overall dimensions. Cavity filters in L/S band are rarely used since they would results in extremely bulky, heavy and space consuming devices. So far, the best compromise between dimensions and Q-factor for L/S band filters deals with the use of multilayered structure as presented in [41], where folded quart-wavelength resonators are patterned on different dielectric layersFig. 2.16. The overlapping between the resonators allows the couplings and leads to reduced filter size.

Moreover it provides wide band and cross-coupling between nonadjacent resonators, allowing also for the introduction of transmission zeros in the filter stop band. Q-factor improvements (> 400) can be obtained by patterning the quart-wavelength resonators on micro-machined membranes, so as to reduce the loss due to the dielectric substrate. Such a solution would lead to a filter footprint increase that could be reduced by additional folding of the resonators, or by using more vertical layers so as to obtain a more compact design.

The surface mounting compatibility of the filter can be obtained by adopting vertical via-holes to connect the external feeding lines (e.g. microstrip or coplanar) with the filter resonators. Such a transition presents the advantage of separating the input/output access from the filter input/output coupling mechanism but requires the implementation of metalized via-holes.

Chapter 3

Design and Fabrication of Ka Band Filters

3.1 Introduction

This chapter introduces the evolution of the design activity performed by the development team from the first concepts till the preliminary design. The design was a highly interdisciplinary activity where the technology concepts had to be developed in parallel to the designs. This work make use of an amalgam of methods and approaches adopted principally from fabrication/technology point of view in order to match the electromagnetic design with a feasible technology. Simulations are always compared against the ESA specifications but also against the known or estimated achievable fabrication tolerances. Finally a concept for a 4^{th} order Ka band pseudo-elliptic filter based on Transverse Electromagnetic (TEM) resonator has been proposed. To achieve this the original approach based on Transverse Electric (TE_{101}) resonant cavities had to be abandoned in favor of TEM resonators, which can more easily be build with the required tolerances.

Based on this technology and design concept simple test structures, 1-port and 2-port resonators, and two 2^{nd} order filters were next designed in order to allow the test of the proposed technology approach on a simplified structure.

The fabrication of the test structures is based on readily available 500 μm thick high resistive silicon wafers.

3.2 Filtering Function and Filter Topology Analysis for Ka Band Filter

The filter design starts with the identification of a suitable filter function. Fig. 3.1 presents a Ka band filter function for a 600 Q-factor resonators, while the related electrical requirements are reported in Table 3.1. The simulation results predicts that all ESA electrical requirements can be fulfilled by employing the proposed multilayer micromachined-cavity filter topology [23] and a 4^{th} order filtering function with two symmetrical transmission zeros.

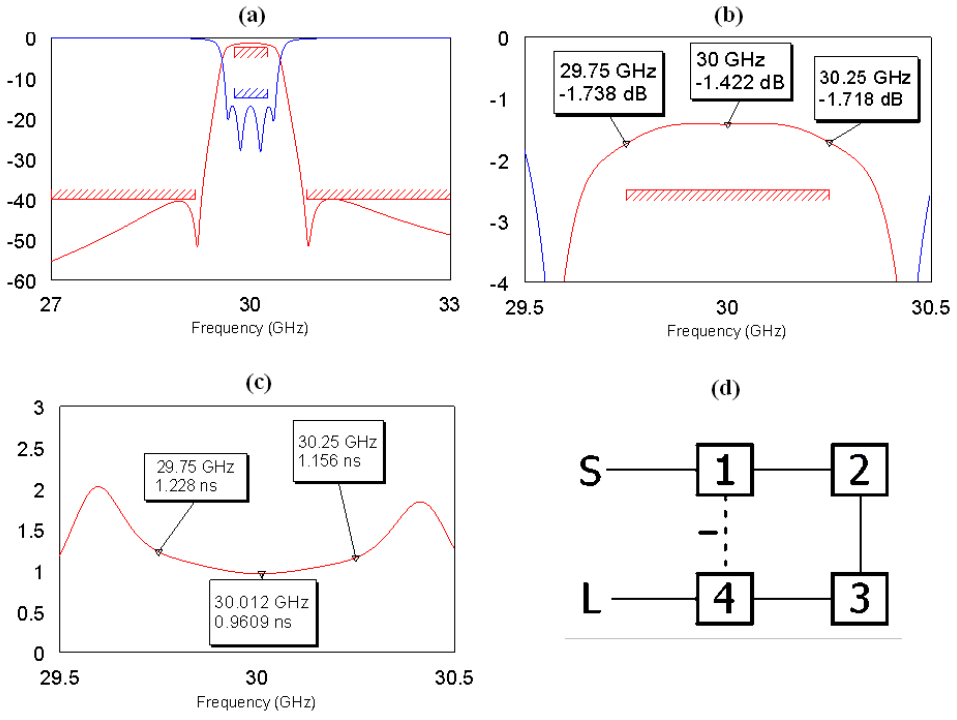


Figure 3.1: Fourth order filtering function with two TZs, and Q = 600: (a) S-parameters, dB; (b) in-band S21, dB; (c) group delay, ns; (d) a possible filter topology. Courtesy: UNIPG.

Table 3.1: Compliance matrix for the electrical requirements of Ka band filter.

ID	PARAMETER	VALUE	UNITS
K1	Centre frequency (fC)	30000	MHz
K2	Useful bandwidth	500	MHz
K3	Maximum insertion losses over bandwidth	2.5	dB
K4	Peak to peak insertion losses flatness	0.3	dB
K5	Maximum S11 and S22	-15	dB
K6	Group delay variation over bandwidth	1	ns
K7	Out-of-band rejection: fc ± 840 MHz to fc ± 10000 MHz	40	dB
K8	Nominal input power	10	dBm
K9	Operating temperature	-10 to +75	°C
K10	Storage temperature	-30 to +90	°C
K11	Mass	TBD	g
K12	Footprint	TBD	mm^2
K13	Interface	SMT like	-

3.3 Evolution of the Ka Band Filter Design

Over the past few years microwave and millimetre wave filters have been realized by employing a variety of resonators which are basic components of the filters. The filters based on waveguide cavity resonators exhibit good performance in terms of insertion loss but are bulky and cumbersome to integrate with a printed circuit board (PCB) [54]. On the contrary microstrip resonators are easy to integrate but are restricted in terms of Q-factor [55]. In recent times the integration of cavities in planar technology has been pursued to implement high quality passive components, such as resonators and filters. Micromachined cavity resonators are particularly suitable for higher frequencies from 20 GHz up to 100 GHz and can be used to achieve very high Q-factors [23] when compared to other conventional substrate supported architectures, except the bulky cylindrical or rectangular waveguide resonators.

The choice of suitable filtering functions and the corresponding filter topologies, as well as the identification of the needed quality factor and physi-

cal realization of the resonators, are the key aspects of microwave filter design especially in case of bandpass filters. The principal figure of merit for a resonator is the unloaded Q-factor which can be defined as the amount of energy stored within the resonator divided by the average power dissipated inside the resonator.

$$Q_0 = \omega_0 \ \frac{\text{energy stored in the resonant circuit}}{\text{power loss in the resonant circuit}}$$

A common issue in filter design is the reduction of the passband insertion loss; the insertion loss of a BPF largely depends on the insertion loss of the single resonator (unloaded Q-factor of the resonators), and it is directly related to the resonator physical realization. In addition, the passband insertion loss is inversely related to the filter bandwidth and directly related to the filter order. Therefore, for a prescribed bandwidth, filters employing a minimum number of resonators are to be preferred. Another advantage of using a minimum number of resonators is that the sensitivity with respect to manufacturing tolerances is reduced. On the contrary the higher the filter order, the higher the sensitivity and the higher the required manufacturing accuracy.

Thus, for better selectivity in filter design advanced filtering functions, such as elliptic or quasi-elliptic functions [56], that exploit finite frequency transmission zeros, are essential to satisfy the filter requirements with a minimum number of resonators.

3.4 Identification of Resonator

Since decades at RF frequencies filters are modeled using lumped elements (inductors, capacitors) [38]. Lumped element models are based on discrete entities that are expected to give a more accurate description of the behavior of the system. Initially the Ka band filter was designed using equivalent

circuit modeling of electromechanical components and then it was modeled by employing micromachined cavity resonators. To evaluate the model the commercial software ANSYS HFSS has been used.

In Section 3.2 a simulated Q-factor of 600 has been assessed, but considering dielectric and parasitic effects the practical realization recommend to take into account only 60% of the simulated Q-factor. Therefore the required Q-factor should not be less than 700. Two types of configuration, (a) vertically stacked cavity resonators and (b) folded waveguide cavity resonators, as micromachined cavity resonators were evaluated on the basis of their Q-factor and footprint. The results of the analysis are supported by computer-based calculations. In order to satisfy the ESA's electrical requirement the preliminary design of Ka band filter was based on TE_{101} mode micromachined cavity resonators.

3.4.1 Vertically Stacked Cavity Resonators

The initial concept considered for the realization of the Ka band filter was based on micromachined cavity resonators. In order to reduce the footprint and to attain a higher Q-factor, it was planned to stacked them vertically. Fig 3.2 illustrate this concept and shows the cross sectional view of the vertically stacked cavities. Vertical integration schemes of micromachined cavity filters have been described in [57–61], the etched wafer segments or pieces were stacked vertically to form a 3D cavity and eventually this arrangement could then be termed as height-stacked micromachined topology. Fig. 3.2 shows a possible realization of a filter with three slot coupled gold plated Transverse Electric (TE_{101} mode) cavities in 500 μm thick Si wafers. In this configuration thick layers make the sidewalls, whereas thin layers form the top and bottom walls of the cavities. The calculated Q-factor is 900 at 30 GHz. The vertically stacked resonators require a layout area of 7x7 mm^2.

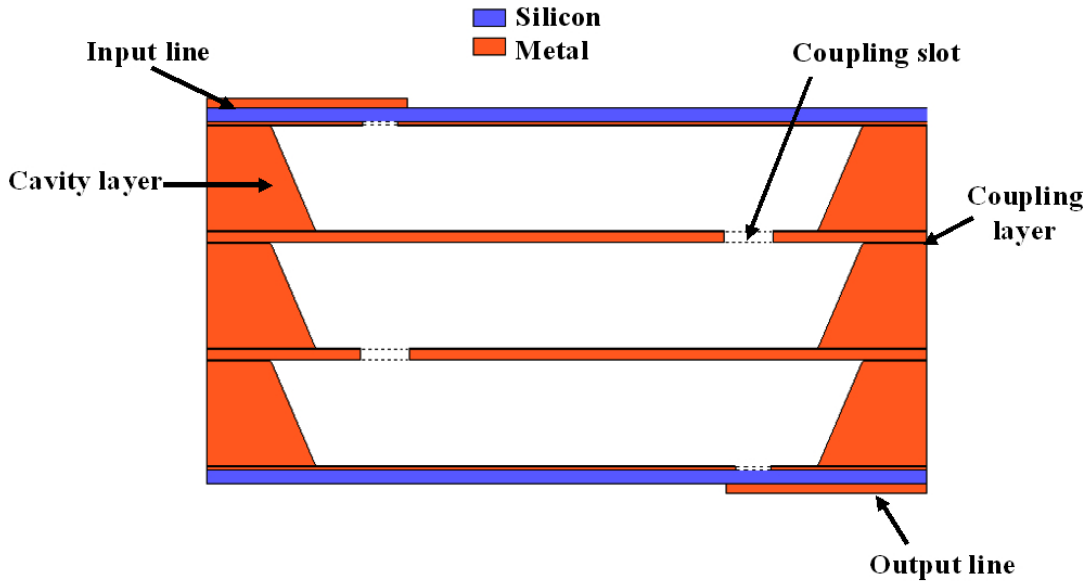


Figure 3.2: Micromachined cavity filter using vertically stacked metal-plated layers.

3.4.2 Folded Waveguide Cavity Resonator

To further minimize filter size folded-waveguide cavities were investigated. A TE_{101} mode cavity can be folded in several manners in order to obtain compact structures. A feasible way to realize a folded-waveguide cavity is to employ two stacked thick layers for a single cavity, whereas a thin layer between the two used as a "folding plane". The formation of a third order filter employing such cavities is shown in Fig 3.3. By comparing the structures presented in Fig. 3.2 Fig. 3.3, it is clear that the footprint is reduced to one half. However, in both structures input and output feeding lines are placed at the opposite ends, restraining strongly the surface mounting compatibility. A more practical structure for the Ka band filter is sketched in Fig. 3.4 it consists of four folded cavities realizing a negative cross-coupling between the first and the fourth cavity as required by the filter topology shown in Fig. 3.1.d. Both the input and output microstrip lines are on the top layer, thus allowing for an easy Surface Mount Technology (SMT) like interface. This structure occupies an area of roughly 8x8 mm^2.

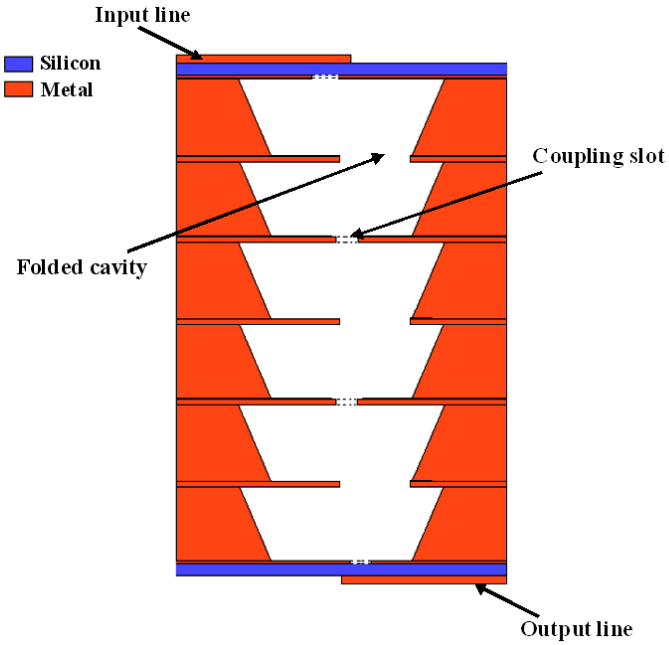


Figure 3.3: Micromachined folded-cavity filter using stacked metal-plated layers.

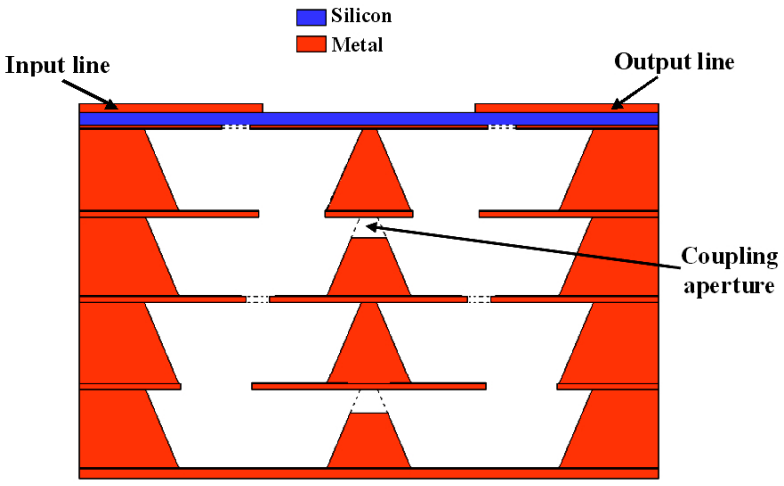


Figure 3.4: Possible structure for the Ka band filter.

3.5 HFSS Simulation of a Single Folded Waveguide Resonator

Fig. 3.5 demonstrates a TE_{101} mode resonator employed in the Ka-band filter which has a volume occupation of 8.5x3.7x2.2 mm^3 (a x l x b). It is a one-time folded rectangular waveguide cavity whose width (a) and length (l) determines the resonant frequency and whose height (b) determines the Q-factor. HFSS simulated Q-factor vs cavity height is given in Fig. 3.6.

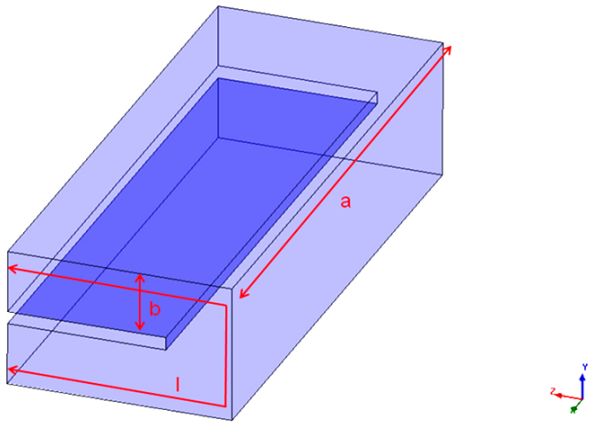


Figure 3.5: One-time folded rectangular waveguide resonant cavity at 30 GHz. Courtesy: UNIPG.

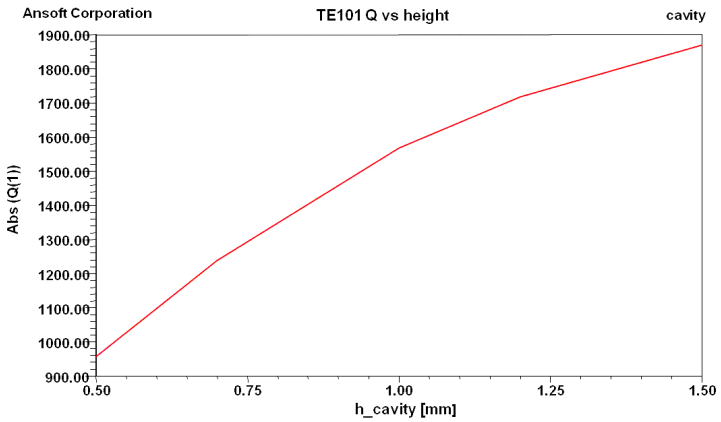


Figure 3.6: HFSS simulated Q-factor vs. height of one-time folded rectangular waveguide resonant cavity at 30 GHz. Courtesy: UNIPG.

Fig. 3.5 demonstrates a TE_{101} mode resonator employed in the Ka-band filter which has a volume occupation of 8.5x3.7x2.2 mm^3 (a x l x b). It is a one-time folded rectangular waveguide cavity whose width (a) and length (l) determines the resonant frequency and whose height (b) determines the Q-factor. HFSS simulated Q-factor vs cavity height is given in Fig. 3.6. Since most likely the actual measured Q-factor will be roughly 60% of the simulated Q-factor, in order to obtain an actual Q-factor above 600, a resonator with a simulated Q-factor above 1000 should be designed. Considering that FBK can process silicon layers having 0.2 mm or 0.5 mm or 1 mm heights, a cavity height of 1 mm was proposed, whose estimated Q-factor was roughly 1500 at 30 GHz. Gold was selected as conductive material having a thickness more than 1.5μm (i.e. 3 times the gold skin-depth at 30 GHz) in order to avoid undesired ohmic loss. Spurious performance was also evaluated for the single resonator as shown in Fig. 3.5.

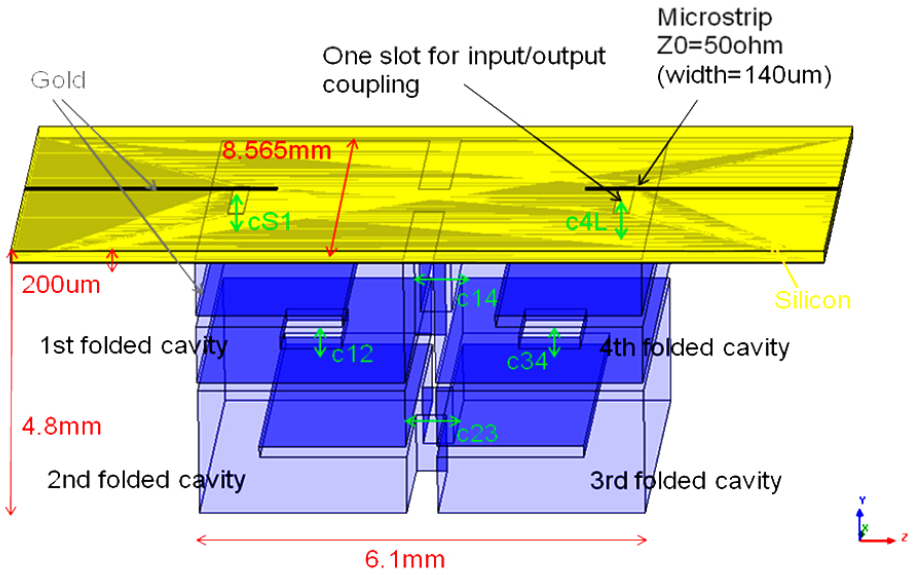


Figure 3.7: HFSS design of Ka-band 4^{th} order filter (perspective view). Courtesy: UNIPG.

3.6 Preliminary Design Based on TE_{101} Mode Cavity

A perspective 3D model of the preliminary 4^{th} order Ka-band filter along with openings on the four cavities for direct-couplings (cS1, c12, c23, c34, c4L) and cross-coupling (c14) is depicted in Fig. 3.7.

In this design the input coupling is realized by means of a slot in the first layer. The EM field of the microstrip feed line can go throughout the slot and excites the fundamental cavity mode by magnetic coupling. The given dimensions of the filter presented in Fig. 3.7 are (8.565 x 6.1 x 4.8 mm^3) while the broadband filter simulation is shown in Fig. 3.8.

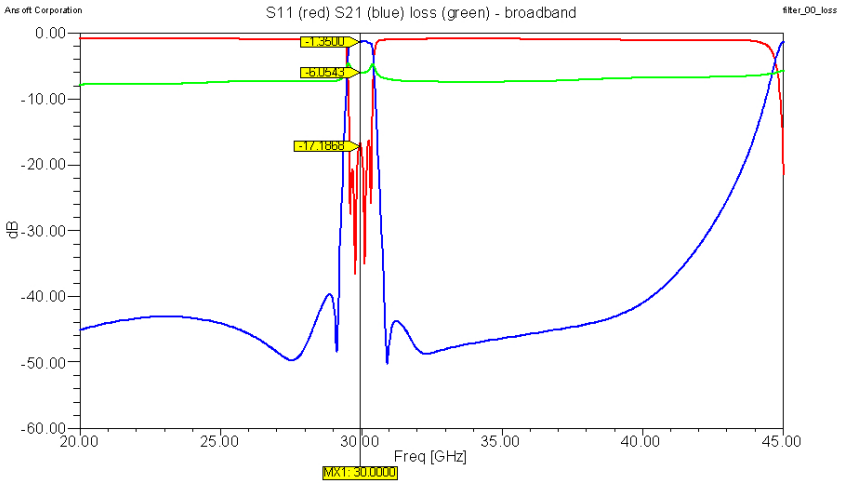


Figure 3.8: Broadband HFSS simulation of Ka-band 4^{th} order filter. Courtesy: UNIPG.

The simulation reveals the presence of a spurious input-to-output coupling: This coupling generates an additional pair of symmetric transmission zeros, and it limits the maximum out-of-band rejection (about 45dB rejection is provided in the stop-band). Also of importance is the fact that the limitation of the out-of-band rejection is mainly due to a coupling occurring throughout radiation between the feeding microstrip lines. On the other hand, the additional transmission zero pair is mainly due to a spurious coupling mechanism occurring within the filter structure (probably between the upper half-cavities).

The results derived from these simulation fulfil all ESA electrical requirements mentioned in Table 3.1. In order to assess the manufacturability of the structure with the proposed micromachining technology an initial sensitivity analysis was carried out taking into account the FBK manufacturing tolerances. Considering a variation of ± 3% in silicon layer thickness resulted in the variation of ±30 μm of all the layer thicknesses (nominal layer thickness of 1mm), a frequency shift of ± 115 MHz was also observed. These changes occurred due to variations of the effective folded cavity lengths when the heights are changed, as illustrated in Fig. 3.9 while thicker curves presents nominal parameters.

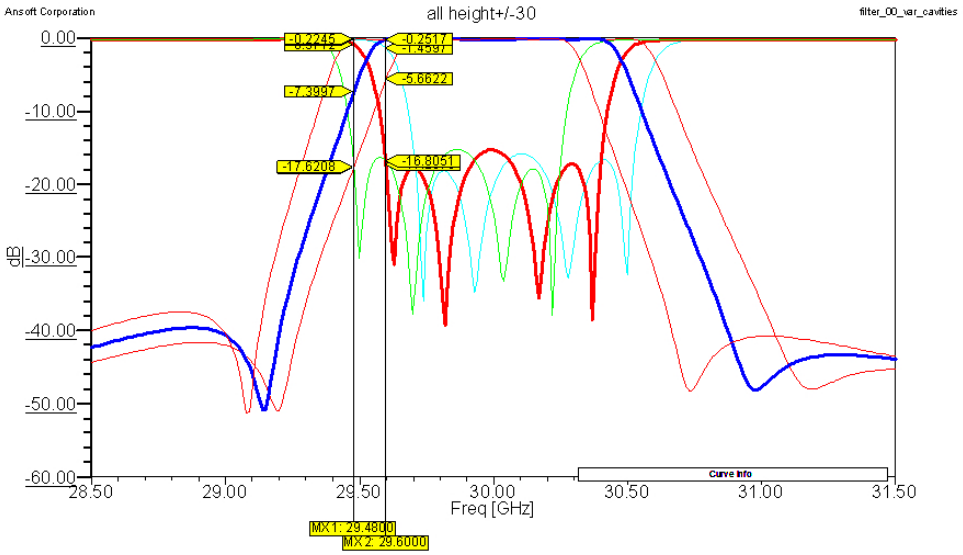


Figure 3.9: Silicon layer synchronous variations (±30 μm) of Ka-band 4^{th} order filter. Courtesy: UNIPG.

However, this variation put no effect on the 12 and 34 couplings. Such results imply the necessity of reducing the silicon layer thickness variation to 1% or increasing the filter response out-of-band rejection margin.

Fig. 3.10 and Fig. 3.11 presents the effects of etching tolerances on filter response estimated for the 12 and 34 openings and for the input and output slots. Of particular importance is that an etching tolerance of ±5 μm did

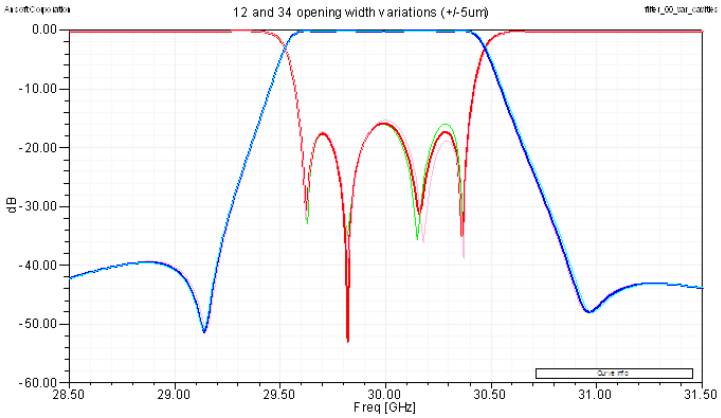


Figure 3.10: Both 12 and 34 openings variations (both width and length ± 5 μm) of Ka band 4th order filter. Courtesy: UNIPG.

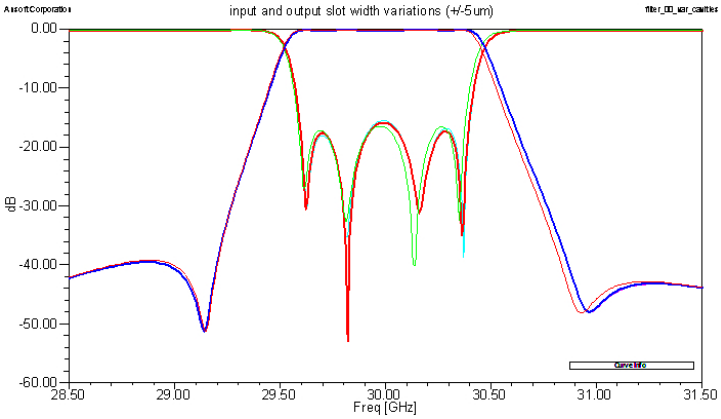


Figure 3.11: Both input and output slot variations (width ± 5 μm) of Ka band 4^{th} order filter. Courtesy: UNIPG.

not produce any significant effect on the 12 and 34 coupling openings (length and width) and on the input/output slots.

The preliminary Ka band filter design also includes a tolerance analysis considering the actual inclined cavity walls due to TMAH etching. Moreover, to verify the simulation accuracy, behaviour over temperature and robustness of the design investigations were carried out to evaluate the following*colon*

- Filter response as function of temperature.
- Filter sensitivity with respect to asynchronous variations of the cavity

parameters that includes layer height, etching angle, membrane thickness.

- Filter sensitivity with respect to assembly misalignments of the silicon layers ($\pm 5\mu$m).
- Sensitivity analysis based on the new technological concept based on 1.5mm thick Si wafers: in particular sensitivity with respect to cavity height, diaphragm thickness, dimensions of coupling apertures.

3.7 Optimization of TE_{101} Mode Cavity

The resonator is the critical component of a microwave filter and the Q -factor is determined by its dimensions. A TE_{101} mode one time folded cavity resonator, as proposed in the preliminary design, along with its variables/parameters is illustrated in Fig. 3.12, where also cavity width (w_c), cavity length (l_c), cavity wafer height (h_w), membrane height (h_m) - thickness of the metalized silicon membrane inside the cavity, width of the folding opening (d_f), and TMHA etching angle (α) are indicated.

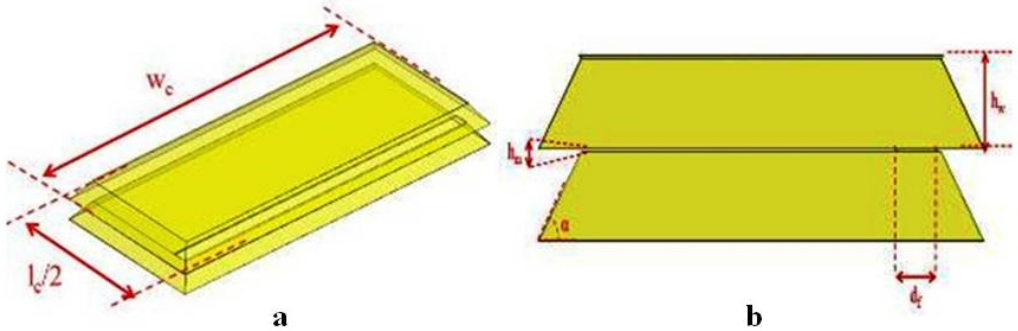


Figure 3.12: One-time folded rectangular waveguide resonant cavity at 30 GHz. (a) Prospective view and (b) Section view. Courtesy: UNIPG.

The optimization process includes a tolerance analysis in order to assess the variability introduced by technology. The above mentioned cavity is

realized on 500 μm thick silicon and simulated spurious modes and Q-factor were calculated for different values of the folding opening width (d_f). From the analysis $d_f = 350$ showed to be a good trade-off between spurious mode allocation and Q-factor. The optimized dimensions of the cavity are depicted in Fig. 3.13. For these dimensions the HFSS simulation estimated a Q-factor equal to 830 for TE_{101} mode at 30 GHz.

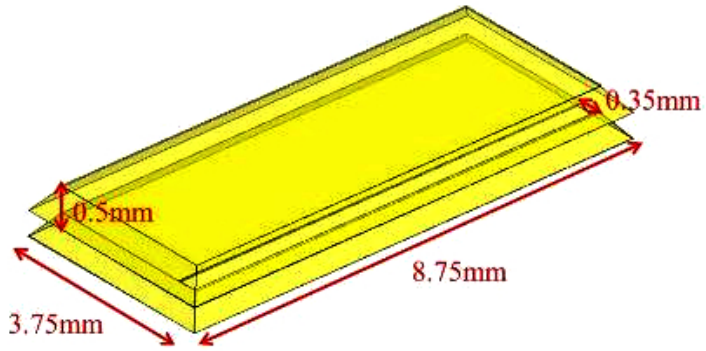


Figure 3.13: Optimized Cavity dimensions for 500 μm thick Si layer. Courtesy: UNIPG.

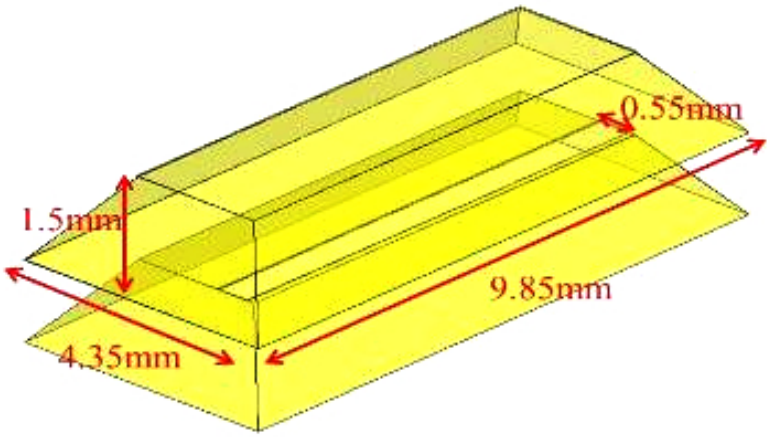


Figure 3.14: Optimized Cavity dimensions for 1500μm thick Si layer. Courtesy: UNIPG.

For 1500 μm thick Silicon the optimized critical parameters are shown in Fig. 3.14. The HFSS simulated TE_{101} mode Q-factor at 30 GHz is 1247. In both cases gold thickness of 2μm, gold roughness of 250 nm and metalized membrane height (h_m) of 20 μm were considered.

Table 3.2: **Tolerance Analysis of TE101 Mode Cavity Resonators.**

	500μm wafer			**1500 μm wafer**		
Parameters	**Expected value (μm)**	**Variation (μm)**	**Resonance frequency (MHz)**	**Expected value (μm)**	**Variation (μm)**	**Resonance frequency (MHz)**
$\mathbf{h}_w$	480	$\pm$10 (i.e. $\pm$2%)	$\pm$60 (i.e. $\pm$0.2%)		$\pm$10 (i.e. 2%)	$\pm$ 60 (i.e. $\pm$0.26%)
$\mathbf{h}_m$	20	$\pm$2.5	$\pm$50 (i.e. $\pm$0.17%)	20	$\pm$2.5	$\pm$60 (i.e. $\pm$0.2%)
$\mathbf{d}_f$	350	$\pm$2	$\pm$15 (i.e. $\pm$0.05%)	350	$\pm$2	$\pm$20 (i.e. $\pm$0.07%)
α		$\pm$1	$\pm$60 (i.e. $\pm$0.2%)		$\pm$1	$\pm$150 (i.e. $\pm$0.5%)
Layer mis-alignment		$\pm$5	$\pm$50 (i.e. $\pm$0.17%)		$\pm$15	$\pm$50 (i.e. $\pm$0.17%)

3.8 Tolerance Analysis for the TE_{101} Mode Cavity

A tolerance analysis was performed to determine the sensitivity of the filter frequency response to random variations in the structural dimensions. After the optimization process the tolerance analysis was carried out first considering 500 μm and then 1500 μm thick silicon to evaluate the resonance frequency as a function of the variation of:(a) Wafer cavity height (h_w), (b) Membrane height (h_m), (c) Width of the folding opening (d_f),(d) Etching angle (α), (e) Layer misalignment. Results are reported in Table 3.2. As expected the structure with 1500 μm thick Si wafers is even more sensitive to manufacturing tolerances.

3.9 Filter Sensitivity to Temperature Variation and Monte Carlo Analysis

The sensitivity to temperature variations has been evaluated next: considering an operating temperature range of -10°C to 75°C, a Si CTE of 2.5x10^{-6}

K-1, and a maximum resonator length of 10mm, the maximum variation in length 2.5 μm. Such a variation can be neglected in the Ka band design.

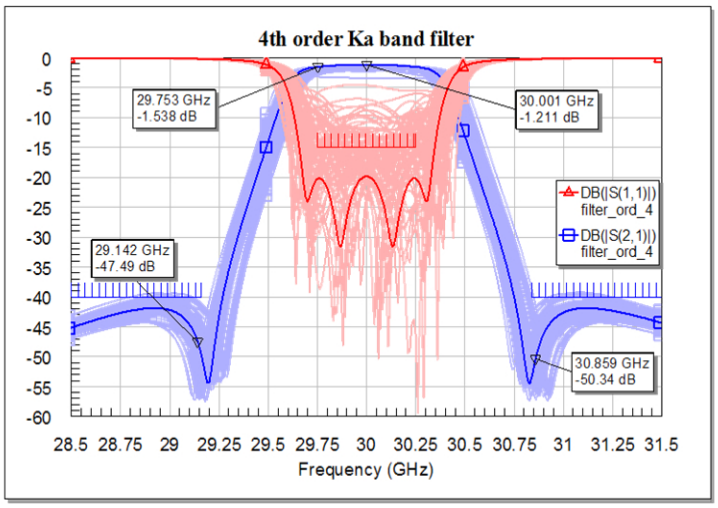


Figure 3.15: Monte Carlo analysis on the 500 μm thick Si design for a maximum resonant frequency variation of ± 60 MHz. 15% yield has been obtained. Courtesy: UNIPG.

Finally a Monte Carlo analysis was performed on the Ka band filter circuital model resonators to get an estimate of the robustness. Maximum resonant frequency variations of ± 60 MHz and ± 150 MHz were considered for the 500 μm and 1500 μm thick designs respectively. As shown in Fig. 3.15 and Fig. 3.16 both designs do not seem to be robust enough: yields of 15% and 1.5% were found for the 500 μm and 1500 μm thick designs respectively.

These results provided by tolerance and Monte Carlo analysis were not promising. The Ka band 4^{th} order filter yield was limited by the asynchronous combined manufacturing and assembly tolerances of the single resonators. The use of 1500 μ thick layers, despite the advantages of higher Q (> 1200), does not allow obtaining an acceptable filter yield ($< 2\%$). Even the use of 500 μm thick layer does not provides acceptable yield. Monte Carlo based tolerance analyses of the filters reveal that the most critical tolerances are :

- **Etching angle variation** (α) - It produces variation of all resonator

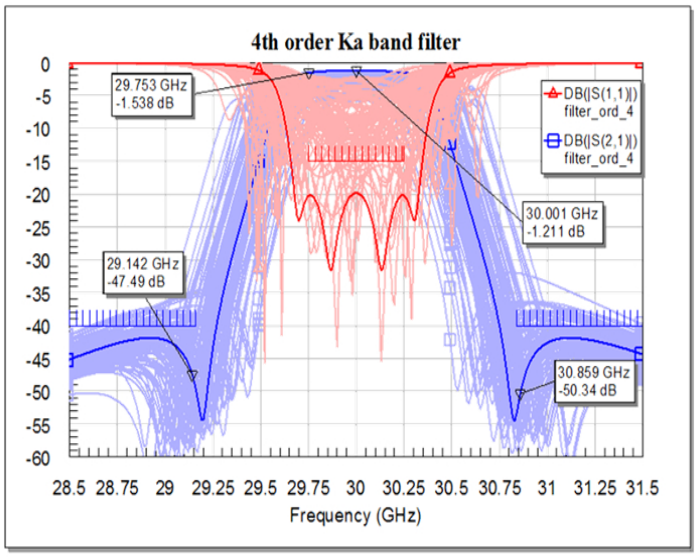


Figure 3.16: Monte Carlo analysis on the 1500 μm thick Si design for a maximum resonant frequency variation of $\pm$150 MHz. 1.5% yield has been obtained. Courtesy: UNIPG.

footprint dimensions (the higher the layer, the higher the footprint variations).

- **Wafer height variation (h_w)** - It produces variation of effective folded cavity length (the cavity is folded, therefore also the height influences the effective length).
- **Membrane height variation (h_m)** - The same concept of wafer height variation.

All these fabrication tolerances cannot be reduced easily. The etching angle variation depends strongly on the etching parameters and the status of the silicon, i.e. the process history and the defects of the silicon. Wafer height variations depend on the manufacturing accuracy of the wafer. In principle a selection can be done to reduce this tolerance but at a much higher cost of the single wafer. Finally the membrane variation depends on the fabrication tolerance. In principle very tight tolerances could be obtained with chemical or electrochemical etch-stop techniques but these techniques are only

applicable to very thin membranes and at the expense of a more complex process or a complicated etching setup. These difficulties lead towards the investigation of TEM mode resonator as an alternative to the cavity based resonators.

3.10 New Proposed Ka Band Filter Design Based on TEM Resonators

This section describes the steps that lead towards the choice of TEM mode cavity resonators. The preliminary design of a Ka filter based on TE_{101} cavity resonator didn't show enough yield and robustness against fabrication process variations. To overcome such problems a new design based on TEM mode resonators was developed for the Ka band filter. The TEM mode resonators (as depicted in Fig. 3.17) allows shifting up in frequency the spurious modes as well as to reduce the filter sensitivity to the manufacturing process. The two main advantages of TEM mode resonators essentially are:

- The fundamental mode of a short-circuited $\lambda/2$ TEM mode resonator has 180° variation along the resonator length: thus, the first higher order mode is at $2 \cdot f_0$ (λTEM mode).
- Theoretically the resonant frequency of a short-circuited $\lambda/2$ TEM mode resonator depends only on the resonator length. Thus, the number of critical geometrical parameters respect to resonant frequency variation can be minimized in the design.

Further simulations were carried out to evaluate the Q-factor and spurious free modes at higher frequencies. The $\lambda/2$ TEM mode resonator sizes are at most the same as those of a TE_{101} mode resonator. Also $\lambda/2$ TEM resonator offers acceptable Q (i.e. > 600). A perspective view of TEM mode resonator is presented in Fig. 3.18. The simulated results for Q and higher spurious free

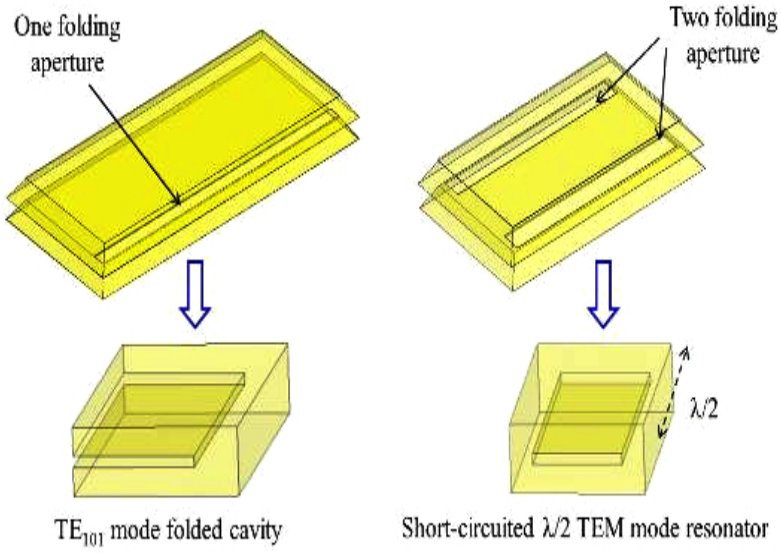


Figure 3.17: Sketch on possible implementation of TEM mode resonators in micromachining technology. Courtesy: UNIPG.

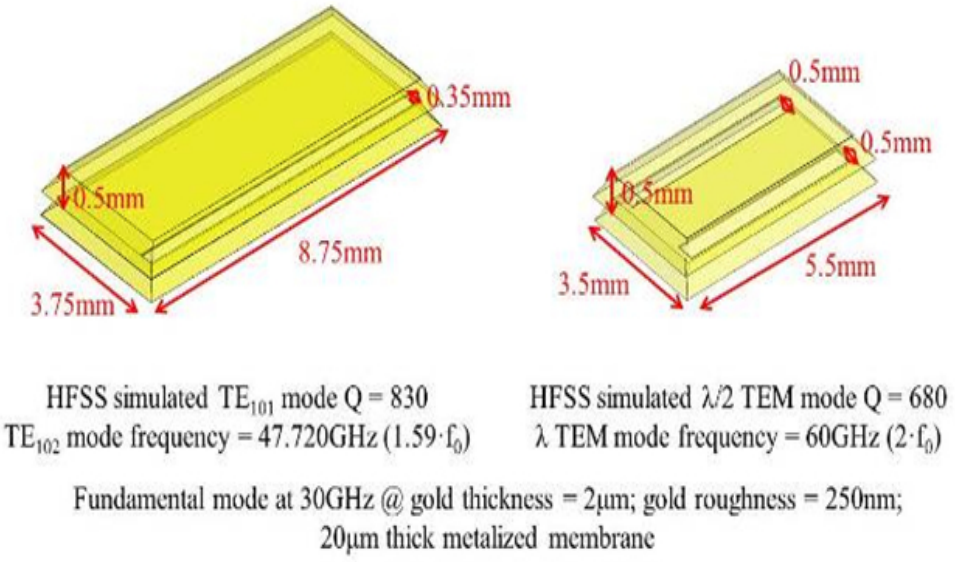


Figure 3.18: Comparison between simulated performance of TE and TEM mode resonators. Courtesy: UNIPG.

modes for TE_{101} and TEM mode resonators are shown on Fig. 3.18. Their analysis shows the following advantages associated with $\lambda/2$ short-circuited TEM mode resonator.

- Higher spurious free range (up to $2f_0$).
- Acceptable Q (value comparable to that obtained in TE_{101} mode case). Thinner folding opening reduces Q in TE_{101} mode folded cavity.
- Lower footprint dimensions than TE_{101} mode case.

The promising results of $\lambda/2$ short-circuited TEM mode resonator (shown in Fig. 3.18) paved the way towards the optimization of TEM mode cavity resonator.

3.11 Optimization of TEM Mode Cavity

This section describes the steps that lead towards the choice of TEM mode cavity resonators. Like in Section 3.7 the resonator dimensions were optimized first considering 500 μm and then 1500 μm thick silicon wafers. The most relevant parameters are defined in Fig. 3.19.

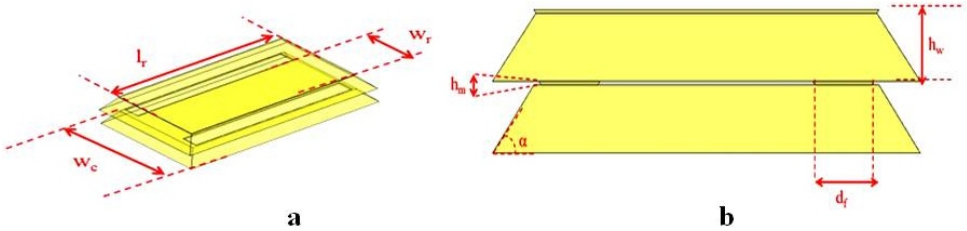


Figure 3.19: TEM mode cavity parameters definition. Courtesy: UNIPG.

For a cavity made out of 500 μm thick silicon the Q-factor was calculated considering different values of:(a) membrane height (hm), (b) resonator width (good trade-off between Q factor and cavity dimensions).

3.12 Tolerance Analysis of the TEM Mode Cavity

Since filters will be manufactured by employing silicon micromachining allowable manufacturing tolerances to the filter dimensions have to be considered in the simulation. Like in the case of the TE_{101} mode cavity resonator in Section 3.7 the tolerance analysis of the TEM mode cavity to resonator was performed for 500 μm thick Si wafers to evaluate the resonance frequencies as a function of the variation of: **(a)**Wafer cavity height (h_w), **(b)**Membrane height (h_m), **(c)**Width of the folding opening (d_f, **(d)** Length of the folding opening (l_f), **(e)**Etching angle (α), **(f)**Layer misalignment. Results are shown in Table 3.3

Table 3.3: **Tolerance Analysis of TEM Mode Cavity Resonators**.

Parameters	**Expected value (μm)**	**Variation (μm)**	**Resonance frequency (MHz)**
$\mathbf{h}_w$	480	$\pm$10 (i.e. $\pm$2%)	$\pm$30 (i.e. $\pm$0.1%)
$\mathbf{h}_m$	20	$\pm$2.5	$\pm$10 (i.e. $\pm$0.033%)
$\mathbf{d}_f$	500	$\pm$2	Negligible effect
$\mathbf{l}_f$	547	$\pm$2	$\pm$10 (i.e. $\pm$0.033%)
α		$\pm$1	$\pm$40 (i.e. $\pm$0.13%)
Layer mis-alignment		$\pm$5	$\pm$50 (i.e. $\pm$0.17%)

3.13 Sensitivity to Temperature Variation and Monte Carlo Analysis

The objective of this simulation was to evaluate the effect of temperature variation on the resonance frequency of a filter for an operating temperature

range from -10°C to 75°C a Si CTE of 2.5 x 10^{-6} x K^{-1}, maximum resonator length of 5 mm, and the maximum variation of length 1.25μm were considered. Such a variation produced negligible effect on Ka band filter design based on TEM mode resonators.

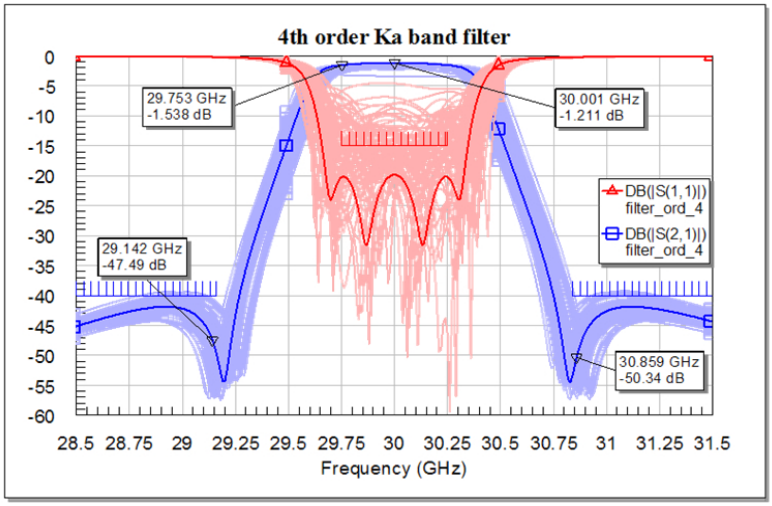


Figure 3.20: Monte Carlo analysis on the 500 μm thick Si design for a maximum resonant frequency variation of ±40 MHz. Courtesy: UNIPG.

Finally Monte Carlo analysis was performed on the Ka band filter circuital model resonators to get an idea of the filter robustness with respect to the manufacturing tolerances. With the filter realized on 500 μm thick Si wafers a maximum resonant frequency variation of ±40 MHz as shown in Fig. 3.20 and 35% yield were obtained. Another advantage of this design shown by the Monte Carlo analysis is the reduction in the number of critical parameters as in case of TE_{101} mode folded resonator described in Section 3.7.

The TEM mode resonator successfully qualified in the Monte Carlo analysis and are also less sensitive against temperature variations. Therefore, the new preliminary Ka band 4^{th} order filter is based on $\lambda/2$ TEM resonator realized on 500 μm thick silicon wafers.

3.14 4^{th} order Ka Filter Based on TEM Mode Resonators

A 4^{th} order Ka band filter design based on TEM mode resonators is presented in Fig. 3.21 while different types of its coupling mechanism are shown in Fig. 3.22 (a,b,c). Initially filters were simulated considering ideal vertical walls (Fig. 3.23- Fig. 3.24), and then re-optimized accounting for the actual micromachining constraints (Fig. 3.25- Fig. 3.27)

The HFSS simulated IL flatness is 0.35 dB as illustrated in Fig. 3.23(c) whereas the required IL is 0.3. The IL flatness can be improved by adopting two alternative approaches:

- First by increasing the wafer thickness to 1000 or 1500 μm and restricting the etching angle tolerance "α" to $\pm 1°$. The resulted IL flatness (i.e. IL = 0.23) is sketched in FiFig. 3.24.a. The increase in height of wafers ultimately increases the cavity depth thus improving the overall Q of resonator. A HFSS simulation shows Q-factor of 900.

- Second by increasing the Q of the internal two resonators (2^{nd} and 3^{rd} up to 750) by increasing only the resonator width (w_r and folding opening (d_f). The resulted IL flatness (i.e. IL = 0.29) is sketched in Fig. 3.24(b).

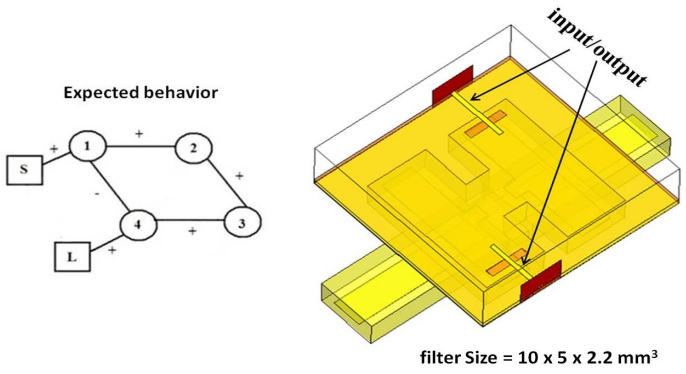


Figure 3.21: Sketch of the 4^{th} order filter model in HFSS. Courtesy: UNIPG.

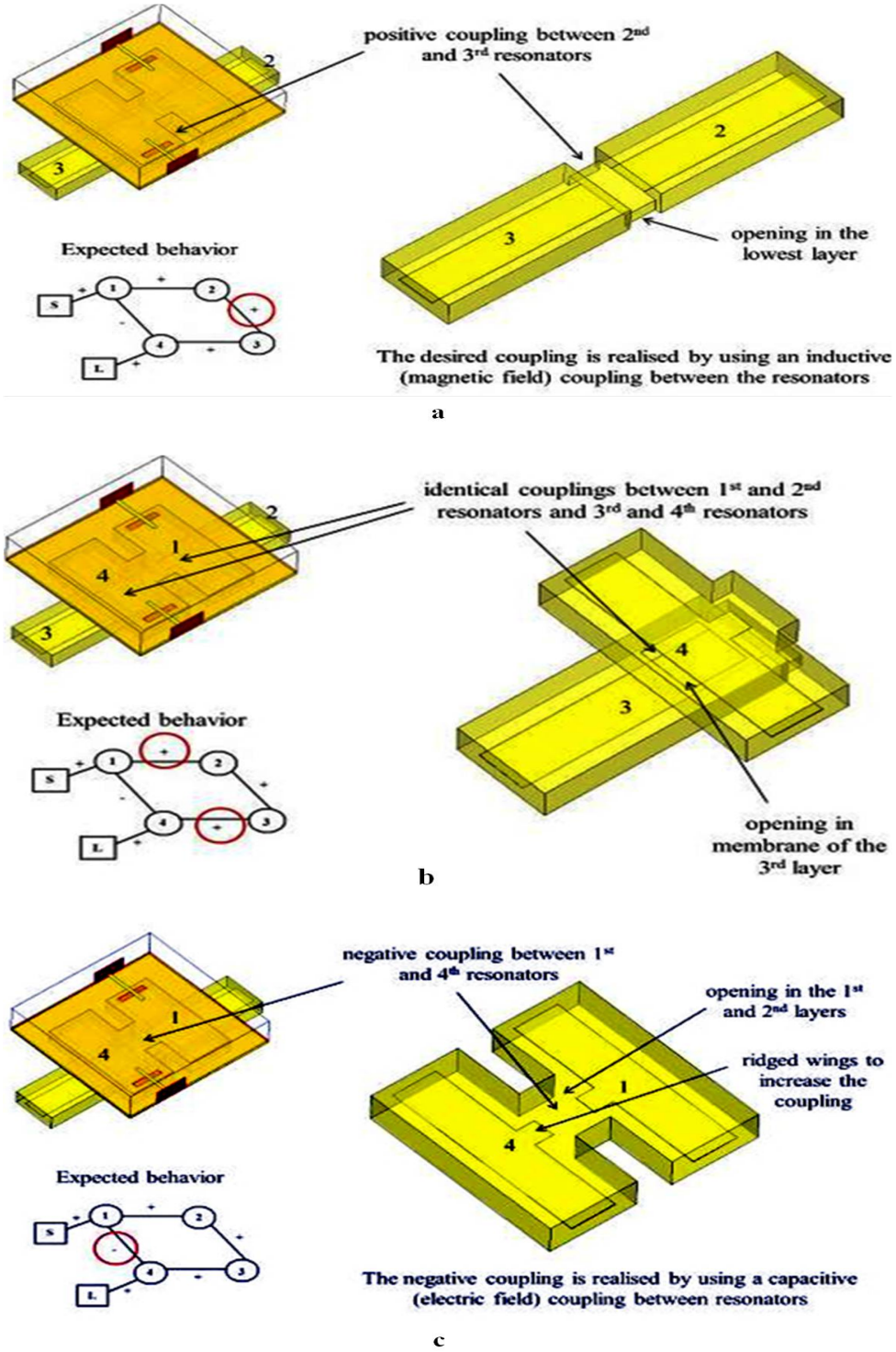
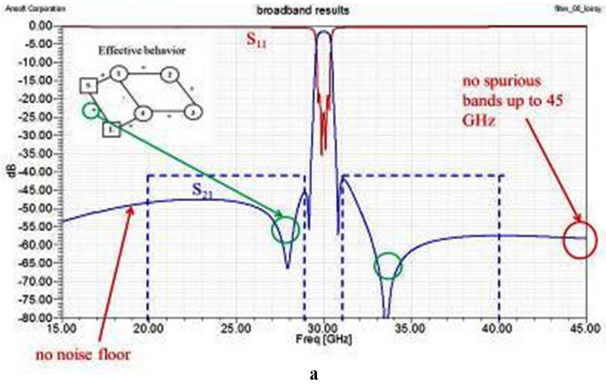
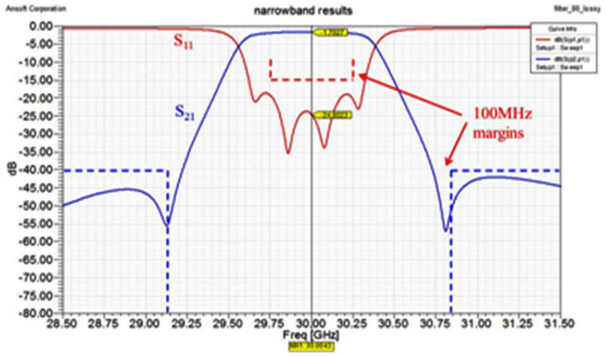


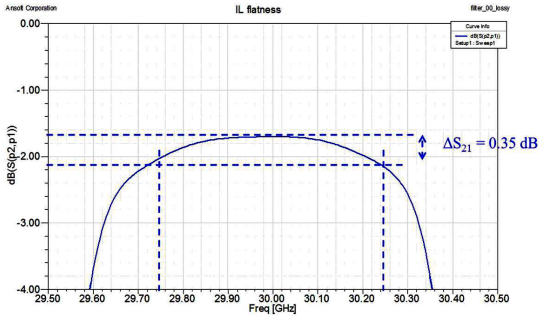
Figure 3.22: Realization of the different couplings: (a) 2 - 3, 1 - 2 and (b) 3 - 4, and (c) 1 - 4. Courtesy: UNIPG.



a

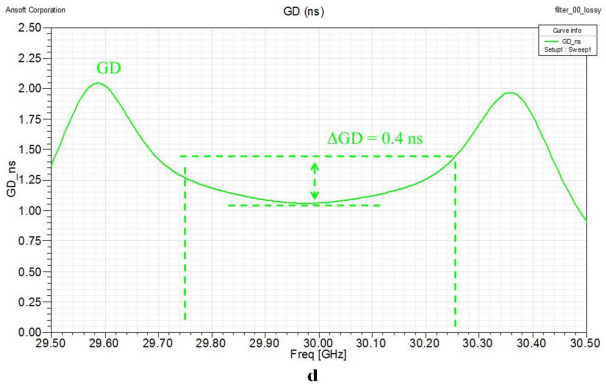


b



IL flatness goal is 0.3dB in 29.75-30.25GHz
→ The ΔIL results of 0.35 dB can be increased in final filter designs (WP401)

c



d

Figure 3.23: Performance of the 4^{th} order filter. (a) Wide-band results, (b) Narrow-band response, (c) Insertion Loss flatness and (d) Group Delay. Courtesy: UNIPG.

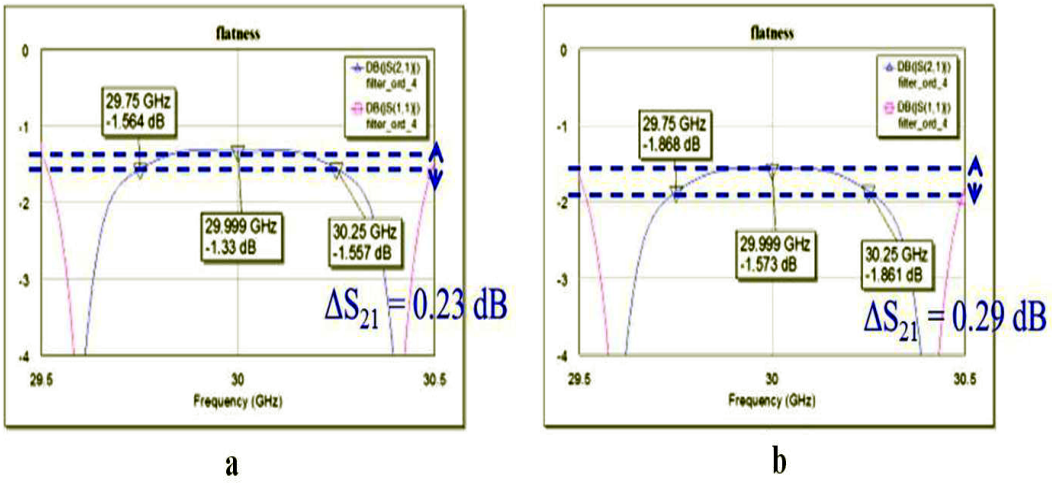


Figure 3.24: Possible improvements of the IL flatness: (a) increasing the wafer thickness or (b) the resonator width and folding opening. Courtesy: UNIPG.

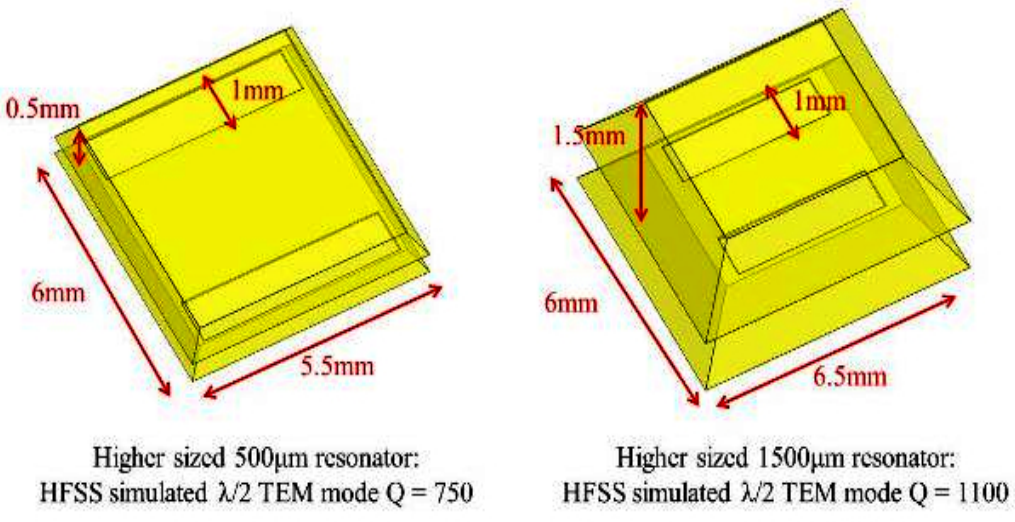


Figure 3.25: Sketch comparing the dimensions and simulated Q factors for the 500 μm and 1500 μm thick wafers. Courtesy: UNIPG.

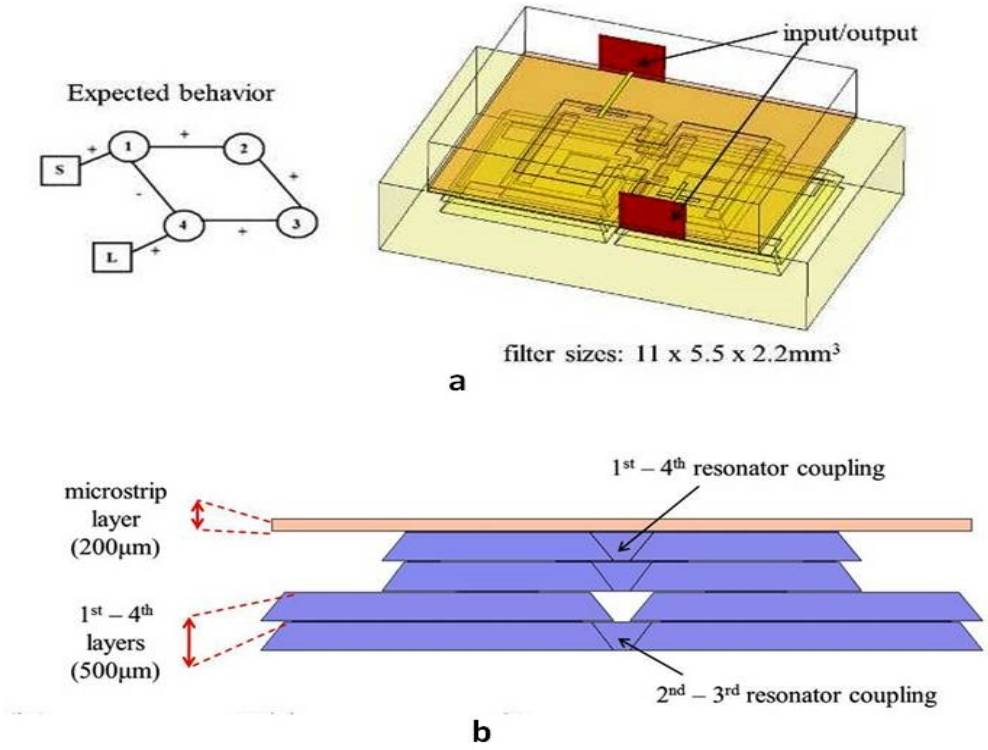


Figure 3.26: Sketch of the 4^{th} order filter: (a) model in HFSS on 500 μm thick Si layers accounting for the non-vertical cavity walls and (b) side view. Courtesy: UNIPG.

Comparison of the dimensions and simulated Q-factors for the 500 μm and 1500 μm thick wafers is presented in Fig. 3.25

The layout and expected performance of the 4^{th} order pseudo-elliptic filter realized by stacking four 500 μm thick Si wafers is depicted in Fig. 3.26and Fig. 3.27. All of the technological constraints of FBK and the material loss have been taken into account. The simulated $\lambda/2$ TEM mode Q factor is 750.

Even if the simulated properties of the final design presented in Fig. 3.26 are compatible with the ESA specifications presented in Table 3.1 it was decided to make a technology development run before trying to fabricate this complex structure. This would allow to verify not only the process architecture and the assembly but also the fabrication tolerances and in general the resonator design. To keep the effort and complexity as low as possible some

simple but significative test structures shown in Fig. 3.28 - Fig. 3.31 were selected. Once fabricated these structures were measured and compared with the simulations, allowing to verify the basic elements of the filter design.

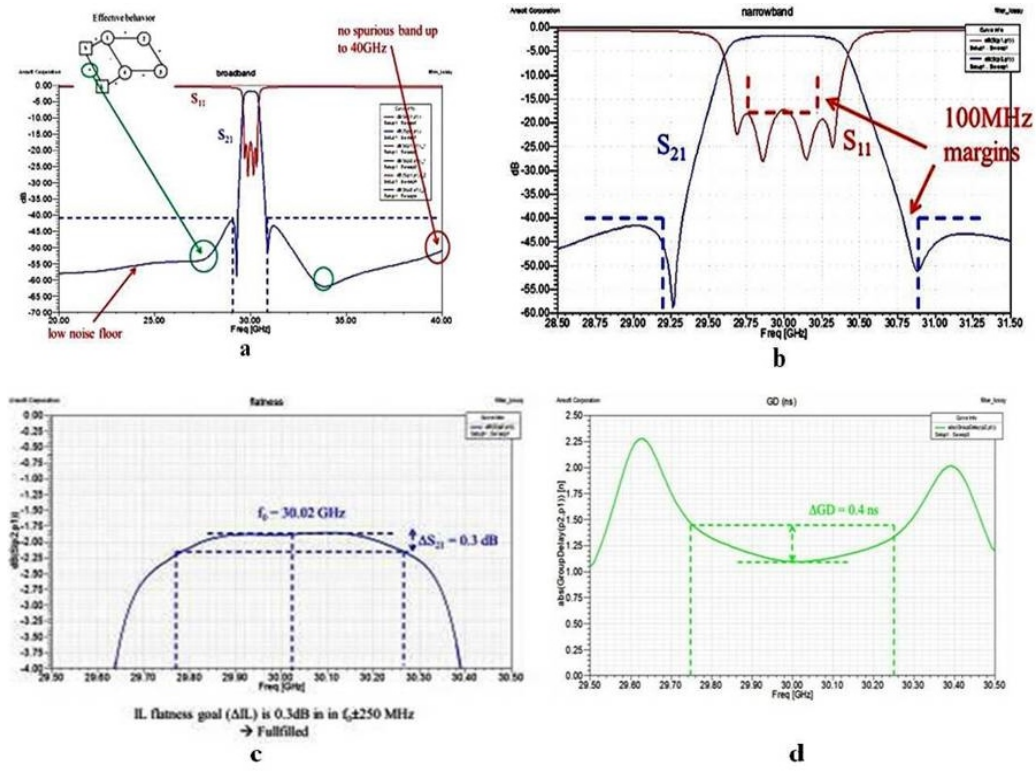


Figure 3.27: Performance of the 4^{th} order filter. (a) wide band results, (b) narrow band response, (c) Insertion Loss flatness, and (d) Group Delay. Courtesy: UNIPG.

3.15 Ka Band Filter Test Structures

This section shows four types of test structure, all based on 500 μm thick Si wafers for convenience. These structures were designed to allow a fabrication test run and to test the basic elements of the filter design. Among these the most crucial ones are the resonator elements itself, two of them are considered, and simple 2 pole filters that allow to test the folded resonator designs.

Ka 01: 1-port Resonator The structure in Fig. 3.28 was designed and fabricated for reflection loss (S11) measurement and Q estimation.

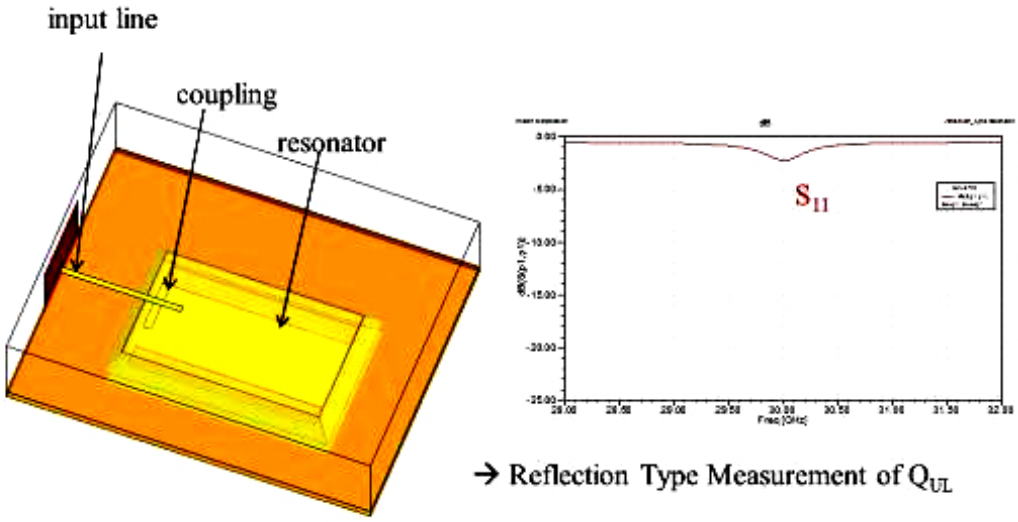


Figure 3.28: Layout and expected performance of test structure Ka 01: 1 port resonator. Courtesy: UNIPG.

Ka 02: 2-port Resonator (S21 measurement for Q estimation)

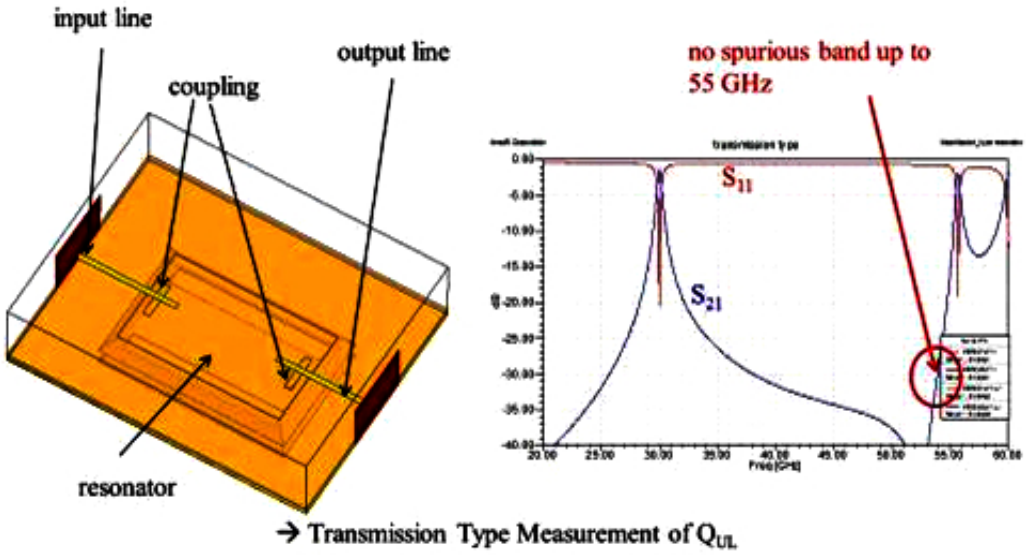


Figure 3.29: Layout and expected performance of test structure Ka 02:2 port resonator. Courtesy: UNIPG.

Ka 03: 2^{nd} order Filter A (Test of negative cross-coupling)

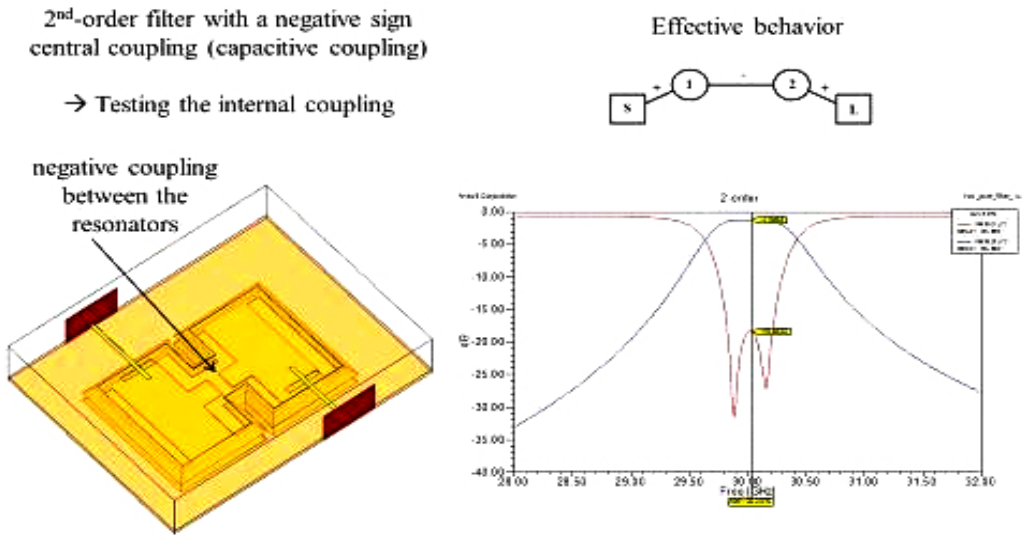


Figure 3.30: Layout and expected performance of test structure Ka 03: 2^{nd} order Filter (A). Courtesy: UNIPG.

Ka 04: 2^{nd} order Filter B (Test of positive cross-coupling)

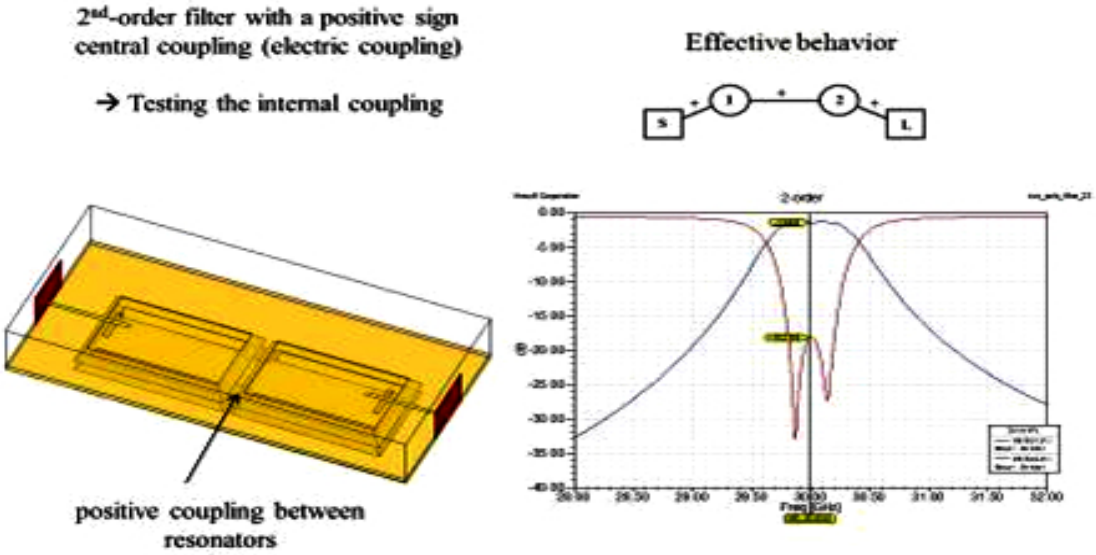


Figure 3.31: Layout and expected performance of test structure Ka 04: 2^{nd} order Filter (B). Courtesy: UNIPG.

3.16 Fabrication of Ka Band Filter

This section describes the fabrication process of the prototype structures mentioned in Section 3.15 for the Ka band filter. The main goal is to identify and optimize a viable technology to fabricate these filters. The activity is performed in two steps fabrication of the individual parts and assembly of the prototype. Before heading for the fabrication process it is important to describe briefly the evolution of technological concept for Ka band filter.

3.16.1 Evolution of Technological Concept for Ka Band Filter

The simplified cross section of the technology concept for Ka band filter initially developed is summarized in Fig. 3.32. The figure shows only half of the structure, which is symmetrical with respect to vertical axis. In this concept the device is formed by 6 wafers, which are bonded together by gold to gold thermocompression bonding. Top and bottom plates are formed by 200 μm thick high resistive <100> p type Si wafers. While the middle plates which hosts the TE_{101} mode cavities are made by standard 500 μm thick <100> p type high resistive (HR) Si wafers.

The studies performed on the HFSS model of the above structure that include the fabrication tolerances showed poor robustness of the design and the forecasted yield was too low. Therefore a new approach was adopted for the filter design but the technological concept with little modification remained the same. The modified preliminary design of 4^{th} order Ka band filter is based on a TEM mode resonator and the technological concept is summed up in the Fig. 3.33.

Fig. 3.33 represent the cross sectional view of the structure shown in Fig. 3.26. The figure shows only half of the structure, which is symmetrical with respect to the vertical axis. The filter is Fig. 3.13build up by 6 Si layers, which are vertically stacked and bonded by metal to metal ther-

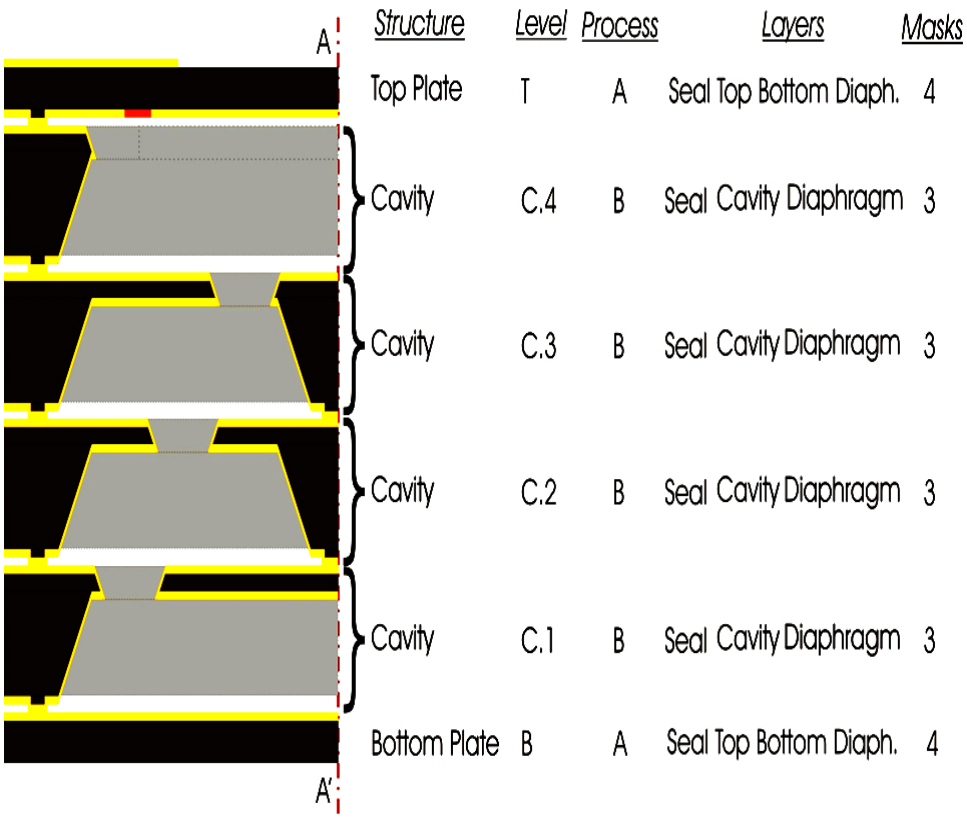


Figure 3.32: Cross section view of the initially developed technology concept for Ka band filter based on TE_{101} resonator cavities. Only one half of the structure is shown. A-A' is the symmetry plane.

mocompression bonding. The revised version differs only in the top layer, which includes now TSVs. This incorporation of TSV in the design on one hand provides electrical connection between ground planes of the coplanar lines and internal metalized cavities and on the other hand allows both flip chip mounting and the implementation of a proper coplanar to microstrip transition which is necessary for the on-wafer/die testing of the filters. The addition of TSV's made the top layer process more complex. Three additional mask layers were used to realize the structure. For simplicity the TSVs were etched by bulk micromachining and plated internally with the same gold layer already anticipated for the bottom metallization of the top layer.

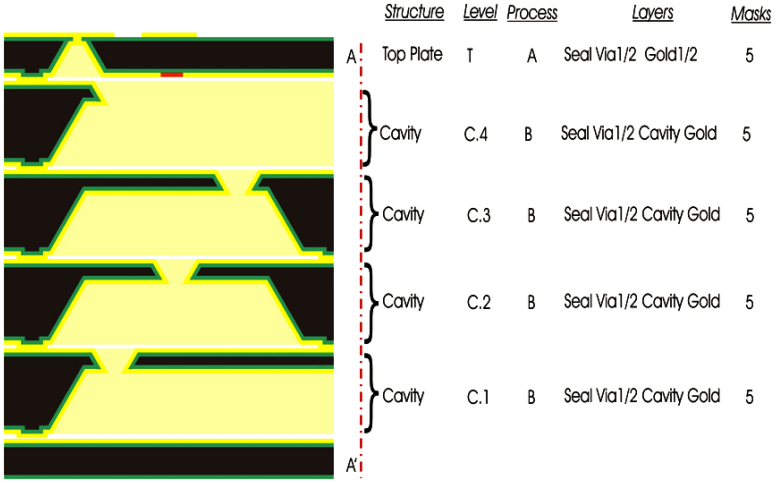


Figure 3.33: Cross section view of the preliminary design of Ka band filter based on TEM resonator cavities. Only one half of the structure is shown. A-A' is the symmetry plane.

3.16.2 Fabrication Process Description

To test the technology and the design methodology simple test structures presented in Section 3.15 were fabricated. Fig. 3.34.a and b presents the layout of Ka2 and Ka3 filters respectively. The top plate of Ka4 filter is similar to Ka2. Fig.3.35 describes the cross section view of half of the devices shown in Fig. 3.34.a and b. With respect to the complete four-pole filter these test structures have for simplicity only two middle planes to test the concept. In this

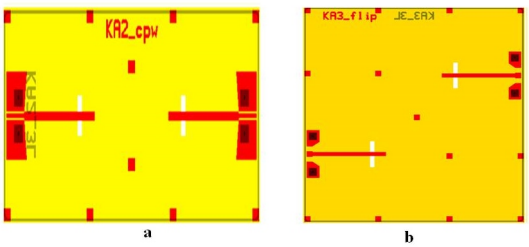


Figure 3.34: Die layout for the top plates of the filters: (a) Ka2 and (b) Ka3

case bottom layer and the two middle layers are constructed by 500 μm thick Float-Zone (FZ) Si wafers while the top layer is based on 200 μm thick

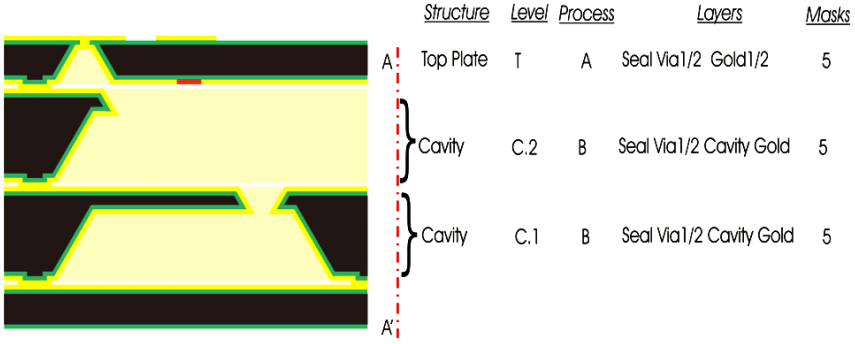


Figure 3.35: Simplified cross section view of the structures shown in Fig. 3.33. Only one half of the structure is shown and A-A' is the symmetry plane.

FZ Si wafer. In order to build the structure presented in Fig. 3.33 two types of fabrication process were developed namely the KaA Process and the KaB Process. Fig. 3.36 demonstrates the splitting of fabrication process.

- **KaA Process**: KaA process consist of 5 mask and deals with the construction of top and bottom layers of the structure.

- **KaB Process**: KaB process also consist of 4 mask and is employed to construct the cavities in middle layers of the structure.

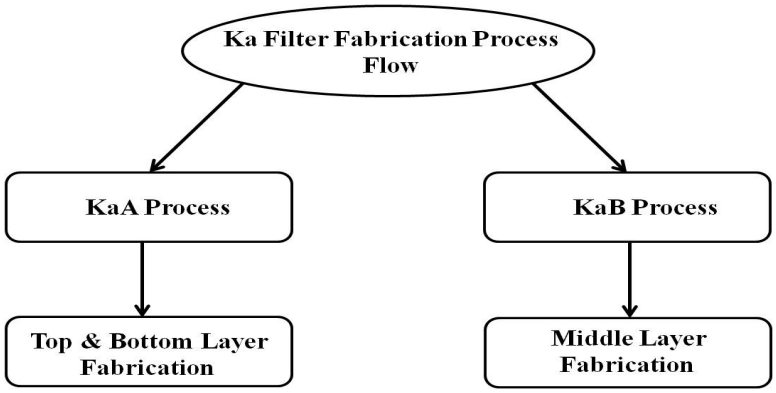


Figure 3.36: Splitting of fabrication process for Ka band filter test structures

3.17 Fabrication Process Flow of Top layer - Basic Steps for KaA Process

The KaA process is a five mask fabrication process developed to construct the top and bottom layer of the Ka band test filter. Process details are provided in **Appendix "A"** and the scheme of the process flow is sketched in Fig. 3.37.

In this process 200 μm thick, HR 5000 Ω cm, p-type, <100>, double side polished and four inch diameter silicon wafers are used as substrate. Before initiating the fabrication the process wafers were labeled with alphanumeric characters on a predetermined region of the wafer so that they can be identified correctly. To this purpose the wafers were coated with PR and labels were applied with a felt pencil soaked in acetone followed by dry etching in order to avoid any mechanical stress and damage, typically produced by mechanical scribing operations, on these very fragile wafers.

The fabrication process started with the first lithography step by defining the sealing ring on the backside of the wafer. At this point PR was spun on the wafer, exposed and developed. The pattern was then transferred to the silicon by a plasma etching with a DRIE technique and a sealing ring with a nominal step height of 2 μm was formed as shown in Fig. 3.37.a. After that 1 μm thick thermal oxide was grown employing steam oxidation at 975°C, then a 150 nm thick Si_3N_4 film was deposited by LPCVD at 775°C, followed by a Low Pressure Chemical Vapor Deposition (LPCVD) medium temperature oxide deposition from Tertraethyl orthosilicate (TEOS) at 718°C. This multilayer structure is a so called hard mask layer and was deposited on both sides of the wafer.

Second lithography defines the via openings on the wafer backside. The mask for the bottom vias was printed and dry etched to form a etch window in the dielectric layer, see Fig. 3.37.b. Anisotropic chemical etching has long

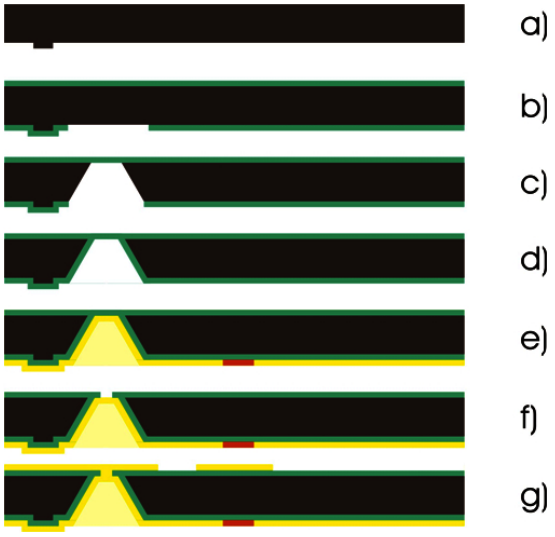


Figure 3.37: Process sequence for the top layer of the Ka band filter.

been used for producing microstructures and some typical examples are: deep cavities, membranes and cantilevers on a silicon wafer. The wet anisotropic etchant used in this work is TMAH in water [62]. As a subsequent step vias opened in the 2^{nd} lithography step were etched in a 25% (TMAH) water solution in two steps. In this way the actual etch rate could be determined in the first step which allows a precise control of the second etch step. In order to determine the precise etch rate [63] a first etch of less than 4.5 hrs was performed that produces a ~175 μm deep cavity. In a second step the cavity is deepened to the full wafer thickness with a little over etch to exposes the bottom of the front hard mask layer. Due to the small dimensions (less than 50 x 50 μm^2) the resulting membranes were sufficiently robust to tolerate the mechanical stresses during the last phases of the bulk-etch, giving a very high yield of intact membranes, see Fig. 3.37.c.

Next, the frontside of wafer was covered by PR and the TEOS layer was selectively removed from the backside of the wafer with the help of buffered hydrofluoric acid (HF). After ashing the PR the nitride layer was stripped from the backside of the wafer with phosphoric acid (H_3PO_4) at 150 °C for 30 min. During this etching the Si_3N_4 on the front side of wafer was protected

by the TEOS layer. Then the wafers were oxidized again for 385 minute in steam at 975°C in order to grow a 1 μm thick oxide layer on the sidewalls of the through silicon vias. In order to reduce the trapped oxide charge the wafers were annealed in nitrogen at 975°C for 1 hour. This completes the isolation of the silicon substrate, see Fig. 3.37.d.

In the subsequent steps the TEOS oxide layer on the wafer frontside was removed by dry etching the oxide, and then the Si_3N_4 was removed as above by hot phosphoric acid (H_3PO_4). At this point the backside of the wafer was coated with a conductive seed layer for electroplating. This layer was composed of 2.5 nm of chromium (Cr), 25 nm of gold (Au) and 2 nm of Cr, respectively. These layers were deposited in a vacuum chamber by Physical Vapor Deposition (PVD) with an e-gun without interrupting the vacuum. The first chromium layer acts as an adhesive layer on the oxide for the gold layer, which otherwise would not adhere well to the substrate. The top chromium layer is the adhesion layer for the PR, which adheres much better on an oxidized surface than on gold.

The third lithography step was done with a negative dry film resist and slots were defined on the bottom gold layer. The RF signals are inserted and extracted from the cavity through these slots as shown in Fig. 3.38.

Figure 3.38: Top view of slot defined on the negative dry film resist

A dry film resist was used because standard polymer resist puddle in the

TSVs and lead to strongly inhomogeneous resist coating, while the lamination of dry film resist was almost unaffected by the presence of the vias. After developing the dry film resist the top chrome layer was removed in the exposed areas with chromium etch, a solution of ammonium cerium nitrate $[(NH_4)_2Ce(NO_3)_6]$, acetic acid (CH_3CO_2H) and water (H_2O) known also as Balzers Chromium etchant and a 2.5 μm thick gold layer was plated from a cyanide based gold bath (Aurolyte 200) in a fountain plater from RENA. After gold plating the resist mask was wet etched with the proper solvent as well as the seed layer, which was removed with a sequence of chromium etch, gold etch and chromium etch as depicted in Fig. 3.37.e. At this stage in order to connect electrically top metalized layer with the bottom gold layer vias were needed. Therefore top via holes were defined by a fourth lithography and oxide dry etching as illustrated in Fig. 3.37.f.

The fabrication of top layer ends by depositing a second seed layer, identical to the first one, on top of the wafer. Then standard resist (AZ 1050) was span and the fifth lithography was performed to patterned the feeding lines that carry the RF signals, see Fig. 3.39, followed by the 2.5 μm of Au plating after which the seed layer was removed as above from unwanted areas as illustrated in Fig. 3.37.g. Finally the wafers were annealed at 190°C for 30 min to sinter the gold layers.

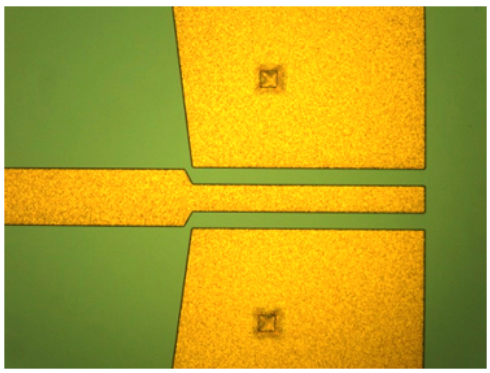


Figure 3.39: Au plated feeding line on the front side of wafer (KaA process)

3.18 Process Flow of Middle Layers (KaB Process)

To produce cavities in the middle layers of the structure sketched in Fig. 3.33 a five mask KaB process based on bulk micromachining is developed. A process flow is shown in Fig. 3.40 and details are mentioned in **Appendix "B"**. For creating deep cavities 500 μm thick, HR 5000 Ω cm, $< 100 >$, p-type, double side polished silicon wafers are used as substrate and labeling is done as in Section 3.17.

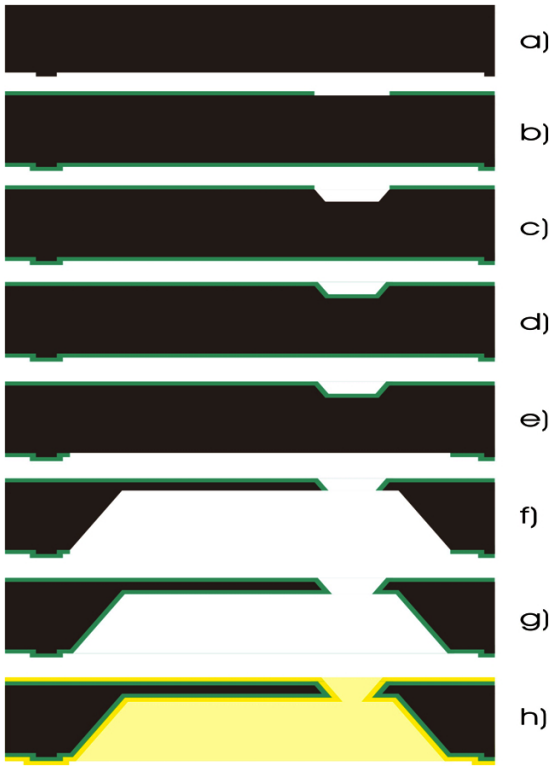


Figure 3.40: Processing sequence for the middle layers of the Ka band filter based on the simplified cross-section of Figure 3.33

As a first step a 120 nm thick thermal oxide was grown with by steam oxidation of Si at 975°C. After that for crystal orientation alignment a special mask consisting of small circular openings is used and the 1^{st} lithography is performed to define the lattice alignment marks followed by dry etching of the thin oxide layer. After ashing the PR layer a short bulk micromachining

of silicon (20 μm deep) using a 25% TMAH: water solution is carried out to produce small pyramidal cavities in each circular window opening. With the help of optical inspection the orientation of the sides of these cavities that are aligned with the crystal are measured individually. This allows the precise identification of the crystal orientation on each wafer with an error less than 0.1°, while typically the primary flat is aligned with an error of ± 0.5° but in praxis also values as high as 2.5° have been measured.

RCA cleaning was performed before the 2^{nd} lithography and then PR was deposited, exposed and developed to define the sealing ring of 50 μm width. Alcatel (DRIE) system was used to etch the sealing ring with a nominal step height of 2 μm, as shown in Fig. 3.40.a . The step height and width was later measured by optical profiler.

Subsequently a 120 nm thick thermal oxide that is grown with a steam oxidation at 975°C and prelithography cleaning was performed. Then with the help of 3^{rd} lithography the etch window for the top cavity on the wafer front side is defined by dry etching the oxide layer as presented in Fig. 3.40.b.

After removal of the PR by ashing a short bulk silicon etch with a 4:1 TMAH:water solution at 90°C is performed in order to etch a 20 μm deep cavity in the silicon, see Fig. 3.40(c). At this point a 300 nm thick thermal oxide is grown with a 60 min steam oxidation at 975°C. On top of the thermal oxide a 150 nm thick Si_3N_4 layer is deposited by LPCVD at 775°C from diclorosilane and ammonia. The Si_3N_4 is then covered with a 300 nm thick TEOS layer obtained by LPCVD at 718°C. This multilayer oxide deposition called "hard mask" is used to protect the front and backside of the wafer from the bulk silicon etching that will be used for the formation of the main cavity. The resistant layer of the hard mask is the nitride layer, which etches only at a rate of 2 nm/h. The underlying oxide layer has the function to absorb the extremely high tensile stress of the nitride film which can cause cracking in the silicon substrate, while the top oxide layer main function is

to protect the nitride layer from any mechanical scratch as any minor defect in this layer would lead to a large defects in the final device, as shown in Fig. 3.40.d.

The 4^{th} lithography defines the etch window for the main cavity by etching the hard mask layer with plasma etching on the bottom of the wafer as depicted in Fig. 3.40.e. Later the cavities were bulk etched with a 4:1 TMAH: water solution at 90°C in two steps. First step with an etching time of approximately 11 hrs results in a 455 μm deep cavity. In the second step the cavity is deepened in order to meet the smaller cavity etched from the front side, refer to Fig. 3.40.f.

Next the dielectric layers are removed with a sequence of three wet etchings: first the residues of the top oxide, followed by the removal of Si_3N_4 and the underlying oxide layer, till the bare silicon. After that the wafers are oxidized for 385 minute in steam at 975°C in order to grow a 1 μm thick oxide layer on Fig. 3.40.g all silicon surfaces. In order to reduce the trapped oxide charge the wafers are then annealed in nitrogen at 975°C for 1 h. This completes the isolation of the silicon substrate, see Fig. 3.40.g). The KaB fabrication process ends with the metallization of both side of wafers. For this purpose a seed layer consisting of a 2.5 nm thick chromium layer followed by a 25 nm thick gold layer is evaporated by Physical Vapor Deposition (PVD) on both front and back side of the wafer. Then electroplating is performed to deposit the 2.5 μm thick gold layer onto the surface of the previously deposited gold seed layer, as shown in Fig. 3.40.h. This provides a continuous coating also around the corners. Finally the wafers are annealed at 190°C for 30 min in order to sinter the gold layers.

3.19 Fabrication of Test Structures of Ka Band Filter

MEMS technology offers numerous advantages and one of them is batch fabrication of the devices. In order to realize these test structures (presented in Section 3.15) at wafer level each layer has to be fabricated individually by using one of the two processes described above. The technological concept presented in Fig. 3.33 for the 4^{th} order Ka band filter requires only one top layer and four different intermediate layers (two in the reduced test version) i.e. an individual mask set for each. While only sealing ring mask is the same for all.

3.19.1 Fabrication of Top Plate (KaA Process)

As a base substrate 200 μm thick, high resistive 5000 Ω cm, p-type, <100> wafers have been employed in the KaA process. Fig. 3.40.a shows the wafer layout for the top layer. The wafer hosts additional devices beyond the top plates of the filters. The top side of the wafer contains some structures for calibration while at the bottom right of the wafer simple test structures are placed. The rest of the wafer is populated by the replicas of three designs, all in two configurations, i.e. CPW configuration for on wafer tests and flip chip configuration for PCB compatibility.

A set of 115 sequential process steps is adopted for the fabrication of the top plates (i.e. KaA process). In the FBK foundry the whole process flow is controlled by computer. Therefore the steps were uploaded to the CAM program which controls the manufacturing of each wafer lot. In the first run initially 6 process wafers and 6 test wafers (for process monitoring) were used. Furthermore, at this stage two splitting regarding the step height of the sealing ring were introduced as shown in Table 3.4.

Starting with the definition of sealing the manufacturing followed the predetermined order till the opening of the etch window for TSVs as depicted

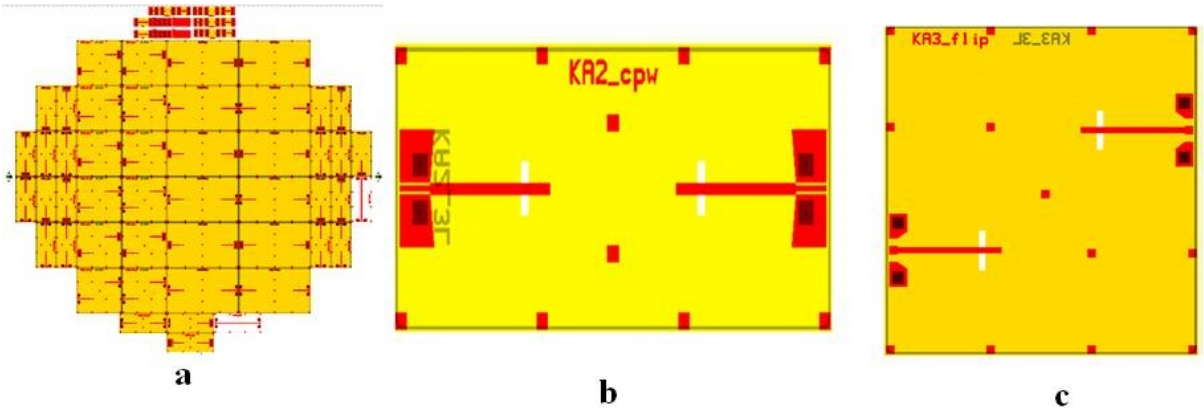


Figure 3.41: Wafer layout for the filter's top plate i.e. KaA process. (a) On top and on the bottom right of the wafers there are test and calibration structures. The rest of the area is divided between three different filter types, each in CPW and flip chip configuration. (b) die layout of the KA2_cpw structure, (c) die layout of the KA3_flip filter.

Table 3.4: Splitting scheme of run KaA1. A lot of 6 wafers divided in two splits for different sealing ring height.

SPLITTING	**STEP**	**LOTS**					
		1			**2**		
		1	**2**	**3**	**4**	**5**	**6**
A	Std: substrate						
	HR substrate 200 μm	x	x	x	x	x	x
B	Sealing Ring 1 μm	x	x	x			
	Sealing Ring 2 μm				x	x	x

in Fig. 3.37.b. After that to monitor the fabrication process vigilantly only wafers 2, 3 and 4 were etched and electroplated respectively and at this stage of fabrication two critical problems occurred were:

- Wafers borders etching

- Non metallization of Vias

Wafers Borders Etching

After the opening of the etch window the first problem was detected. The TMAH bulk etching of silicon also etched severely the wafer edges because during the opening of the etch window the hard mask was also removed from the border of the wafers. These exposed areas were no longer protected from the etchant and large areas were attacked thus making the wafers fragile and their handling more critical, as shown inFig. 3.42. Even with this initial problem the manufacturing process was continued in order to probe other hidden issues related to fabrication process.

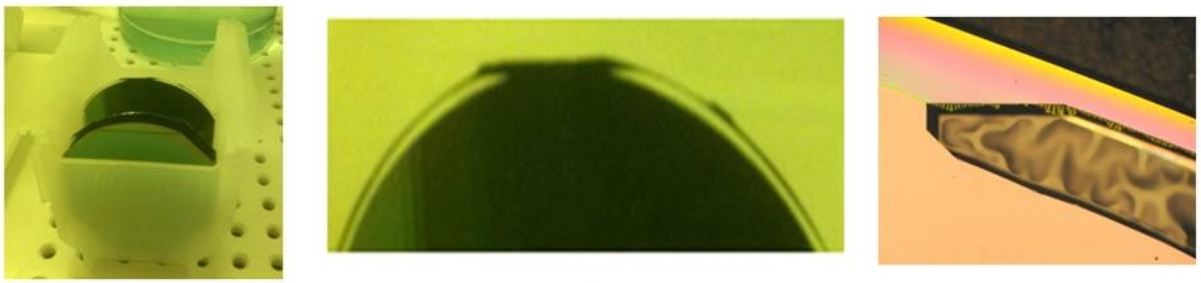


Figure 3.42: Damaged wafer edge after bulk etching of silicon for the through silicon vias while (b) and (c) are close ups.

Next the TEOS and the Si_3N_4 were removed applying dry etching and hot phosphoric acid (H_3PO_4) respectively from the bottom of the wafer followed by the growth of 1μm of oxide and the removal of the hard mask from the wafer top side. Then a seed layer was deposited on the bottom of the wafer in order to prepare the back side for the gold plating.

Problems with The Metallization of Vias Wafers Borders Etching

After seed layer deposition a dry film, Ordyl SY 300, which is compatible with a cyanide based plating bath was used as a masking layer on the wafer back side for the electroplating of gold. During the optical inspection after

the gold electroplating a second major problem was observed, i.e. nearly none of the via holes were coated with gold as presented in Fig. 3.43.

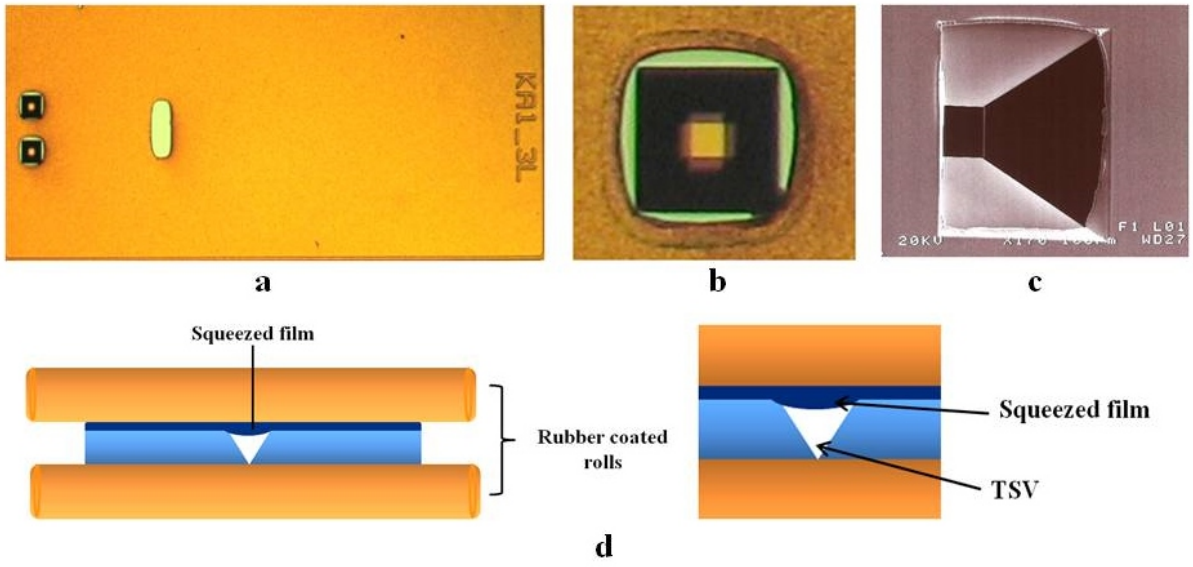


Figure 3.43: (a) and (b) bottom of a Ka1 die with two via holes and a slot on the left side. It is apparent that vias are not plated internally whereas the definition of slot is fair. (c) SEM images of a via which shows that the sidewalls and the bottom of via are not plated with gold. (d) Conceptual illustration of dry film squeezing into via holes.

A close examination of the wafer surface led to the origin of problem. During the lamination process the rubber coated roll presses the dry film into the via and the sharp bottom corner of the via cuts the dry film resulting in poorer resist conformation and uncovered via holes. Fig. 3.43.d shows a conceptual illustration of the process. During the following etching of the seed layer in the slots the seed layer was also etched from the sidewalls of the TSVs, which in turn could not be plated with gold.

A further investigation of TSVs brought up a third problem. In few vias were the side walls were perfectly plated the bottom was not coated at all. This problem was traced back to the hard mask removal step. On the first wafers this was accomplished, according to the schedule, by wet etching. Doing so during the removal of the two oxides also the oxide on the bottom

of the cavity (on the top of the wafer) was etched off which produced a strong undercut under the silicon edge which hindered the deposition of a continuous seed layer as shown in Fig. 3.44(a,b,c). The absence of seed layer in the shadow area did not allow the platting of the bottom of the via holes.

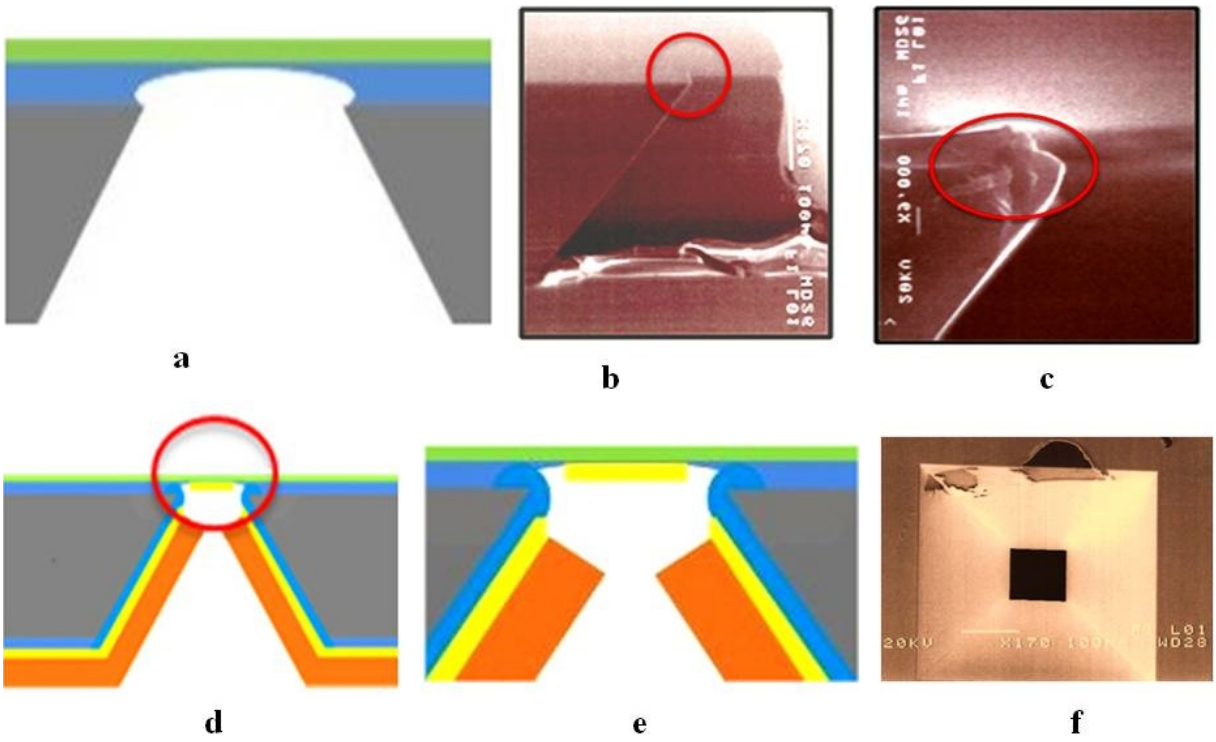


Figure 3.44: The removal of the hard mask on the wafer bottom by wet etching created a small undercut under the top silicon edge of the via (a - c). This hindered the deposition of a continuous seed layer (d, e) which results in a via only plated on the side walls (f).

3.19.2 Corrected Fabrication Process

The above mentioned problems were rectified in a second run on wafers 1, 5, 6 and the following changes in the processing sequence of: (a) TSV etching, (b) hard mask removal and (c) dry film lamination, were adopted in order to produce to useable top layer for the filters.

TSV Bulk Silicon Etching

To mitigate the problem related to the etching of the wafer border during the TSV etching it was decided to remove the edge cleaning process during the photo resist coating. This step is normally performed in order to remove about 2 mm of resist starting from the wafer edge by spraying an organic solvent from the bottom to the rear side of the wafer. By skipping this step better results in terms of edge protection during the bulk silicon etch were obtained. Nevertheless the handling of the wafers after the etching in TMAH without holder to protect the border remained still a critical aspect. In the future it has to be verified if the very small oxide membranes that form on the bottom of the via holes are able to withstand the hydrostatic pressure. A rough estimate shows that a 1 μm thick square membrane with 100 μm side length should be able to sustain a pressure difference of $\sim$1.7 bar. This is for sure enough to sustain the hydrostatic pressure that is present during the etching but it has to be evaluated if it is also enough to sustain the dynamic pressures that develop during handling of the wafer in the etching fluid.

Hard Mask Removal

A second correction in the processing sequence deals with the removal of the hard mask from the wafer backside. To avoid the etching of the exposed oxide from the bottom of the via hole cavity as sketched in Fig. 3.44.a, and to prevent any under etching or negative angle at the top of the vias that would lead to a discontinuity in the seed layer it was chosen to remove the hard mask multilayer on the wafer backside with a single step of dry etching since dry etching of silicon has widely been used in the fabrication of TSV [64–67]. Fig. 3.45(a, b) schematically shows how the cross section of the via should look like after this treatment.

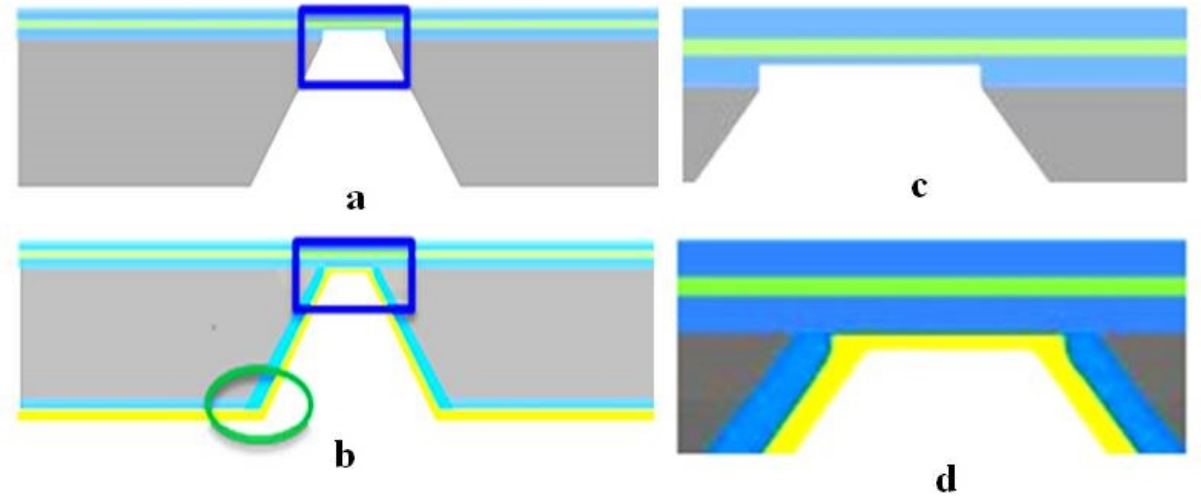


Figure 3.45: Schematic cross section of a via hole after hard mask removal by dry etching (a-b) and after the seed layer deposition (c-d). The use of dry etching eliminates the undercut of the silicon in the bottom of the via and makes “smoother" edge near the upper border which guaranties a good coverage of the seed layer without interruptions.

Dry Film Lamination and Via Metallization

After the seed layer deposition a third correction to the process schedule regarding the slot definition was made and with this lithography step the slots are exposed and then etched with gold etchant. It is important that the dry film is faultless otherwise the seed layer will be removed also in the areas of the defects. In the first test it turned out that one critical area is the via hole because the rubber coated rolls of the laminating tool tends to “cut" out the dry film over the vias and this process was also favored by the sharp edges of the vias. To guarantee the coverage of the via holes the resist was laminated together with an additional Mylar sheet, thick enough to reduce the risk of damaging the dry film hanging over the via holes. After the definition each via hole was carefully inspected and in those cases where the resist over the via holes was damaged the resist coating was repaired by applying a small droplet of standard resist with a syringe. After this the manufacturing of the wafers continued with the deposition of a 2.5 μm thick

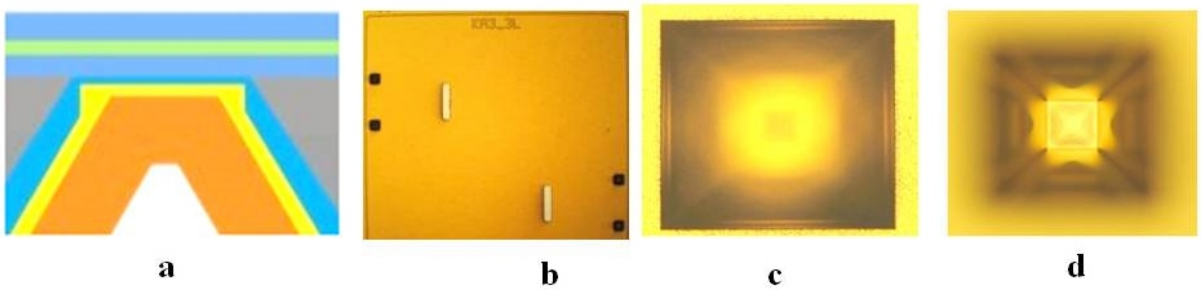


Figure 3.46: (a) Schematic cross section of the bottom of the via hole. (b) bottom view of a Ka3 die with two slots and the four via holes. (c) Close-up of a of via top and (d) via bottom coated with gold.

galvanic gold layer. With a conformal seed layer coating this time it was possible to cover the sidewalls of the vias as well as the bottom with a very high yield, this is illustrated in Fig. 3.46.

The last critical step was the opening of the via top to allow the electrical contact to the metallized plane of the wafer backside as demonstrated in Fig. 3.47. For this purpose the wafers were coated with standard PR and the top via were defined by lithography and dry etched till the bottom gold layer was reached. The larger square with slightly curved sides is the “footprint" of the bottom of the via cavity, which has been designed to be slightly larger than the via top. The misalignment between the two squares (in the order of $<$10 μm gives an idea of the precision of the front to back alignment that can be achieved.

The 1 μm thick oxide membranes supported with 2.5 μm of plated gold proved to be robust enough to sustain the 1 bar pressure difference. Fig. 3.47.c depicts the top via hole and the ghost image of the bottom of the via cavities left in the gold layer with minor misalignment from front to backside of the wafer.

Finally the top seed layer was deposited and defined and a 2.5 μm thick gold layer was grown by using the standard masking and plating sequence, as illustrated in Fig. 3.48. The process was finished with a 30 min sintering

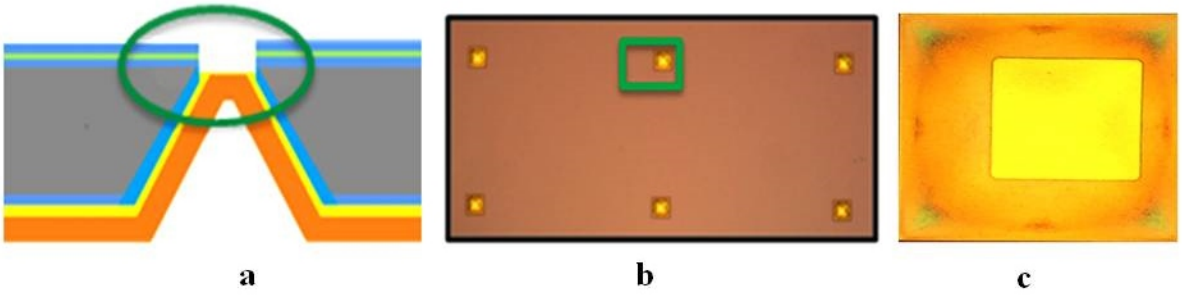


Figure 3.47: Opening of via top (a) schematic cross section of the structure, (b) picture of a Ka2 die from the top and (c) close-up of a via whereas the via corresponds to the square.

at 190 °C in nitrogen. After the above mentioned modifications the manufacturing process produced two usable wafers, i.e. top plates for ∼88 devices.

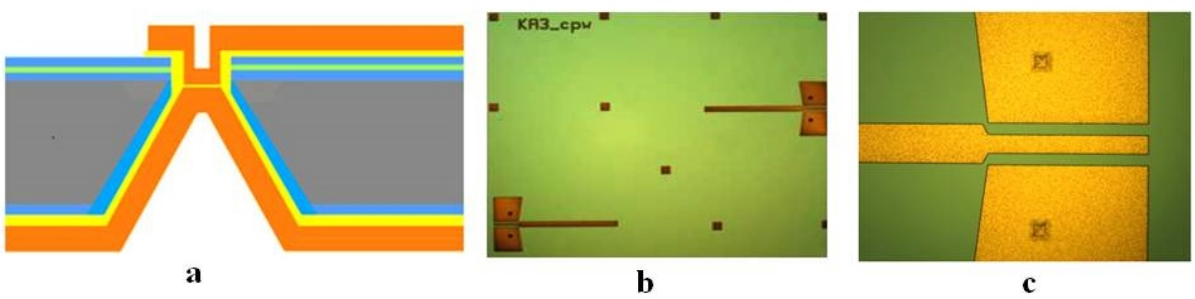


Figure 3.48: Top metallization: (a) schematic cross section, (b) top view of a Ka3 device and (c) close-up of a microstrip to CPW transition

3.20 Fabrication of the Middle Plate (KaB Process)

A detailed view of the middle plate geometries used for three different types of filters is presented in Fig. 3.49.a. The wafer region is comprising the replicas of the three filter designs including two layers for each design. While Fig. 3.49(b, c) presents the die layout of middle plates of KA3 filters.

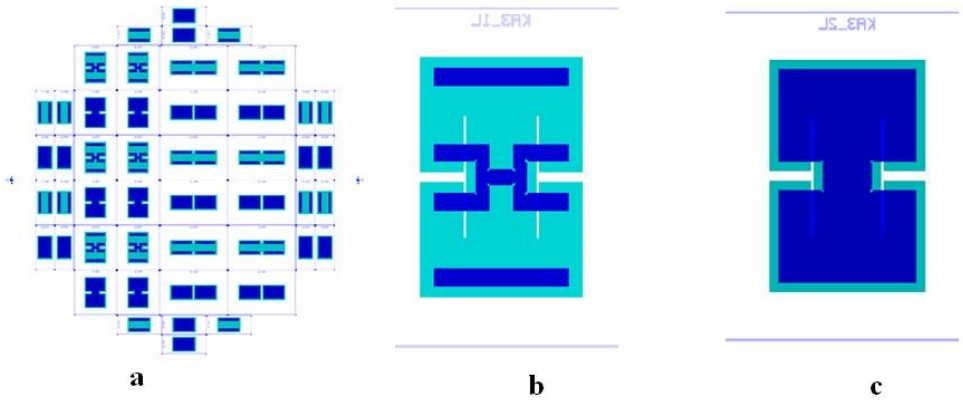


Figure 3.49: (a) Wafer layout for KaB Process. The area is divided between three different filter types including two different middle plates for each type. (b) Die layout of the KA3 middle plate with the membrane. (c) Die layout of the KA3 middle plate with cavity.

3.20.1 First Run of the KaB Process (KaB1)

To fabricate the middle plate geometries presented in Fig. 3.49.a, the process flow described in Section 3.18 can be transcribed into a process sequence of 94 individual processing steps, feasible in the FBK foundry, and uploaded to CAM program that control the manufacturing process. In this first run a total of 6 process wafers and 4 test wafers were used. In process development test wafers are extensively used to monitor the process sequence [68–70]. As in case of the KaA process it was also decided to include two splitting on the step height of the sealing ring as illustrated in Table 3.5

Table 3.5: Splitting scheme of run KaB1. A lot of 6 wafers divided in two splits for different sealing ring height.

SPLITTING	**STEP**	**LOTS**					
		1			**2**		
		1	**2**	**3**	**4**	**5**	**6**
A	Std: substrate						
	HR substrate 500 μm	x	x	x	x	x	x
B	Sealing Ring 1 μm	x	x	x			
	Sealing Ring 2 μm				x	x	x

For the KaB process the substrate material were 500 μm thick, p-type, <100>, HR $\sim$ 5000 Ω cm wafers. A sequential fabrication process as described in Section 3.18 was followed and after the growth of a first masking oxide the wafers were patterned for crystal alignment marks and etched and then the short anisotropic etch was performed in order to put into evidence the lattice planes. After this the sealing ring was patterned on the bottom of the wafer and also in this case two step heights were realized (i.e. 1 and 2 μm).

Then a second oxide masking layer and the top cavity etch window was defined and etched. The 20 μm shallow cavity was etched with a short ($\sim$30 min) anisotropic etch with a 1:4 TMAH:water solution at 80°C. The so formed shallow cavities showed perfect convex corners thanks to the small corner compensation structures included in the design as depicted in Fig. 3.50.

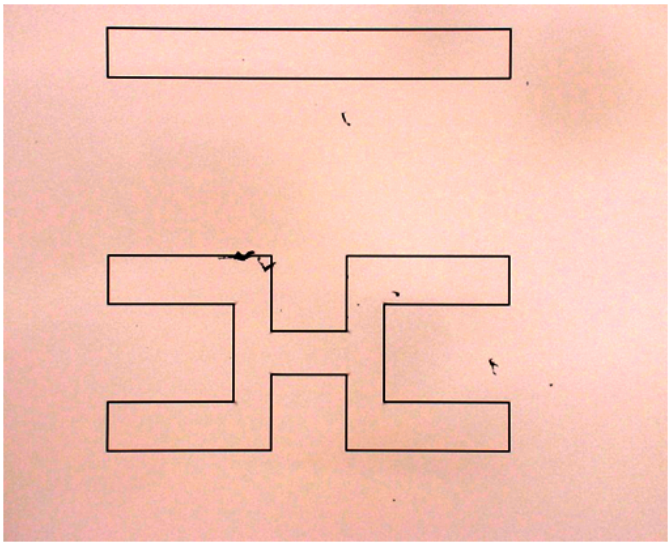


Figure 3.50: Top view of a Ka3 middle plate with the first shallow anisotropic etch performed (with the hard mask removed). The convex corners are square thanks to the corner compensation structures that have been included into the design.

Next the hard mask for the deep cavity etch, composed of 300 nm thermal oxide, 150 nm of Si_3N_4 and 300 nm of TEOS oxide, was deposited as shown in Fig. 3.40.d. The hard mask on the bottom side of the wafer was then

patterned and etched [71–74], as shown in Fig. 3.40.e. To this purpose a 1:4 TMAH : aqueous solution at 80°C was used. The etching was performed in a reactor made of fused quartz instead of Pyrex in order to eliminate any possible contamination with sodium as the wafers had to be oxidized after the anisotropic etch. Due to heat losses in the setup it was not possible to obtain the planned etch temperature of 90°C as with the old setup. Formation of a deep cavity is again a two step bulk anisotropic etching process [24]. In a first step with an etching time of 21hr at 80°C an approximately 450 μm deep cavity was etched. After measuring the cavity depth and recalibrating the etch rate in the 2^{nd} step, again at 80°C , the cavity was brought to the final depth as depicted in Fig. 3.51.a.

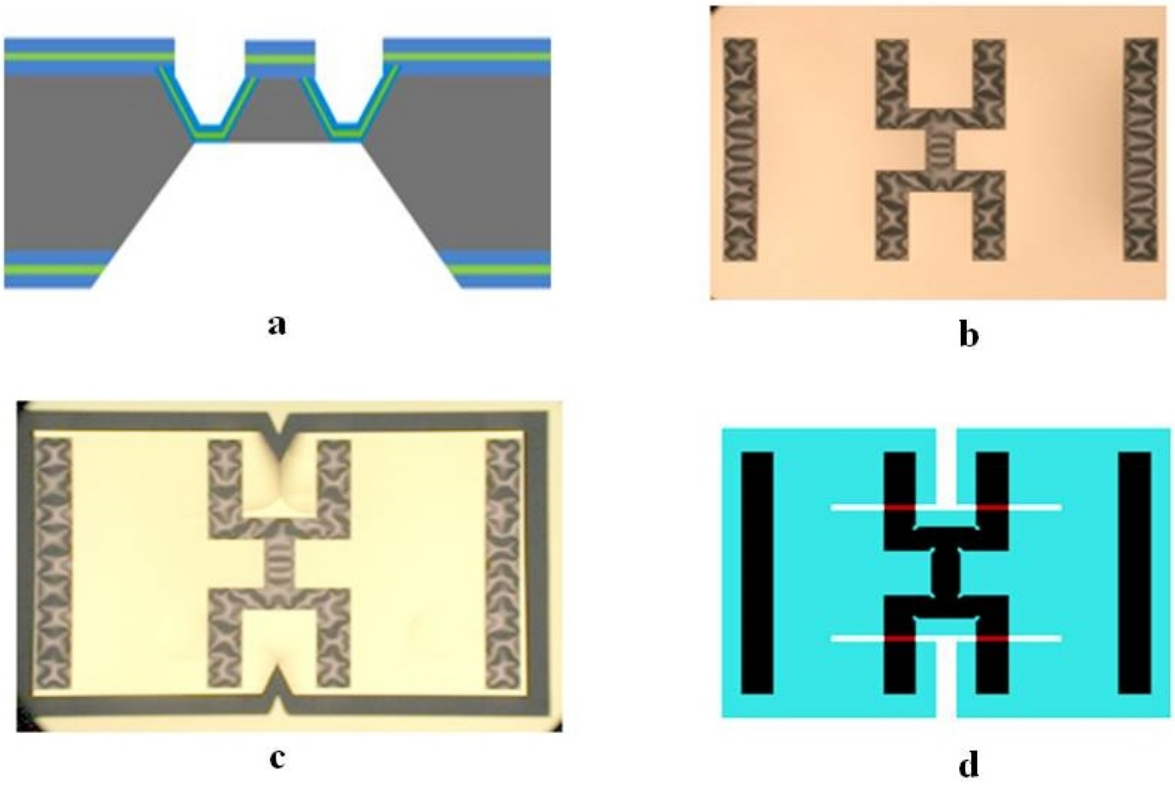


Figure 3.51: Anisotropic bulk etch of the main cavity: (a) schematic cross section, (b) top view of a Ka3 middle plane, (c) bottom view of the same die and (d) layout of the die showing the compensation structures (in white).

At this point the wafers were inspected and it became evident that the corner compensation structures were etched off completely and nearly nothing of the structures with convex corners survived, as presented in Fig. 3.51(c, d). This is apparent in the middle plane of the Ka3 structure where the separation walls between the two cavities almost disappeared. In this phase the problem was traced back to the crystal alignment. Due to the fact that the first litho step for the sealing rings was on the backside while the crystal alignment structures were realized on the wafer front side the measurements should have been mirrored. Because of this omission the alignment procedure in fact increased the misalignment to more than 2° The problem was immediately addressed by launching a recovery run, KaB2, but the previous run i.e. KaB1 was nonetheless continued in order to see if there are additional problems in the processing sequence.

The process was completed as per process schedule first by coating the wafers with a seed layer on both sides followed by gold plating as shown in Fig. 3.52. For gold electroplating an experimental set up was used where the wafer can be fully immersed in the electrolyte, facing a mesh type anode. First one side and then for the other side were plated. No particular problems were encountered, see Fig. 3.52.

3.20.2 First Recovery Run (Process KaB2)

After encountering the problem with the corner compensation structures a recovery run with three wafers was started immediately. As in the case of the KaB1 process it was also decided to include two splitting on the step height of the sealing ring, see Table 3.6.

The recovery run is similar to the previous run (KaB1) and again uses 500 μm thick, p-type, <100>, HR 5000 Ω cm Silicon wafers as substrates. The manufacturing followed the same schedule as run KaB1. Formation of crystal alignment marks begins with the growth of a first masking oxide. Then the

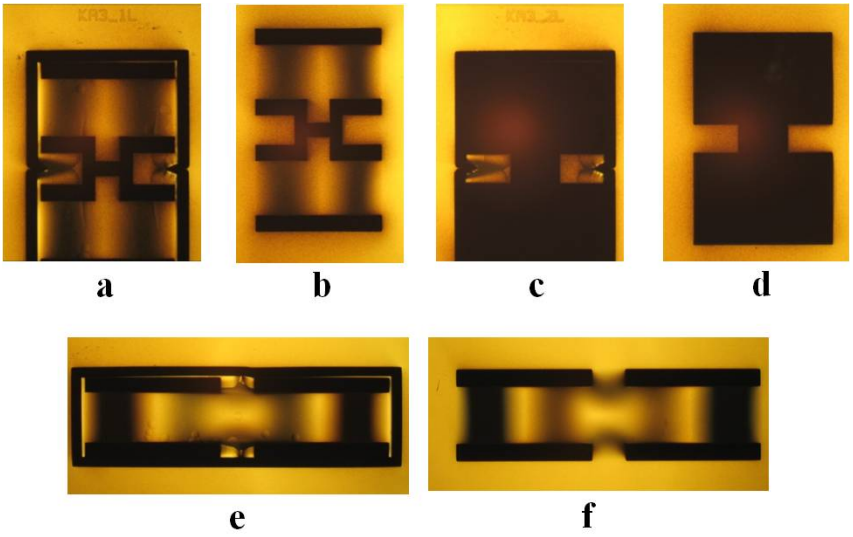


Figure 3.52: Completed wafers of KaB1 process. Middle plates for the Ka3 filter, (b and d) front view and (a and c) back view. Middle planes for the Ka4 filter, (e) front view and (f) back view.

structures for the crystal alignment were patterned and etched. This time attention was paid to correctly apply the measured crystal orientation to the mask on the backside of the wafer. The short anisotropic etch used to put into evidence the lattice planes was performed as before.

Next the sealing ring was patterned and two step heights were realized (1 and 2 μm) respectively. After the growth of a second masking oxide the top cavity etch window was defined end etched on wafer front side. The 20 μm

Table 3.6: Splitting scheme for run KaB2. The lot consist of 3 wafers divided in two splits for different sealing ring height.

SPLITTING	**STEP**	**LOTS**		
		1		**2**
		1	**2**	**3**
A	Std: substrate			
	HR substrate 500 μm	x	x	x
B	Sealing Ring 1 μm	x	x	
	Sealing Ring 2 μm			x

shallow cavities were etched with a short (∼30 min) anisotropic etch with a 1:4 TMAH:water solution at 80°C.

Next the etch windows for the deep cavity at wafer backside was opened and the cavities were etched with a 1:4 TMAH:water solution at 80°C. This time etching was performed in 5 steps in order to carefully monitor the evolution of the corner compensation structures, as illustrated in Fig. 3.53.

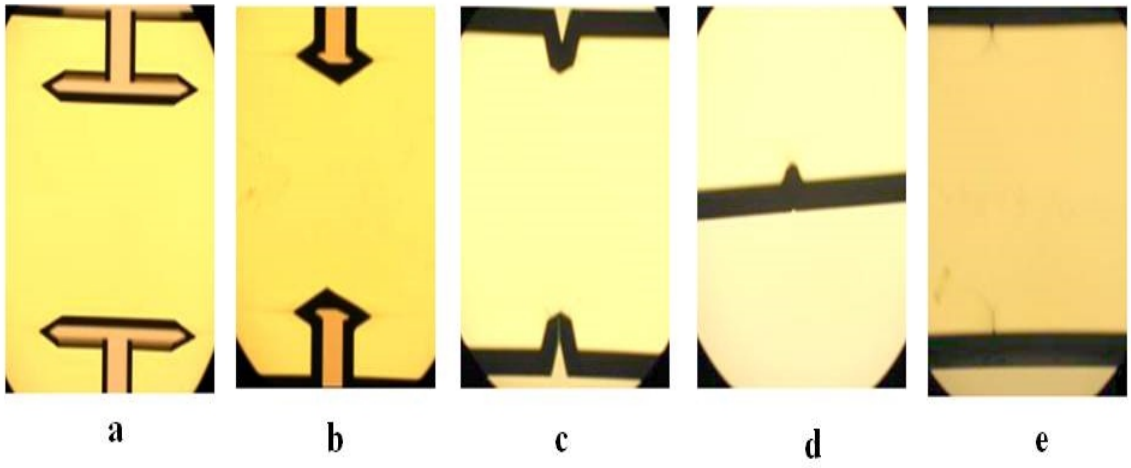


Figure 3.53: Anisotropic bulk etching of the deep cavity of run KaB2. The middle plane of the cavity of a Ka3 structure was monitored at different etch times/cavity depths. (a) 6h - 129 μm, (b) 11h 45' - 253 μm, (c) 18h 30' - 398 μm, (d) 21h 15' - 457 μm and (e) 22h 20' - 480 μm.

From the above figure it is apparent that beside the proper crystal alignment the corner compensation structures were again ineffective. The problem was finally traced back to two causes:

- Design error of the compensation structure
- Wrong etching conditions.

To properly deal with both issues it was essential to re-design the cavity etch mask then the optimization of the anisotropic etching set-up.

3.20.3 Corrective Actions in KaB2 Run

Mask Re-design and Optimization of Etching Temperature:

In order to identify correctly the error in the design of the compensation structures, all available data on the <110> bar compensation structures used in the layout was analyzed again. In addition to the (KaB2) run also the data on the old test run (ECE1) made in 2006 was investigated. The later run, used a purposely designed mask set for the measurement of the different etch rates of the various crystal planes of silicon in a variety of etching conditions as shown in Fig. 3.54.a. The test mask contains array of squares with different compensation structures at each corner for obtaining the convex corner.

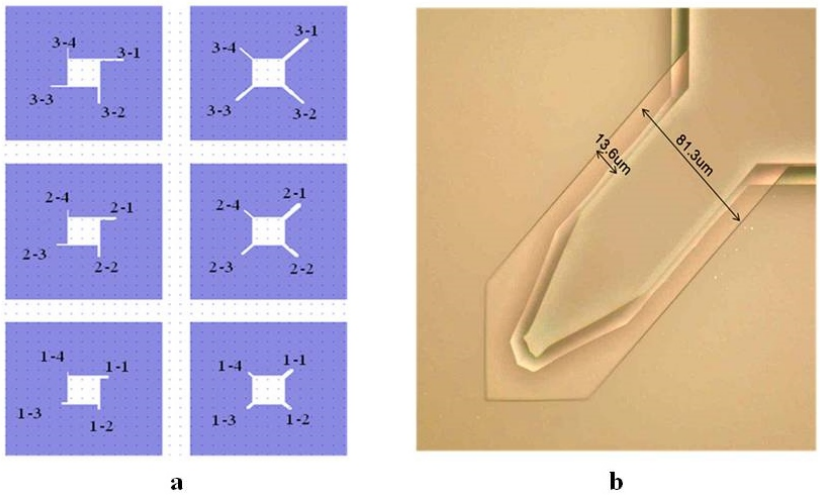


Figure 3.54: Test mask of run ECE1. (a) The layout contains test structures for <110> bar compensation structures on the left and <100> bar compensation structures on the right. Each corner compensation structure is identified by two numbers, the first one refers to the length of the group (4 structures per square) and the second refers to the length within a particular group. (b) Sample measurement. The etching was performed with a 25% TMAH water solution at 90°C for 20 min. Measured <100> under etch 13.6 μm and <100> etch rate 40.8 μm/h.

For this study two types of compensation bar structures were useful: <110> and <100> bar structures. In Fig. 3.54.b a sample measurement of

<100> bar compensation structure etched in a 25% TMAH water solution at 90°C is shown. All tests were performed at open circuit potential (OPC) as in the processing of the KaB samples. SEM images of the <100> bar structures after etching and with the relevant measurements are depicted in Fig. 3.55. While Table 3.7 summarizes the measured data for an anisotropic etch with a 25% TMAH water solution at 90°C considered for the analysis. From these data the calculated <311> etch rate at 90°C was 89.31 μm/h which is in accordance with the value, 89 μm/h, reported in [75].

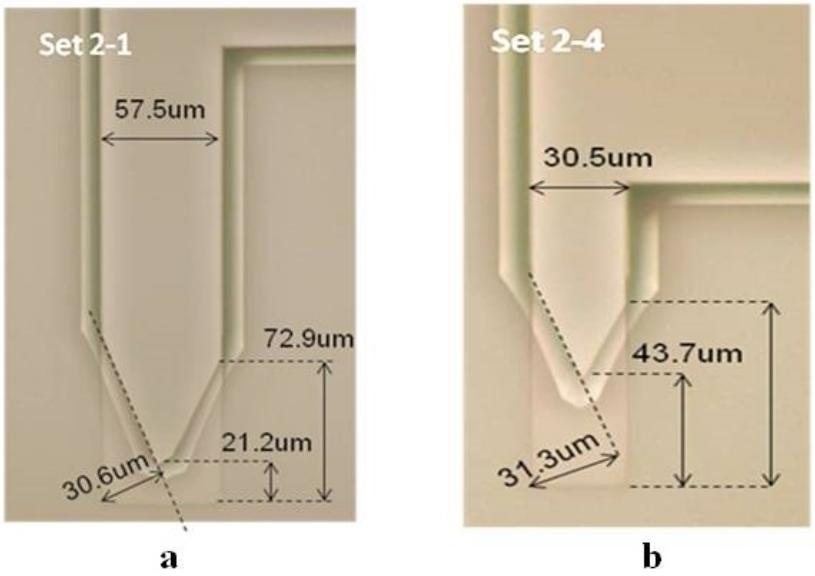


Figure 3.55: <110> bar compensation structures measured after 20min etch in a 25% TMAH water solution at 90°C. (a) a Set 2-1 structure and (b) a Set 2-4 structure.

Regarding the faster than expected etching of the convex corner compensation structures the main finding was that apparently the tip of the bar structure is etched relatively slower than the side walls. In theory both should etch at the same rate but the data shows that the tip is etched with a delay. Therefore the etch rates estimated on the etch rate of the tip are underestimated by about 50% and in turn the corner compensation structure was under dimensioned by the same factor.

Table 3.7: Summary of the measurements and the calculated etch rates for the <110> bar compensation structures for a 20 min etch at 90°C in a 25% TMAH water solution.

Test structure set	2-1	2-4
Bar width(μm)	57.5	30.5
<311> underetch(μm)	30.6	31.3
Tip etch(μm)	21.2	43.7
Tip base etch(μm)	72.9	70.6
Tip base etch rate(μm/h)	218	211.8

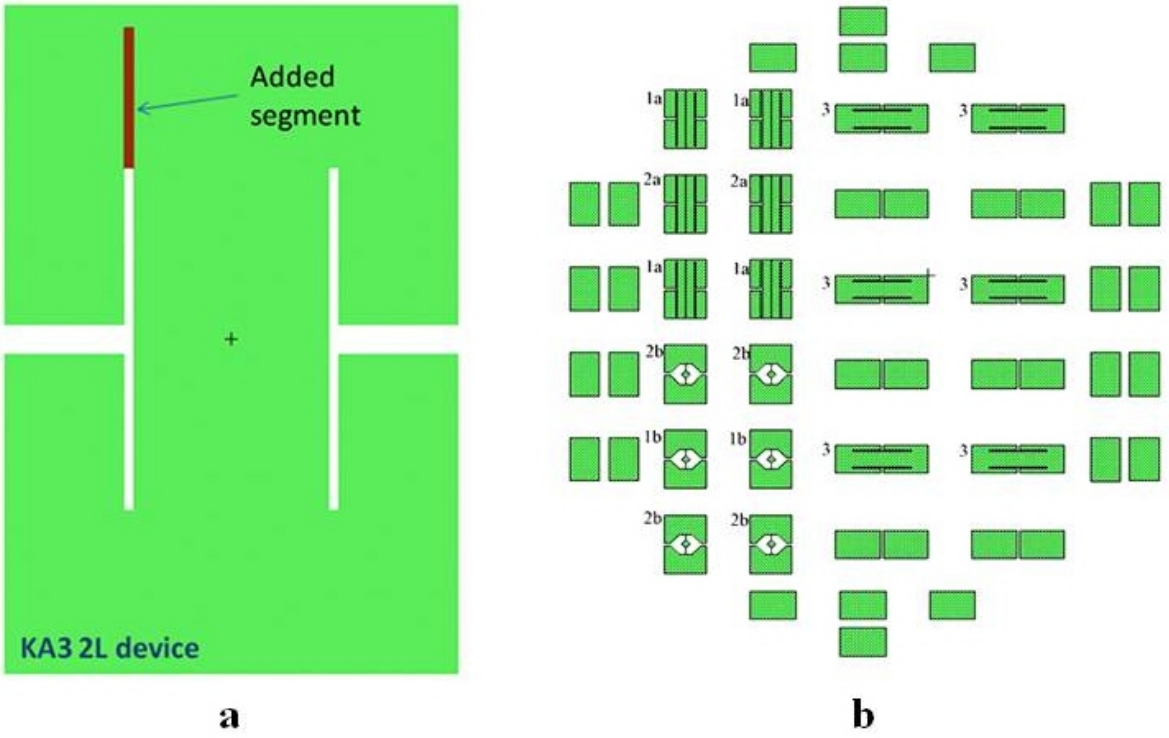


Figure 3.56: (a) Example of a corrected structure. (a) New mask layout with corrected corner compensation structures. Legend: 1a: Ka3-1L with 90° compensation, 1b Ka3-1L with 45° compensation, 2a Ka3-2L with 90° compensation, 2b Ka3-1L with 45° compensation and 3 Ka4-1L with 90° compensation.

Taking into account the data from test ECE1, valid for a 25% TMAH:water solution at 90°C, the correct ratio for the etch rates between the tip and the <100> plane is 215:40 = 5.38, while the same ratio calculated from the

data of run KaB2, valid for a 25% TMAH:water solution at 80°C, results in 143:21.5 = 6.65. On the other hand for Ka3_2L (i.e. 2^{nd} layer) the <110> bar compensation structures were designed with a length of 1680 μm. Considering etching with a 25% TMAH:water solution at 90°C the correct length would have been 2582 μm while for an etching with the same solution at 80°C the compensation structure must be 3192.6 μm long as shown in Fig. 3.56.a. Thus to rectify the design error a new mask for the cavity etch was designed, as presented in Fig. 3.56.b, with an extension of the <110> bar compensation structures.

However, in this case the <110> bar compensation structures also by adopting these corrections it will be not possible to completely compensate the convex corner. Even in case of optimum compensation their remain some residues and small peaks as depicted in Fig. 3.57.

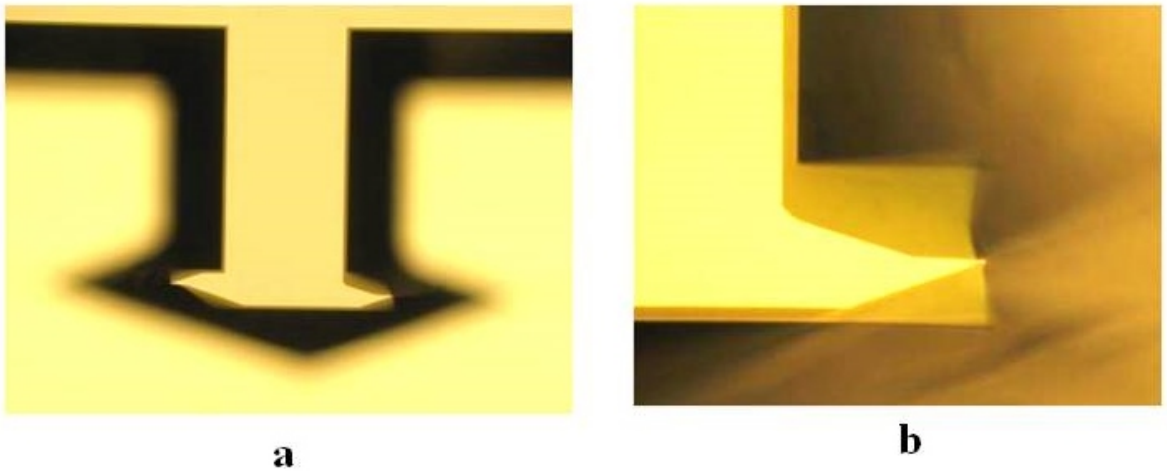


Figure 3.57: Best corner compensation that can be obtained with <110> bar structures. (a) two convex corners near optimum etch depth/best compensation, (b) Magnified image of the edge.

In a very few die layers it was possible to include a <100> bar compensation structure at 45°, see Fig. 3.58.a. The main advantage of these structure is that they provide a straight edge but on the other hand they are large and also require a large space to be placed. Due to the fixed space a minimum

gap between them that allows the under etch of the structure was left, refer to Fig. 3.58.b.

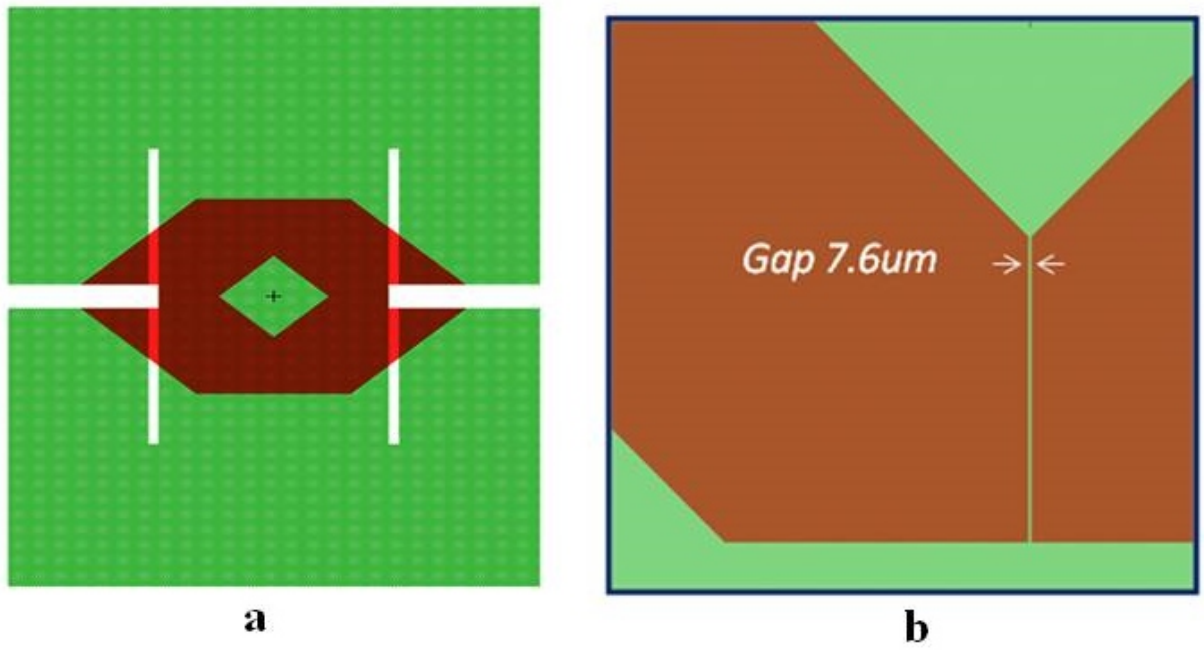


Figure 3.58: Layout of the <100> bar compensation structure at 45°. (a) die layout and (b) a close up on the critical detail showing the difficulty to place the structure in this design.

In summary there are two main reasons behind the failure in not attaining the perfect corner compensation in KaB2 run. First the compensation structures were too short and second the etching was performed at a lower temperature than for which the compensation structures were designed. Due to the fact that both 45° and 90° compensation structures are outsized for an etching at 80°C. The etching should have been performed at 90°C.

3.20.4 Second Recovery Run (Process KaB3)

Once identified the main causes of the failure of the corner compensation structures second recovery run based on 4 Si wafers with the similar specs as of KaB2 was launched. In the KaB3 run two splitting on the step height of

sealing ring as in case of previous two runs was also made. Table 3.8 shows the splitting scheme for KaB3 run.

Table 3.8: Splitting scheme for run KaB3. The lot consist of 4 wafers divided in two splits for different sealing ring height.

SPLITTING	**STEP**	**LOTS**			
		1		**2**	
		1	**2**	**3**	**4**
A	Std: substrate				
	HR substrate 500 μm	x	x	x	x
B	Sealing Ring 1 μm	x	x		
	Sealing Ring 2 μm			x	x

The KaB3 process was aligned with the same manufacturing sequence as in the KaB2 run and the same sequence was followed till the anisotropic etching of deep cavity. Before the cavity etch some changes were made in the etching set up in order to increase the etching temperature to 90°C, as demanded by the design. The setup is made up of double walled reactor in quartz which is heated through a heating fluid controlled by a thermostat that is placed at the back side of the wet bench. The temperature in the vessel is limited by two factors: (a) heat losses in the pipes and (b) maximum temperature of the fluid in the thermostat or in other words the boiling temperature of the fluid. The heat losses were reduced by isolating the tubes and the vessel with reflective aluminum foil. Next water as heating fluid was replaced with a glycol based solution which boils at higher temperature. Lastly fluid velocity was increased by removing the air bubbles in the fluid circuit. All these measures allowed to set the reactor temperature to 90°C.

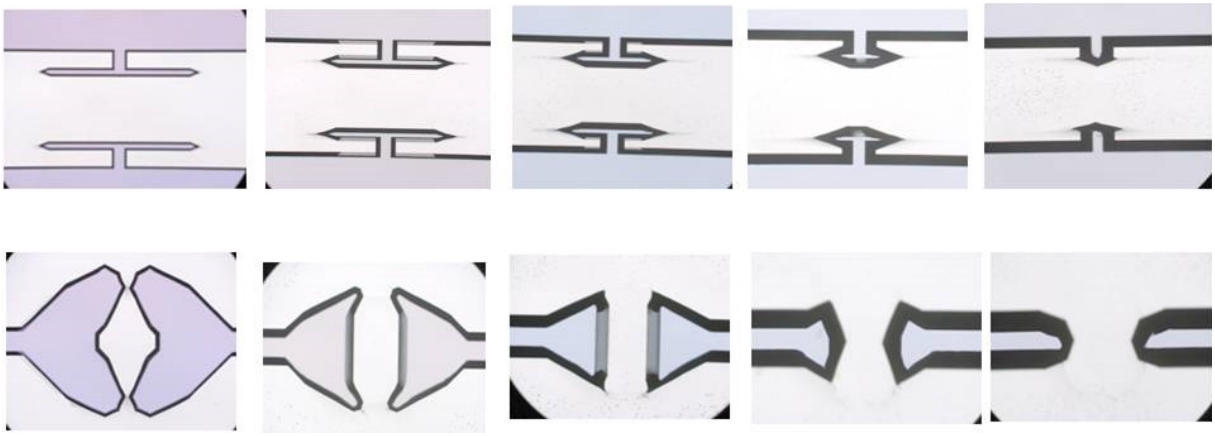


Figure 3.59: Evolution of the corner compensation structures with time for wafer 1 of run KaB3. First row shows the <110> and 2nd row shows the <100> bar compensation structure. The relative etch times are reported at the bottom.

Cavities were etched in the so modified setup and the etching was performed with the 1:4 TMAH:water solution at 90°C. The wafer border was preserved by a newly acquired wafer holder that covered the wafer border successfully during the etch. Again the etching was performed in 5 steps in order to monitor the evolution of the corner compensation structures as presented in Fig. 3.59. Overall the changes in the etching setup made the corner compensation structures more effective albeit not totally free of defects. In case of the <110> bar structure, as expected, small lateral horns remained and both compensation structures resulted still slightly under dimensioned.

At break through, i.e. when the two cavities meet, additional defects appeared due to the very tight design of the structures, see Fig. 3.60. These defects are mainly horn like shapes generated in the membrane layer which sometimes weld the membrane to the outer rim of the structure. These structures cannot be removed by over etching because otherwise the condition for corner compensation is no more satisfied. Within these limitations all four wafers were processed successfully.

After the etching of the cavity the hard mask was removed and the wafers were oxidized at 975°C in steam atmosphere in order to grow 1 μm of thermal

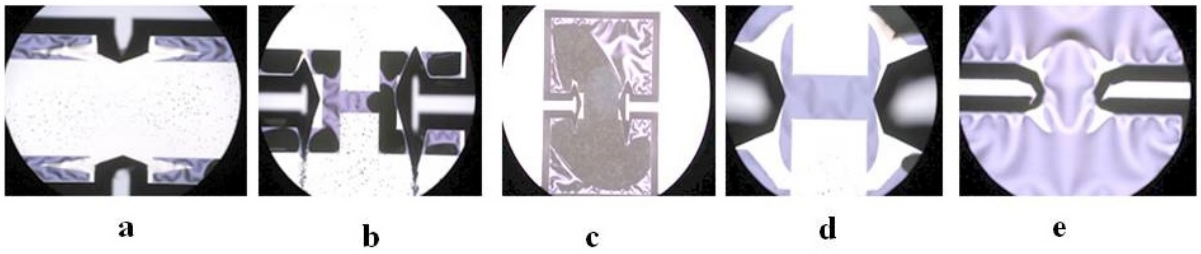


Figure 3.60: Defects left by the corner compensation structures. The <110> bar structures generate horns in the top membrane (a - c) which sometimes welds the membrane to the fixed part. The <100> bar structure shows similar problems (d - e).

oxide. Next a seed layer was deposited by PVD on both sides of the wafers followed by electroplating of gold on both sides as already successfully experimented in the previous run. Finally the gold plated wafers were sintered at 190°C for 30 min and this completed the manufacturing sequence of the middle planes.

3.21 Manufacturing of The Bottom Plate and Structural Characterization

For the bottom layer standard, 500 μm thick, HR, p-type, <100>, silicon wafers have been used. The bottom plates of the Ka filters are without any geometry and they were simply prepared by first growing 1 μm thick thermal oxide and then depositing a multimetal seed layer Cr/Au/Cr (2.5/25/2 nm). After that a 2.5 μm thick gold layer was electroplated, see Fig. 3.61.

Gold is widely used material in MEMS and semiconductor industry specially when an application, e.g. RF MEMS devices, requires low electrical resistivity and hermetic packaging [76–78]

After fabrication the wafers were inspected and the most critical parameters measured. There are two basic aspects of the manufactured elements, which are crucial for the realization of a filter:

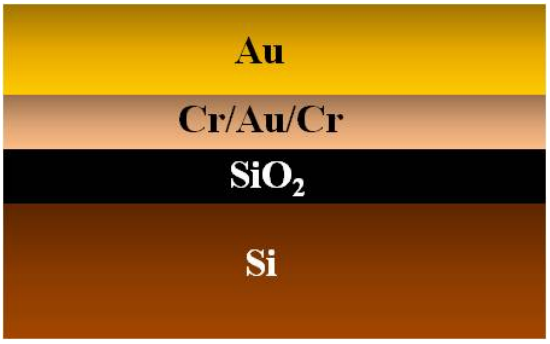


Figure 3.61: Cross sectional view of multimetal seed layer composed of Cr/Au/Cr.

- the roughness of the plated gold layer
- the uniformity and thickness of the coverage, especially around critical points like the sharp corners which are formed in that position where the two cavities meet.

Roughness of the electroplated layers is directly related to its thickness and it increases with the thickness of the plated coating. In order to measure the roughness of the, nominal, 2.5 μm thick plated gold layer a KLA-Tencor P-15 mechanical stylus profiler was used. The roughness was measured in 5 points on the wafer on a 200 μm long trace, as shown in Table 3.9

As expected the values are higher than for evaporated films but still within an acceptable range of the design parameters of the devices. In addition a few devices of the KaB run were diced through one of the most critical areas of the middle plane, i.e. the point where the upper cavity meets the lower cavity. This was done to measure thickness and coverage uniformity of the plated gold layer on the manufactured devices. The cross section made by dicing the device was inspected with a SEM, as illustrated in Fig. 3.62. At the juncture between the upper and lower cavity, depending if the upper cavity is smaller than the lower cavity or vice versa the geometry of the edge changes quite drastically, but even in the most awkward situation, as shown in Fig. 3.62(b). The coverage of the edge resulted conformal and the measured thickness was

Table 3.9: Sample roughness measurement of the 2.5 μm gold layer of the KaB2 samples. All values are in nm.

Parameters	**Center**	Top **left**	Top **right**	Bottom **left**	Bottom **right**	**Mean**	Std-**dev**
Ra **Roughness**	45.5	76.3	77.5	93.5	85.6	75.7	18.2
Rmax **Max Ra**	71.2	104.4	131.7	202.7	130.5	128.1	48.4
Rq RMS	60.2	94.4	102.4	134.4	11.4	80.6	46.8
Peak	254.3	301.5	369.2	625.1	392.4	388.5	143.1
Valley	187.1	198.3	297.5	427.8	274	276.9	96.8
Peak **valley**	441.5	499.8	666.7	1052.9	666.5	665.5	238.6

$\sim$5.5 μm. A last concern of the design team was related to the radius of curvature of the sharp corners produced by the anisotropic etching. This radius was found to be $\sim$5 μm, i.e. of the same order of the thickness of the gold layer.

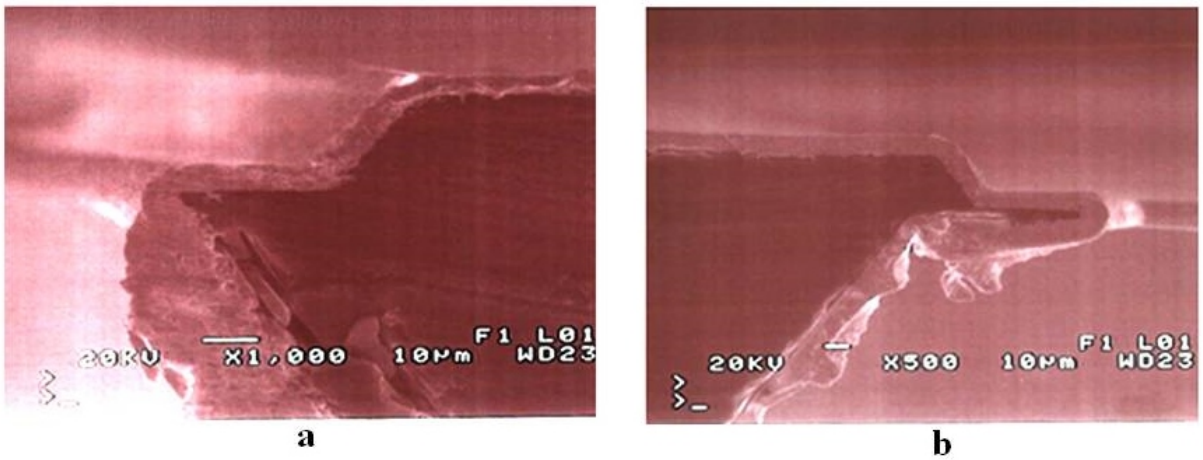


Figure 3.62: SEM picture on a cross section of a KaB middle plane. The geometry of the edge that forms at the conjunction between the upper and lower cavity. A sharp edge forms depends if the lower cavity is (a) smaller or (b) wider than the upper cavity.

Finally the wafers prepared from the KaA and KaB processes were subject to dicing. The dicing was performed on by DISCO^R DAD-2h-6T dicing saw machine and then top, middle and bottom layers were separated, visually inspected, selected and then arranged in a sequential order for the final assembly of the devices.

Chapter 4

Design and Fabrication of L/S Band Filters

4.1 Introduction

This chapter summarize the design and technology work of the L/S band filter. In order to meet the ESA requirements a 4^{th} order pseudo-elliptic filter realized on three 1500 μm and one 200 μm thick Si wafers has been proposed. The chapter also describes the design, fabrication and characterization of dedicated test structures fabricated on HR 500 μm thick Si wafer. The main scope of this technology run was to investigate experimentally the critical issues of the fabrication process and the design, and to optimize both.

4.2 Filtering Function and Filter Topology Analysis for the L/S Band Filter

ESA's electrical requirements for the L/S band filter are reported in Table 4.1. To meet these specifications analytical models have been developed describing filtering functions and filter topologies. The models have been verified by ANSYS HFSS. To this purpose 4^{th}, 5^{th} and 6^{th} filter orders were examined to achieve a compact filter design with acceptable Q-factor and

Table 4.1: Electrical requirements of L/S band filter.

ID	PARAMETER	VALUE	UNITS
A1	Centre frequency (FC)	2000	MHz
A2	Useful bandwidth	125	MHz
A3	Maximum insertion losses over bandwidth	2.5	dB
A4	Peak to peak insertion losses flatness	0.2	dB
A5	Maximum S11 and S22	-15	dB
A6	Group delay variation over bandwidth	1.5	ns
A7	Out-of-band rejection: FC±150MHz to FC±2000MHz	40	dB
A8	Nominal input power	10	dBm
A9	Operating temperature	-10 to +75	°C
A10	Storage temperature	-30 to +90	°C
A11	Mass	TBD	g
A12	Footprint	TBD	mm2
A13	Interface	SMT like	-

with a minimum number of resonators.

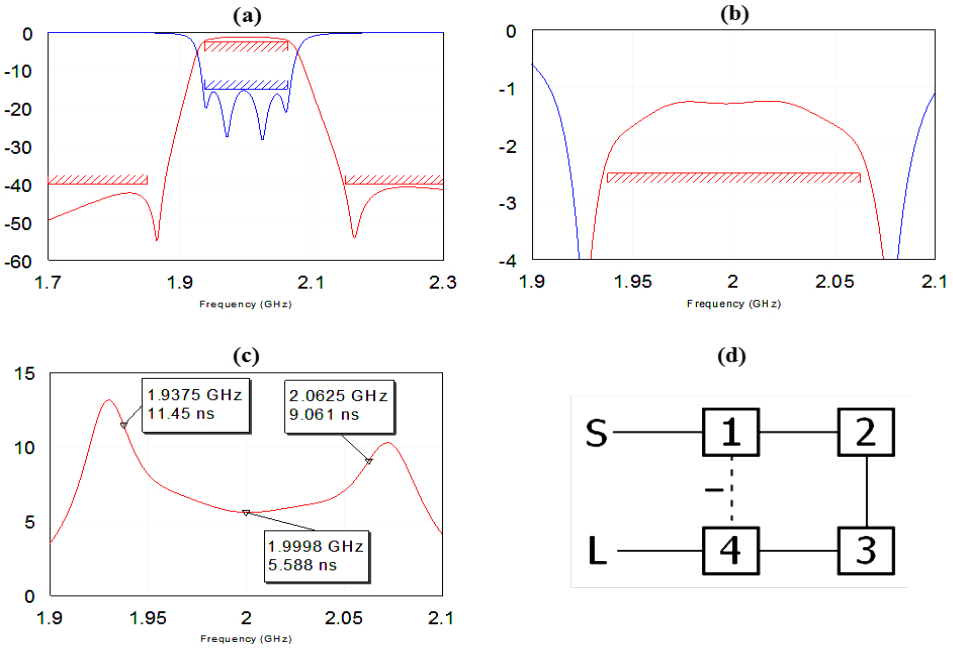


Figure 4.1: Fourth order filtering function with two TZs and Q=270: (a) S-parameters, dB (b) in-band S21, dB (c) group delay, ns; (d) a possible filter topology. Courtesy: UNIPG.

4.2.1 4^{th} order Filtering Function

In order to study the effect of the key parameters a lumped element model for the resonators was employed. As a starting point a 4^{th} order filtering function was adopted and next simulated using ANSYS HFSS assuming that the requirements labeled as A1, A2, A3, A5, and A7 could be satisfied using 4^{th} order filtering functions with two symmetric transmission zeros, and using resonators with a minimum Q-factor of 270. Fig. 4.1 shows ANSYS HFSS simulation for such a filtering function, along with the group delay and a expected filter topology.

The simulated results of Fig. 4.1(b) and 4.1(c) are showing approximately 1 dB peak to peak insertion loss variation and 6 ns group delay variation. Unfortunately with such values the electrical requirements labeled as A4 and A6 cannot be fulfilled by 4^{th} order configuration, see Table 4.2. Both in-

Table 4.2: Compliance matrix for the electrical requirements of 4^{th} order L/S band filter.

ID	PARAMETER	VALUE	UNITS	Comp	Expected
A1	Centre frequency (FC)	2000	MHz	C	
A2	Useful bandwidth	125	MHz	C	
A3	Maximum insertion losses over bandwidth	2.5	dB	C	
A4	Peak to peak insertion losses flatness	0.2	dB	NC	1
A5	Maximum S11 and S22	-15	dB	C	
A6	Group delay variation over bandwidth	1.5	ns	NC	6
A7	Out-of-band rejection: FC±150MHz to FC±2000MHz	40	dB	C	
A8	Nominal input power	10	dBm	C	
A9	Operating temperature	-10 to +75	°C	C	
A10	Storage temperature	-30 to +90	°C	C	
A11	Mass	TBD	g	-	
A12	Footprint	TBD	mm^2	-	
A13	Interface	SMT like	-	C	

sertion loss and flatness (A4) can be improved by higher Q-factors of the resonators (i.e. > 1000). The drawback is that at lower frequencies such as 2 GHz a Q-factor > 1000 can be obtained by employing large and intricate structures, like half-wave transmission lines or waveguide cavities: this would be probably out of the scope of the L/S band filter whose aim is to achieve compact filters. The above mentioned figures also reveal that the group delay and insertion loss variation is maximum at the edges of the passband. Therefore, a higher flatness of such parameters could be obtained by broadening the bandwidth and adopting higher order filtering functions.

4.2.2 5^{th} order Filtering Function

The widening of the bandwidth at one hand allows adequate passband frequency margins that can be used to compensate for manufacturing tolerances and temperature variations (A9). On the other hand, the wider the bandwidth the narrower the transition bands, thus needing higher order filters employing more resonators. This can be achieved by employing a 5^{th} order filtering function with 2 transmission zeros. This configuration allows widening of the bandwidth up to 165 MHz (20 MHz frequency margins at both passband sides). Fig. 4.2 shows the filtering function for Q=270 (solid lines) and Q=500 (dashed lines), along with the group delay and a possible filter topology. With regards to insertion loss flatness, for Q=270, the peak to peak variation is 0.4 dB (instead of 1 dB as for the 4^{th} order filtering function); the requirement A4 (0.2 dB peak to peak variation) can be fulfilled with a Q-factor greater than 500. The group delay variation is 2.8 ns, that is better than that obtained with the 4^{th} order filter (6 ns), but still quite far from the requirement A6 (1.5 ns). Therefore, to minimize the gap between the ESA electrical requirements and the filter's design next simulation was performed on 6^{th} order filter.

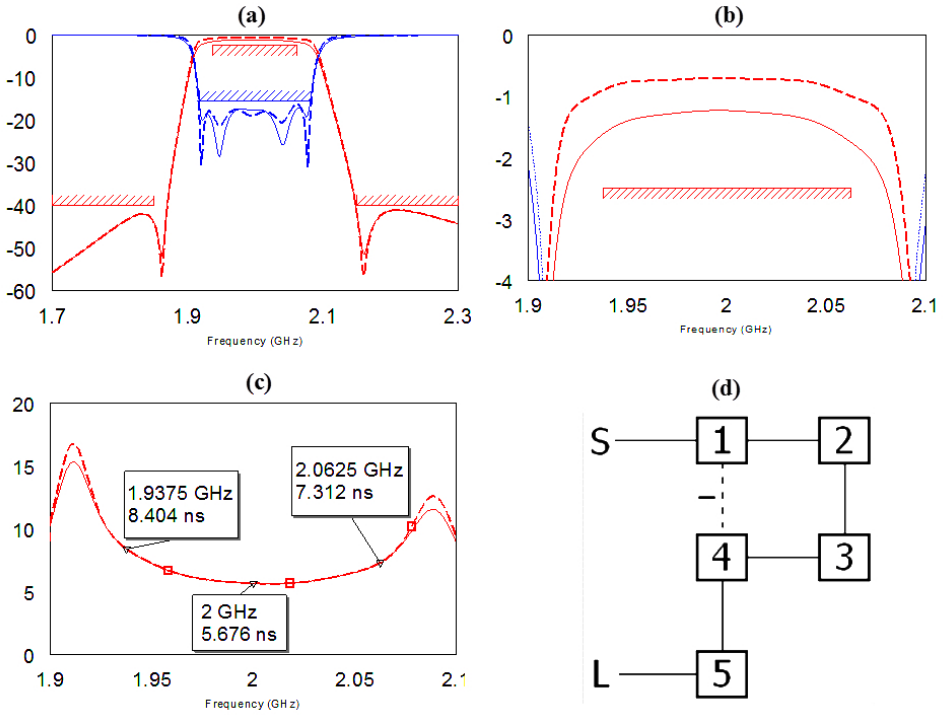


Figure 4.2: Fifth order filtering function with two TZs and Q=270 (solid lines) and Q=500 (dashed lines): (a) S-parameters, dB (b) in-band S21, dB (c) group delay, ns (d) a potential filter topology. Courtesy: UNIPG.

4.2.3 6^{th} order Filtering Function

To further improve the simulated results for requirements (A4 & A6) a wider bandwidth could be obtained by using 6^{th} order filtering functions. Whereas the filter selectivity can be improved by realizing 2 transmission zeros in the stopband 2 further zeros could be employed to reduce the group delay variation by placing the zeros in the real axis of the complex plane. Fig. 4.3 shows filtering function, along with a possible filter topology.

Preliminary simulations show that the requirement (A6) is very close to the fulfillment (roughly 1.7 ns instead of 1.5 ns as required), see Table 4.3. However, in order to address the insertion loss flatness requirement (A4) a Q-factor of 700 would be required (instead of 500 as for the 5^{th} order filtering function).

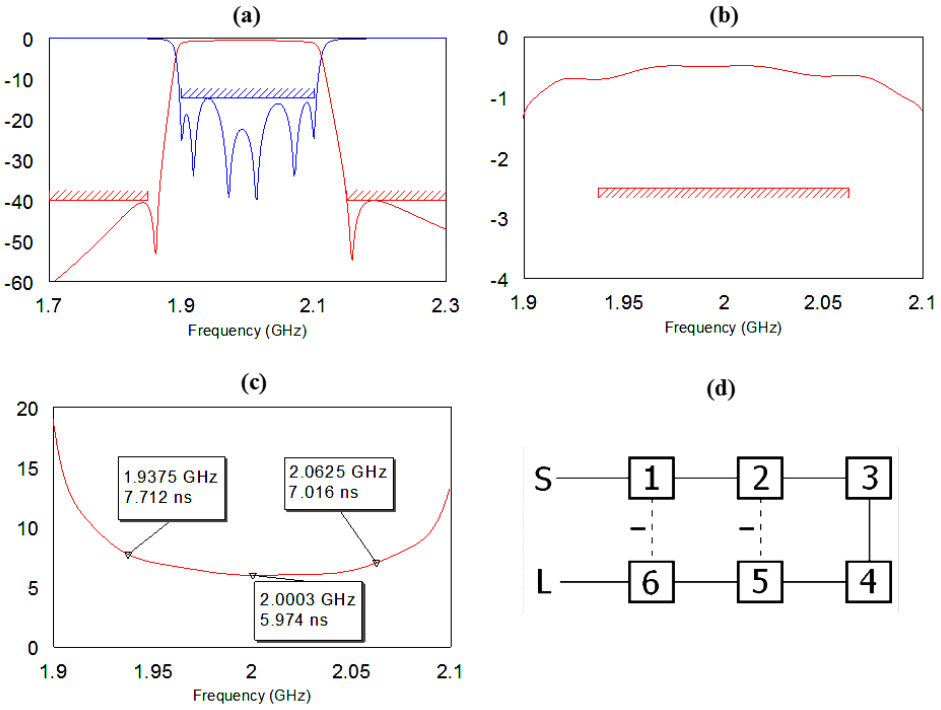


Figure 4.3: Sixth order filtering function with two TZs, two real zeros, and Q=700: (a) S-parameters, dB; (b) in-band S21, dB (c) group delay, ns (d) a potential filter topology.

Table 4.3: Compliance matrix for the electrical requirements of 6^{th} order L/S band filter.

ID	PARAMETER	VALUE	UNITS	Comp	Expected
A1	Centre frequency (FC)	2000	MHz	C	
A2	Useful bandwidth	125	MHz	C	
A3	Maximum insertion losses over bandwidth	2.5	dB	C	
A4	Peak to peak insertion losses flatness	0.2	dB	NC	0.3
A5	Maximum S11 and S22	-15	dB	C	
A6	Group delay variation over bandwidth	1.5	ns	NC	1.7
A7	Out-of-band rejection: FC±150MHz to FC±2000MHz	40	dB	C	
A8	Nominal input power	10	dBm	C	
A9	Operating temperature	-10 to +75	°C	C	
A10	Storage temperature	-30 to +90	°C	C	
A11	Mass	TBD	g	-	
A12	Footprint	TBD	mm^2	-	
A13	Interface	SMT like	-	C	

The obtained results for 4^{th}, 5^{th} and 6^{th} order filtering functions and related topologies allows the conclusion that the requirements A4 and A6 can only be meet with higher filter orders ($= 6$) and comparatively high Q-factors ($= 700$). Moreover, the use of high filter orders increases the sensitiveness with respect to the manufacturing accuracy and also the literature review of micromachined filters on L/S in (Chapter 2) confirms that, it is not common to find published data on L/S band filters with orders larger than 4. Additionally, a Q-factor of 700 requires a cumbersome physical realization for the resonators, thus compromising the filter compactness.

From this analysis it became evident that it is possible to realize L/S band filters with a limited number of resonators (4) and with a reasonable Q-factor (270), that are suitable for the project in the sense that they could be small and compact, but from Table 4.2 it is clear that the requirements A4 and A6 are far more stringent that they could be addressed successfully by a design that exploits the realistic capabilities of the micromachining technology. This could be only achieved by using higher order filters and suitable resonators.

4.3 Identification of the Basic Resonator

This section presents the types and physical realization of the resonators and highlights advantages and critical aspects of the solutions shown in Chapter 2 [41, 44]. As pointed out in Chapter 3 it is reasonable to expect that, the resonator technology directly impacts on the resulting unloaded Q-factor. In general it is found that as the resonator size decreases the resulting unloaded Q-factor also decreases. The reason is that in smaller structures the EM field is more concentrated, which increases significantly the losses that occurs on the resonator surfaces. Therefore, in spite of their compactness, lumped element based resonators [10, 38, 39] are commonly unsuitable to provide reasonable high Q-factors. On the other hand, three-dimensional waveguide

cavities offer very high Q-factor [79–81] but also occupy a considerable volume that, especially at the lower part of the microwave spectrum, can be very cumbersome. The trade-off between compactness and Q-factor is therefore an essential issue in the design of microwave filters.

As shown earlier in Subsection 4.2.3 for the design of a LS band filter, resonators having a Q-factor larger than 270 are needed. This is due to the fact that the measured Q-factor is normally 60% lower than the simulated one. Therefore for design purpose the practical Q-factor requirement should be set to 400. This decrease in Q-factor in fabricated designs is generally due to roughness, sharp edges and other parasitic effects, such as the losses occurring into the thin dielectric membranes.

As shown earlier in general the current trend in microwave filter technology is weight and overall volume reduction of the communication system. Suspended membrane resonators or cavity based resonators provide good performance but at the expense of large volumes. On the other side lumped element resonators [10, 38, 39] can be very compact, but preliminary simulations have shown that their Q-factor is significantly smaller than the minimum required above. Also half-wave TEM transmission line resonators [3, 27, 82] albeit provide acceptable Q-factors are quite large for a L/S band SMT component: as an example at 2 GHz the half wavelength resonator is roughly 70 mm. Nonetheless there are a few concepts that can provide a good tradeoff between size and performance. A good tradeoff between compactness and Q-factor can be provided by (a) strongly coupled lines based resonators and (b) folded quarter-wave resonators, which are analyzed in more detail next.

4.3.1 Strongly-Coupled Lines Based Resonator

The schematic view of the strongly coupled lines based resonator is illustrated in Fig. 4.4. The resonator is build by two centrally suspended strongly coupled transmission lines of equal length that are short-circuited at the opposite

ends of a conductive enclosure. This pair of strongly coupled transmission lines acts as a single low frequency resonator. The model has been simulated

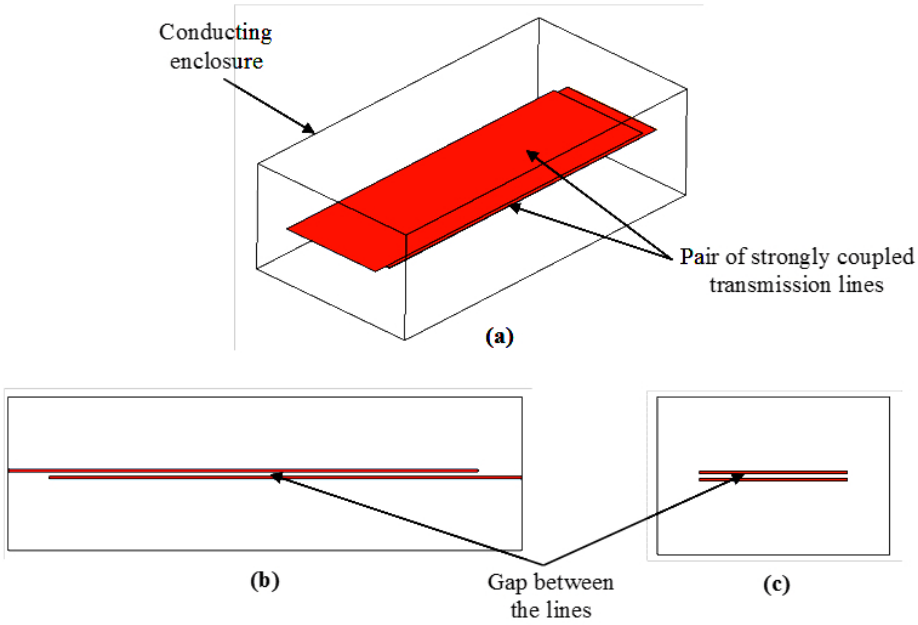


Figure 4.4: Strongly coupled lines based resonator: (a) perspective view (b) side view (c) front view. Courtesy: UNIPG.

by CST Microwave Studio and Ansoft HFSS considering gold for the metallic surface. According the simulation it is possible to realize a resonator at 2 GHz having a Q-factor of 450 in a conductive enclosure of 13x6x4 mm^3 and (12x5 mm^2 footprint). In this case the parameters that effects the resonant frequency are:

1. the conductive enclosure height (i.e. the distance between transmission line pair and upper and lower ground planes) and it is not possible to reduce the enclosure height (e.g. 4mm) for a given filter frequency band.

2. the "space/gap" (e.g. 200 μm) between the lines which form the mutual capacitance or the coupling between the two transmission lines.

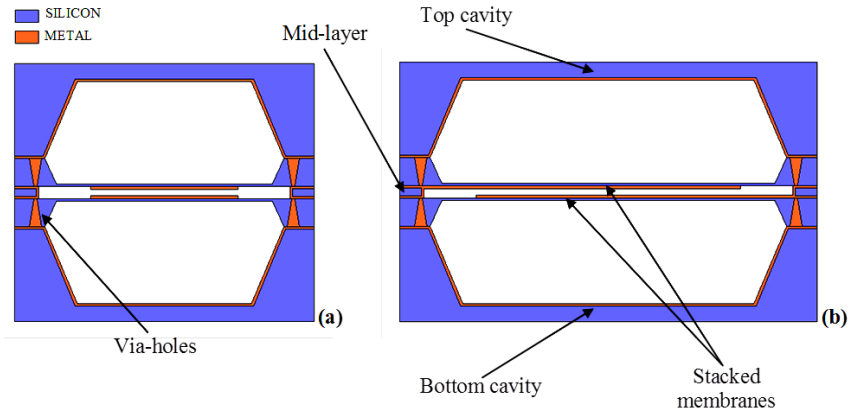


Figure 4.5: Possible realization of the strongly coupled transmission line resonator using multiple stacked bulk-micromachined layers: (a) side view (b) front view. Courtesy: UNIPG.

The resonator structure of Fig. 4.4 can be realized by using multiple stacked bulk-micromachined layers, as presented in Fig. 4.5. The transmission lines are supported by two bulk micromachined Si membranes. A mid-layer is used to realize the capacitive gap between the lines while the ground planes are realized by the upper and lower metalized cavities. Gold plated via holes are realized all around the membrane in order to provide the electrical connection between the layers.

While strongly-coupled lines based resonators are very compact in size and provide reasonable Q-factors but the main shortcoming is their sensitiveness to the gap spacing between the lines. As an example it has been verified that in the case of 200 μm gap spacing a tolerance of ± 2 μm can imply at least a 20 MHz shift of the resonance frequency. This type of large deviation is not acceptable since it would shift and deteriorate the filter response especially when the deviation is not uniform among the filter resonators. Practically tolerances higher than ± 2 μm should be considered for such a structure due to uncertainties in the technological processes as well as possible vibrations of the thin membranes. Therefore in this case a high sensitivity makes the initially proposed filter design unsuitable for the present project.

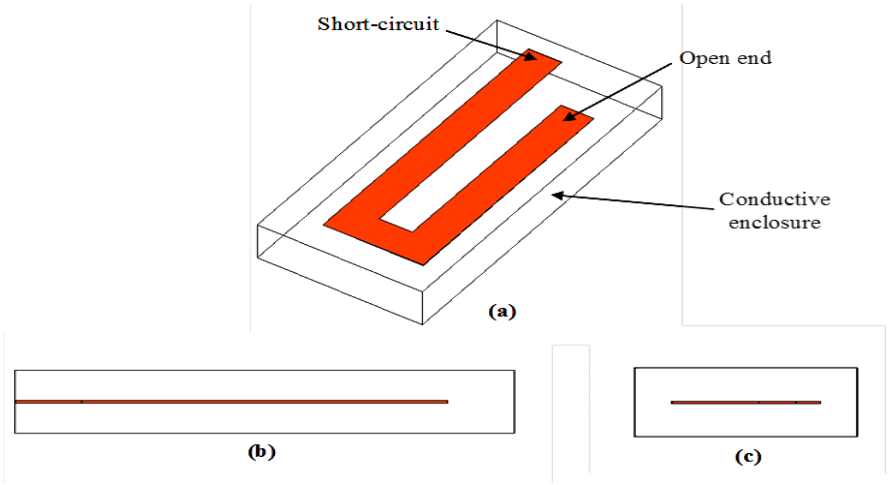


Figure 4.6: U-shape folded quarter-wave resonator: (a) perspective view (b) side view (c) front view. Courtesy: UNIPG.

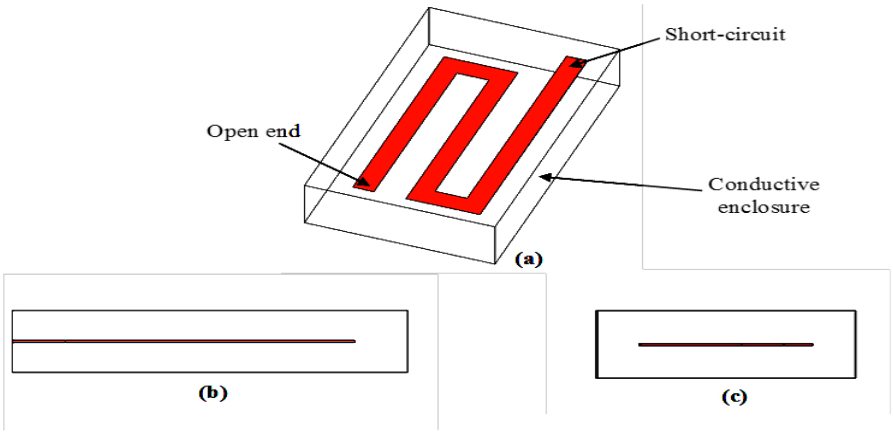


Figure 4.7: S-shape folded quarter-wave resonator: (a) perspective view (b) side view (c) front view.

4.3.2 Folded Quarter-Wave Resonator

Quarter-wave length resonators combine the advantage of reduced size and a good stop-band rejection with a good tradeoff for the Q-factor. In addition their design is very robust. Several folded resonator solution realized in conventional planar or LTCC technology are reported in [41–43] [83–85]. For the present application U-shape and S-shape folded quarter wave resonators

can be used. The structures of U and S-shape quarter-wave length resonators are illustrated in Fig. 4.6 and 4.7. The folding in a U and S-shape reduces clearly the occupied area with respect to a conventional inline resonator and provides a more favorable square shaped foot print. In both structures one end of the resonator is short-circuited, i.e. directly connected to the side wall of the conductive enclosure, while the other end is open-ended. To reduce the overall circuit size, the length of resonator is shortened to $\lambda/4$.

Unlike in the case of strongly coupled lines resonator the resonance frequency of folded quarter-wave resonator is independent of the conductive enclosure height. Instead the enclosure height directly affects the Q-factor, i.e. the smaller the enclosure height the smaller the Q-factor. However the resonance frequency of the folded quarter-wave resonators is determined by their length which is not so sensitive to the manufacturing tolerances as the gap spacing of the strongly-coupled lines based resonators. The resonator structures presented in Fig. 4.6 and 4.7 can be realized by using a single bulk-micromachined layer. Since in this case no small gap spacing is used to realize capacitive elements, possible vibrations of the membrane dimensions can produce only a minor effect on the response of the filter. In the end compact size and insensitivity to manufacturing tolerances makes U and S shape resonators be the optimum choice for the L/S band filter design. In addition by using shapes for the resonator (e.g. U or S) shapes different footprints and Q-factors can be obtained by design.

4.4 Conceptual Design of L/S Band Filter

As discussed above the L/S band filter can be realized by using four folded quarter-wave resonators. The S-shape resonator is favoured because it has a square footprint providing a uniform area occupation in both planar directions. Two pairs of resonators can be realized on different stacked bulk-

micromachined layers, thus obtaining a compact multilayer micromachined structure. Fig. 4.8 shows a prospective view of a 4^{th} order L/S band filter employing S-shape resonators.

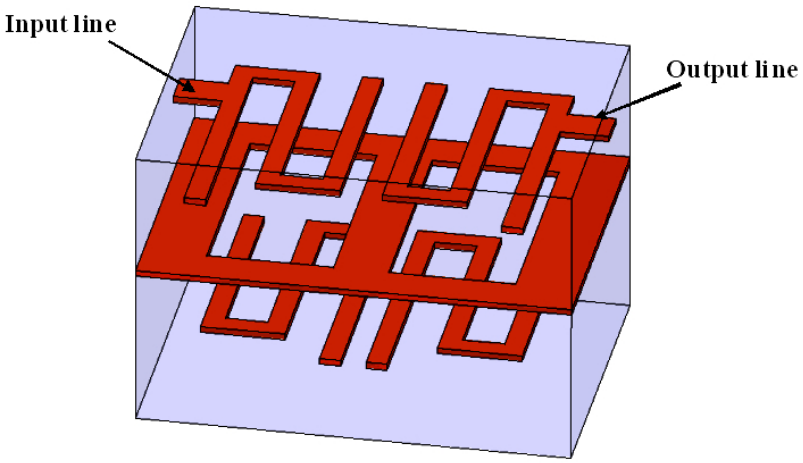


Figure 4.8: Fourth order filter using S-shape folded quarter-wave resonators. Courtesy: UNIPG.

Two pairs of resonators are realized on two different membrane layers; a third membrane layer is located between the two resonator layers to realize a common ground plane and to provide the proper couplings between the resonators. The two resonators on the lower layer are magnetically mutually coupled by means of their short-circuited terminations while the other two resonators on the upper layer are electrically coupled to each other by means of their open-ended terminations. The latter enables a negative cross-coupling between the first and the fourth resonator, thus obtaining the required filter topology reported in Fig. 4.1(d).

In this case preliminary HFSS simulations demonstrate that the resonator structure and the coupling mechanisms are suitable for the implementation of the required elliptic filtering function.

4.5 Preliminary HFSS Design and Simulation of S-shape $\lambda/4$ TEM Mode Resonator

A two time folded S-shape $\lambda/4$ TEM resonator for L/S band filter is shown in Fig. 4.9. The resonator is realized on a 10 μm silicon membrane and enclosed in a shielded cavity. The resonant frequency of the resonator is determined by the length (l) whereas the Q-factor of the resonator depends on the shielding cavity height (b) and the resonator width (a) and not on the conductive enclosure height (i.e. the distance between the resonator and upper and lower ground planes).

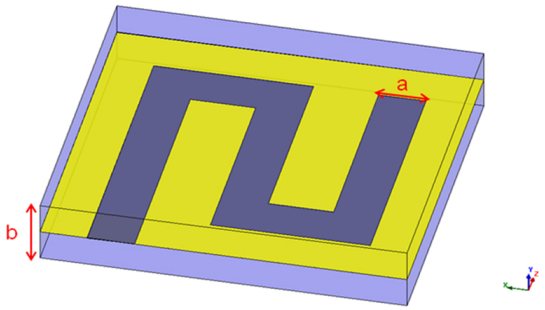


Figure 4.9: Two-time folded quarter-wave resonator at 2 GHz. Courtesy: UNIPG.

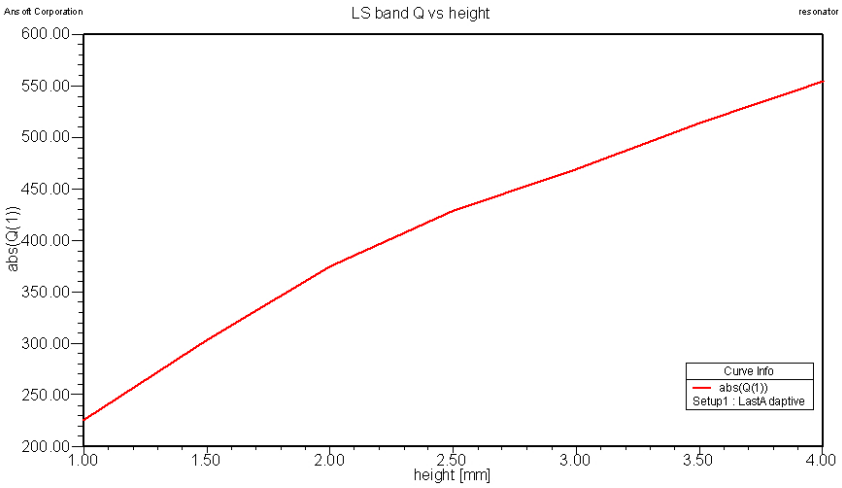


Figure 4.10: HFSS simulated Q-factor vs height of two-time folded quart-wave resonator at 2 GHz. Courtesy: UNIPG.

HFSS simulated Q-factor vs cavity height is given in Fig. 4.10. The simulation shows that the proposed cavity height of 3 mm provides a simulated Q-factor of about 450 at 2GHz. In these calculations a metallization thicker than 5μm (3 times the gold skin-depth at 2 GHz) is assumed to prevent undesired ohmic losses. In order to increase the mechanical stability, a 10 μm thick silicon membrane ($\delta = 0.005$) is foreseen to support the resonator. The obtained characteristics make the resonator suitable for filter design and fabrication. Therefore the preliminary design of 4^{th} order L/S band filter is based on S-shape resonator shown in Fig. 4.9.

4.6 Preliminary Design of 4^{th} order L/S Band Filter

As describe earlier in Subsection 4.2.3 the L/S band filter can be realized with a 4^{th} order filter topology, see Fig. 4.1(d), by employing folded quarter-wave resonators on silicon membranes. All ESA requirements can be fulfilled by this topology except for the insertion loss flatness (A4) and group delay variations (A6), refer to Table 4.2. Another possibility to satisfy all ESA requirements is to adopt a 6^{th} order filter topology with resonators with a Q-factor of 300 and a configuration shown in Fig. 4.3(d). In contrast to the 4^{th} order filter the 6^{th} order filter in multilayer technology involves a large number of layers to be stacked and this increases the fabrication complexity and also requires high manufacturing and assembly tolerances. It is therefore logical, to address the efforts first towards the design and fabrication of a 4^{th} order filter, in order to test the technology on a less complex configuration. Therefore a 4^{th} order filter with two symmetric transmission zeros is preliminary designed employing multilayer folded quart-wave resonators. A prospective view of the 4^{th} order filter is illustrated in Fig. 4.11.

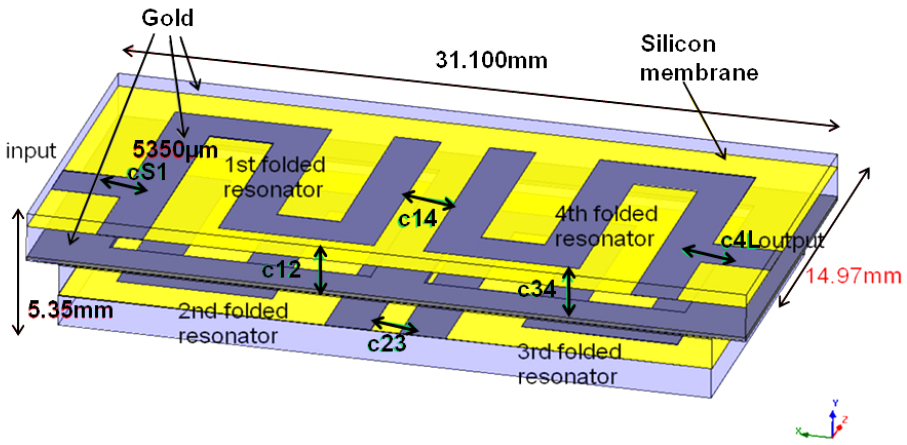


Figure 4.11: HFSS design of LS band 4^{th} order filter (perspective view). Courtesy: UNIPG.

The filter employs six 500 μm thick standard Si wafers. To reduce the filter size the resonators are distributed on four different dielectric layers while the other two layers are used for closing the filter. An opening in a common ground plane determines the direct coupling between resonators on different layers: 1-2 and 3-4 couplings (c12, c34). Resonators on the same layer are coupled by controlling their distances: 2 - 3 magnetic direct coupling and 1-4 electric cross coupling (c23, c14); the opposite sign of these couplings allow the symmetrical transmission zeros to be generated. Also in this case the filter structure is symmetrical.

The upper half-height of the first resonator is lower than the others (0.65mm instead of 0.5mm) due to the constraints introduced by the input transition design (described in the following section). The input coupling (as well as the output coupling) is realized by means of a direct connection to the first (last) resonator. The input line distance from the short-circuited end of the resonator determines the coupling. Total filter sizes without input/output transition are given in Fig. 4.11 (14.97x31.1x5.35 mm^3). The broadband filter simulation is shown in Fig. 4.12.

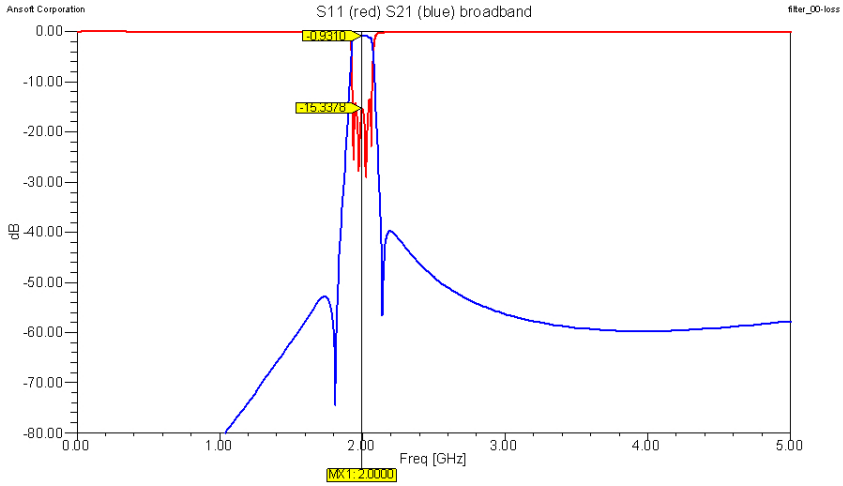


Figure 4.12: Broadband HFSS simulation of L/S-band 4^{th} order filter. Courtesy: UNIPG.

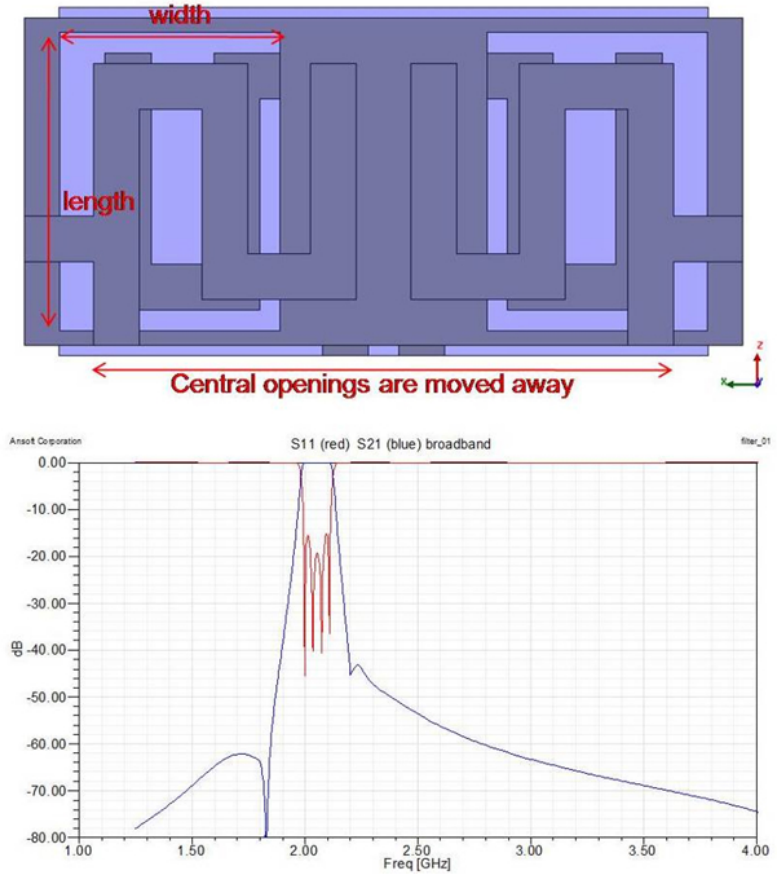


Figure 4.13: Top view and HFSS simulation of optimized openings in central ground plane. Courtesy: UNIPG.

A cross-coupling between diagonal resonators has been introduced by the design team in the configuration shown in Fig. 4.11. These additional cross-couplings introduce the asymmetric behaviour of response shown in Fig. 4.12. In order to reduce this undesired effect it is possible to increase the distance between the two symmetric openings in the central ground plane (Fig. 4.11), so as to reduce the cross-coupling between diagonal resonators. From preliminary results apparently it is not possible to completely avoid this undesired couplings: in fact, also by putting the opening edges at the cavity walls and reducing the width/length aspect ratio, see Fig. 4.13, the undesired asymmetrical behaviour is still there.

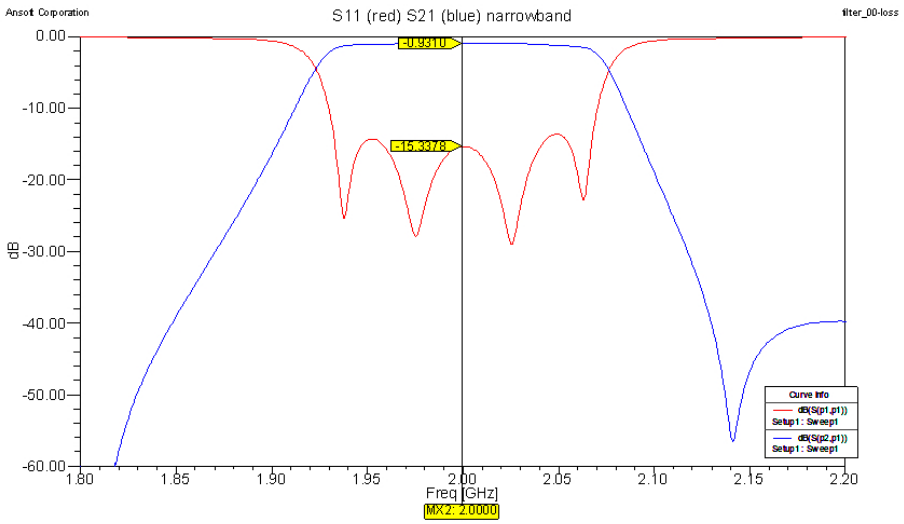


Figure 4.14: Narrowband HFSS simulation of preliminary LS-band 4^{th} order filter. Courtesy: UNIPG.

The HFSS simulation results shown in Fig. 4.12 fulfil all ESA compliance matrix requirements of Table 4.1. Narrowband filter HFSS simulation, IL flatness and group delay behaviours are depicted in Fig. 4.14, Fig. 4.15 and Fig. 4.16 respectively.

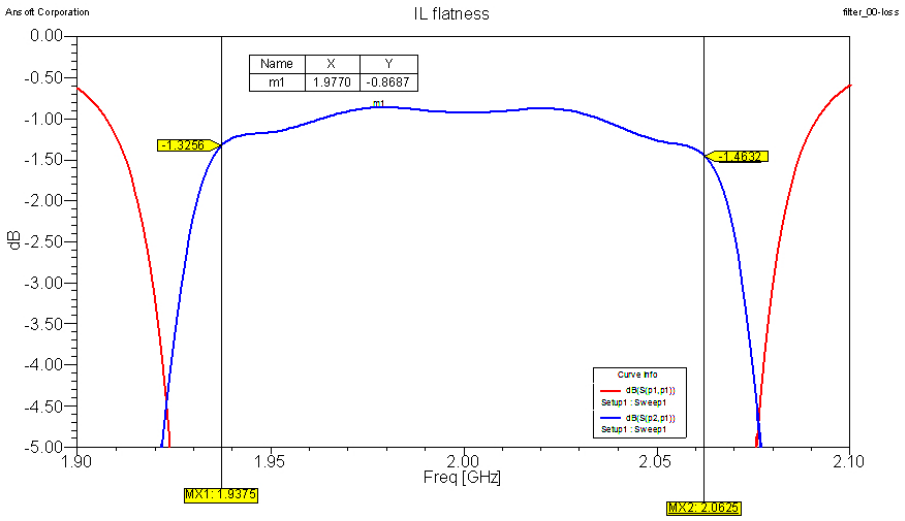


Figure 4.15: IL flatness HFSS simulation of preliminary LS-band 4^{th} order filter. Courtesy: UNIPG.

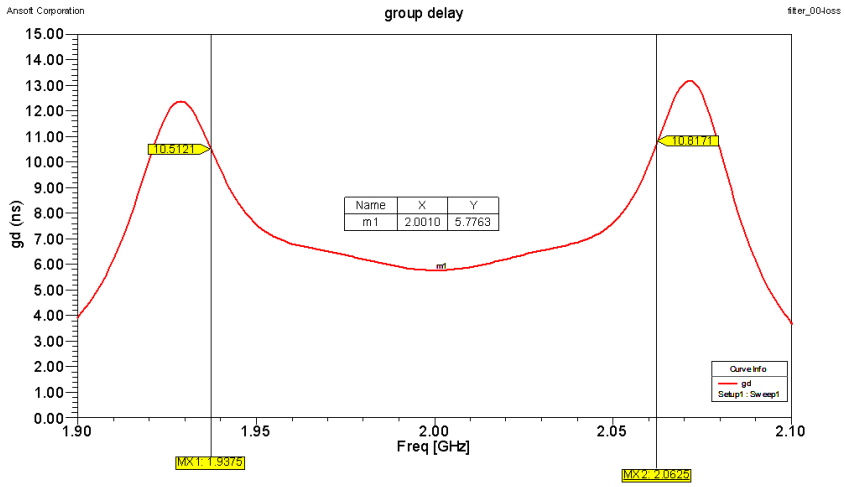


Figure 4.16: L/S band filter transition for SMT compatibility (perspective view). Courtesy: UNIPG.

4.7 Input/Output Coupling of L/S Band Filter for SMT Compatibility

This section describes the proposed input/output couplings for L/S band filter, shown in Fig. 4.11, that provide the surface mount compatibility. These

input/output couplings represent an additional structural element of the filter that has to be realized with the process. Proportionally small input/output coupling can be obtained by using coupling apertures on the top or bottom side of the resonator cavity. In order to achieve suitable input/output coupling to the resonator, a direct connection between the feeding lines and the resonator is desirable. In other words the feeding lines should be patterned on top of the external surface of the filter and connected to the resonators through vertical via holes, a structure already foreseen in the process.

A sketch of a possible input/output transition for the L/S band filter is depicted in Fig. 4.17. One single via hole allows connecting the top microstrip feeding line with the first resonator inside the cavity. The relative permittivity mismatching between silicon and air can be compensated by widening the gold line at the silicon-to-air interface, thus reducing characteristic impedance of the line. HFSS full wave simulations show that a return loss better than 20 dB can be obtained with a described transition.

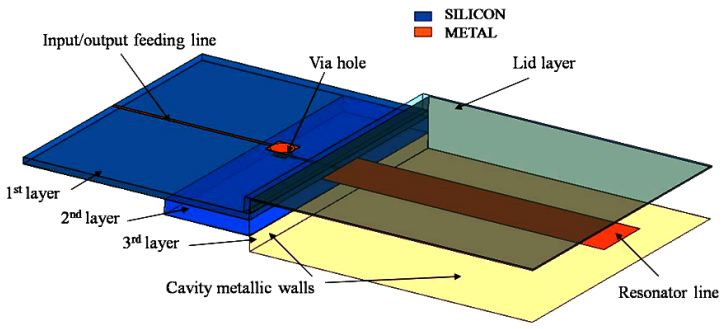


Figure 4.17: SMT compatibility of L/S band filter transition (side view). Courtesy: UNIPG.

An additional silicon layer placed on the top layer (where the feeding lines are patterned) realizes the upper enclosure of the first resonator cavity. The filter can be surface mounted by using solder balls larger than the silicon en-

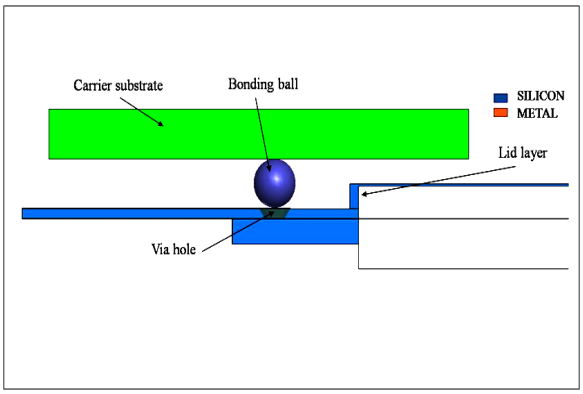


Figure 4.18: SMT compatibility of L/s band filter transitions(side view). Courtesy: UNIPG.

closure thickness. As an example by using for the lid layer and the resonator cavity a thickness of 0.2 mm and 0.5 mm respectively, a distance of 0.6 mm between the resonator line and the upper metallic cavity wall can be achieved. Such a cavity height allows an acceptable Q-factor. Fig. 4.18 shows how a solder ball with a diameter larger than 0.5 mm allows the compatibility with SMT.

An advantage of proposed feed solution is that the input/output filter coupling does not depend on the matching of the external input/output lines but only on the position of the feeding line with respect to the folded resonator ("d" in Fig. 4.19, [44]).

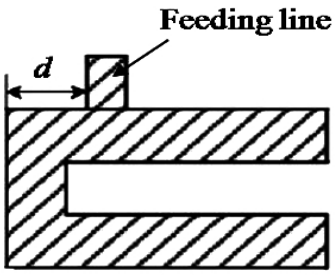


Figure 4.19: Coupling of the first resonator with its feeding line [44] (top view). Courtesy: UNIPG.

In this way the input/output interconnections and the filter input coupling mechanism are separated, thus making the filter less sensitive to manufacturing tolerances and properties of the carrier substrate. On the contrary feeding solutions based on coupling apertures not only allow smaller couplings that limit the filter bandwidth, but also have a filter coupling that depends on the matching of the input interconnection, position and dimensions of the solder balls and characteristics of the carrier circuit.

4.8 Resonator Optimization

Once the general concept of the filter, the resonators and the feed lines have been defined the single $\lambda/4$ TEM mode resonator could be optimized. In Fig. 4.20 a single quarter-wave resonator has been sketched and the important relevant parameters are defined, which are:

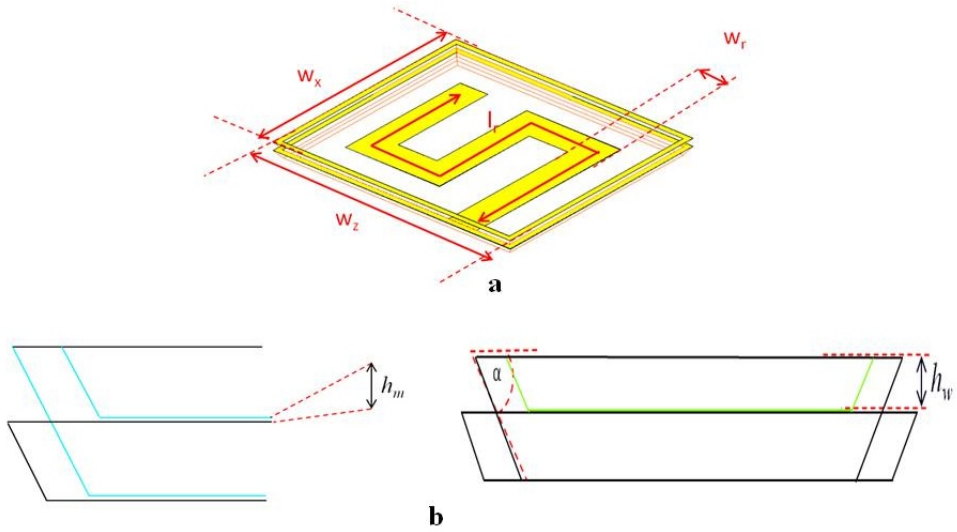


Figure 4.20: Quarter wave resonator at 2 GHz. Prospective view (a) and section view (b). Courtesy: UNIPG.

$\mathbf{w}_z$, $\mathbf{w}_x$ = cavity width along z and x axis.

$\mathbf{w}_r$ = resonator width

$\mathbf{l}_r$ = resonator length

$\mathbf{w}_z$ = cavity height

$\mathbf{h}_m$ = membrane height = thickness of the metalized silicon membrane inside the cavity.

$\mathbf{d}_f$ = width of the folding opening

α = TMAH etching angle.

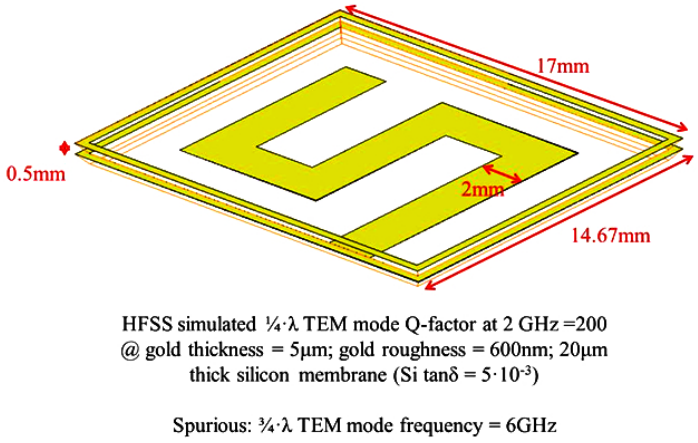


Figure 4.21: Optimized Cavity dimensions for 500 μm thick Si layer. Courtesy: UNIPG.

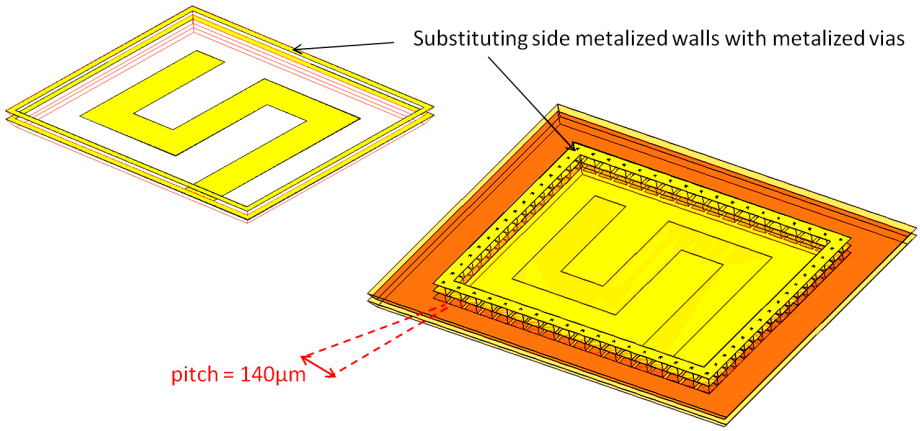


Figure 4.22: Analysis considering actual via lines instead of ideal metal walls. Courtesy: UNIPG.

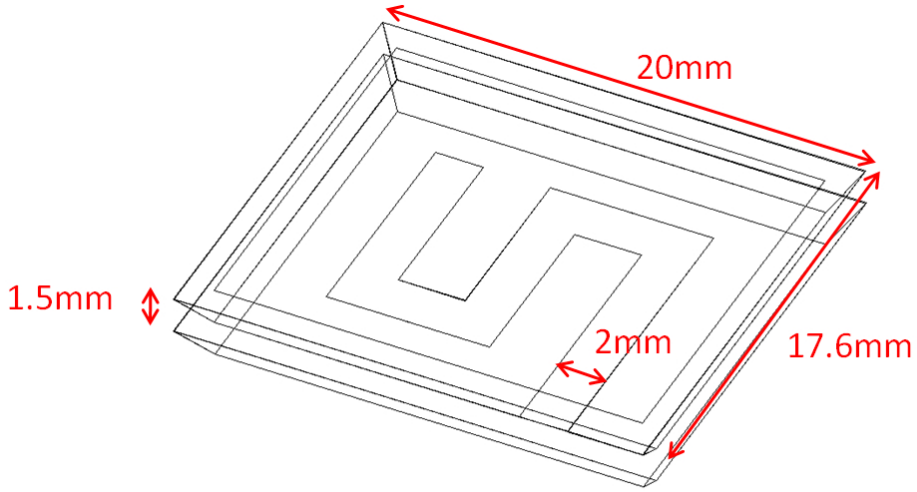


Figure 4.23: Optimized Cavity dimensions for 1500 μm thick Si layer. Courtesy: UNIPG.

The resonator Q-factor was calculated for different values of (a) resonator width (w_r), (b) membrane height (h_m). However the results show no variation in terms of Q-factor (i.e. 200 at 2 GHz) for both parameters once these parameters were optimized for 500 μm thick Si layers. The final resonator geometry is shown in Fig. 4.21.

HFSS simulations were also performed to calculate the Q-factor in case the ideal metal wall is replaced with equally spaced 140 μm TSV's as shown in Fig. 4.22. The simulation showed no variation of the Q factor although a shift of 1% (10 MHz) in frequency was observed. A similar analysis was repeated for 1500 μm thick Si layers and a resonator with dimensions presented in Fig. 4.23. In this case using metalized via's instead of metal walls the HFSS simulated $\lambda/4$ TEM mode is 0.5% (10 MHz) higher and Q remains unchanged.

4.9 Tolerance Analysis

As in the case of the Ka band filter a tolerance analysis has also been carried out on single L/S band filter's resonator to assess the accumulated variation in resonance frequency with respect to variations in: (a) wafer height, (b) membrane thickness, (c) sidewall angle

First each of these parameters were carefully examined to estimate the tolerances in manufacturing, assembly and alignment for both 500 μm and 1500 μm thick Si wafers. Table 4.4 and Table 4.5 reports the simulated results of the tolerance analysis for 500 μm and 1500 μm thick Si wafers respectively.

Table 4.4: Tolerance analysis for 500 μm thick Si layer.

Parameter	**Tolerance**	**Frequency Shift**
Wafer Height	$\pm$ 2% (i.e. $\pm$ 10 μm)	$\pm$ 0.2% (i.e. $\pm$ 4 MHz)
Membrane Height	$\pm$ 2.5 μm	$\pm$ 0.25% (i.e. $\pm$ 5 MHz)
Etching Angle	$< \pm 1^\circ$	$\pm$ 0.25% (i.e. $\pm$ 5 MHz)

Table 4.5: Tolerance analysis for 1500 μm thick Si layer.

Parameter	**Tolerance**	**Frequency Shift**
Wafer Height	$\pm$ 2% (i.e. $\pm$ 30 μm)	$\pm$ 0.25% (i.e. $\pm$ 5MHz)
Membrane Height	$\pm$ 2.5 μm	$\pm$ 0.15% (i.e. $\pm$ 3 MHz)
Etching Angle	$< \pm 1^\circ$	$\pm$ 0.25% (i.e. $\pm$ 5 MHz)

4.10 Sensitivity to Temperature and Layer Misalignment

In similar way the sensitivity with respect to temperature variations in the operating temperature range from -10°C to 75°C was estimated. Si has a CTE of 2.5x10^{-6} K^{-1}, by assuming a maximum resonator length of 20 mm

the maximum change in length is 5 μm. Such a variation is negligible and can be neglected in the L/S band filter design.

The sensitivity to possible misalignments between different stacked wafers had also been evaluated: assuming an expected misalignment error $< \pm$ 5 μm the maximum resonator length variation is 5μm (lr = 0.013%). Again the associated frequency shift is negligible (<1 MHz).

4.11 Monte Carlo Analysis

A statistical tolerance analysis on random sampling is based on the Monte Carlo method. It is an alternative method for calculating probability, mean and standard deviation for the analyzed item. The Monte Carlo analysis was performed on the L/S band filter circuital model resonators to get an idea of the filter robustness. Maximum resonant frequency variations of $\pm$ 5 MHz ($\pm$ 0.25%, i.e. the worst variation) was considered for both the 500 μm and 1500 μm thick designs. As depicted in Fig. 4.24 the 4^{th}-order filter seems to be pretty robust since a yield = 62.5% has been obtained.

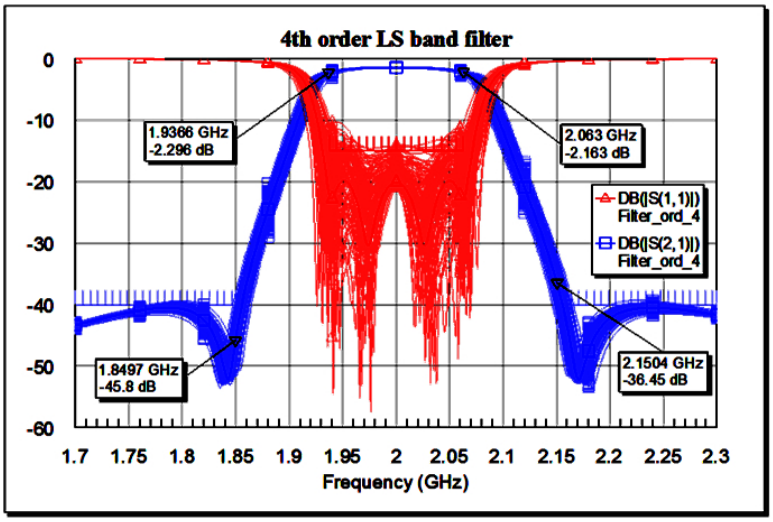


Figure 4.24: Monte Carlo analysis for the L/S band filter considering a maximum resonant frequency variation of $\pm$ 5MHz. 62.5% yield has been obtained. Courtesy: UNIPG.

In conclusion the tolerance analysis shows acceptable robustness for resonators realized on both 500 μm and 1500 μm thick layers. The estimated yield of a 4^{th}order filter using either 500 μm or 1500 μm thick Si layers is roughly 60%.

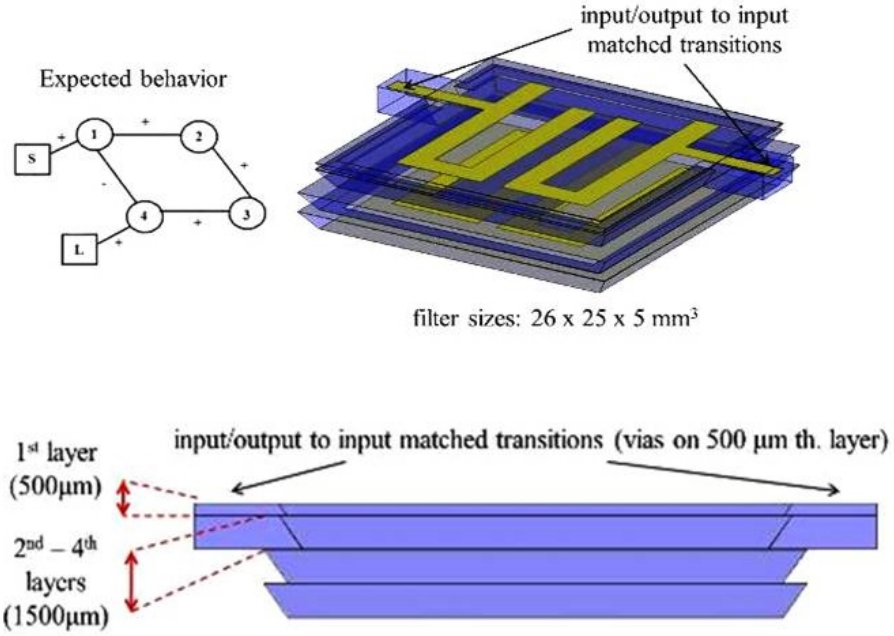


Figure 4.25: Sketch of the 4^{th} order filter model in HFSS on 500 μm thick Si layers accounting for the non-vertical cavity walls. Courtesy: UNIPG.

4.12 Final Design of The 4^{th} order LS Band Filter on New Technological Concept

The layout and expected performance of the 4^{th} order pseudo-elliptic is illustrated in Figs. 4.25 and 4.26. The filter is realized by stacking three 1500 μm thick and one 200 μm thick Si wafer. All FBK technological constraints have been taken into account, as well as material loss. The simulated $\lambda/2$ TEM mode Q factor is 750. U-shaped $\lambda/4$ resonators are used in order to have a square footprint. The presented design qualify all requirements of ESA except the group delay variation which 3 ns instead of 1.5 ns.

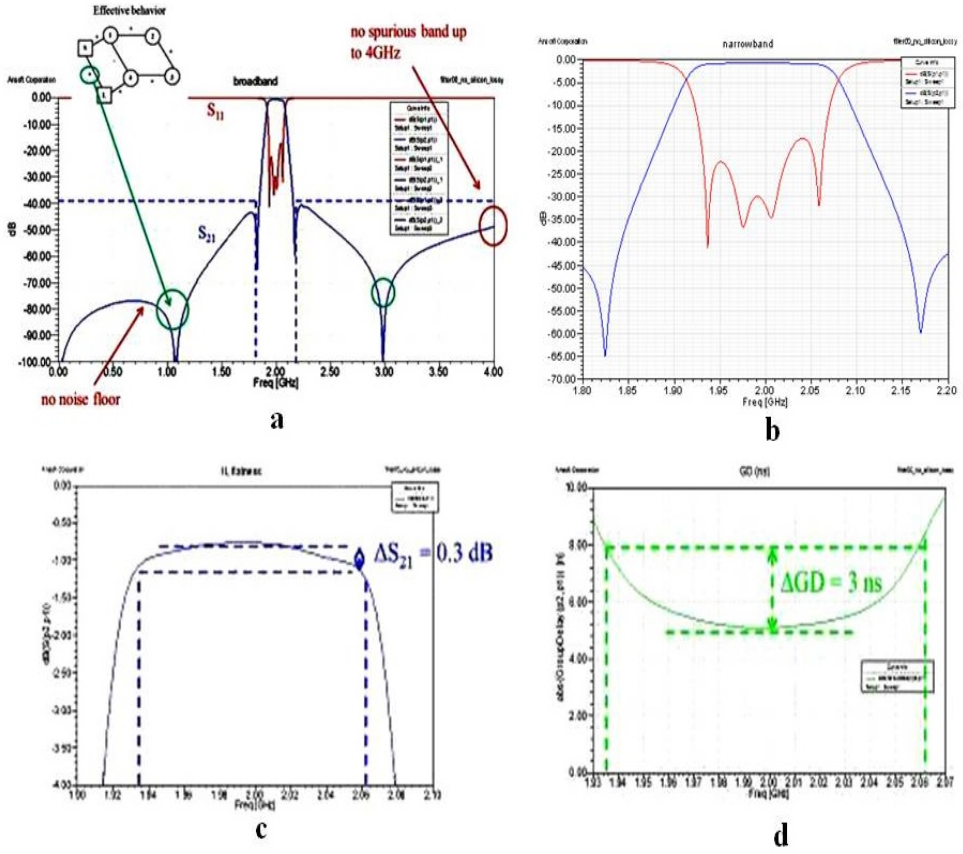


Figure 4.26: Performance of the 4^{th} order filter. (a) wide band results, (b) narrow band response, (c) Insertion Loss flatness (d) Group delay. Courtesy: UNIPG.

4.13 L/S Band Filter Test Structures

In the development of fabrication technologies for complex structures it is preferable to use simpler structures as test structures in order to rapidly analyze and gain insight to the factors affecting performance and reliability of the device and also to identify the main process constraints. Working with simpler structures also allows to develop and modify the technological modules and process steps easily. Therefore to make a technological run simpler test structures presented in Figs. 4.27 - 4.29 were designed and fabricated on 500 μm thick Si wafers instead of 1500 μm.

4.13.1 LS 01: Back-to-back Input Transition with Metalized Via

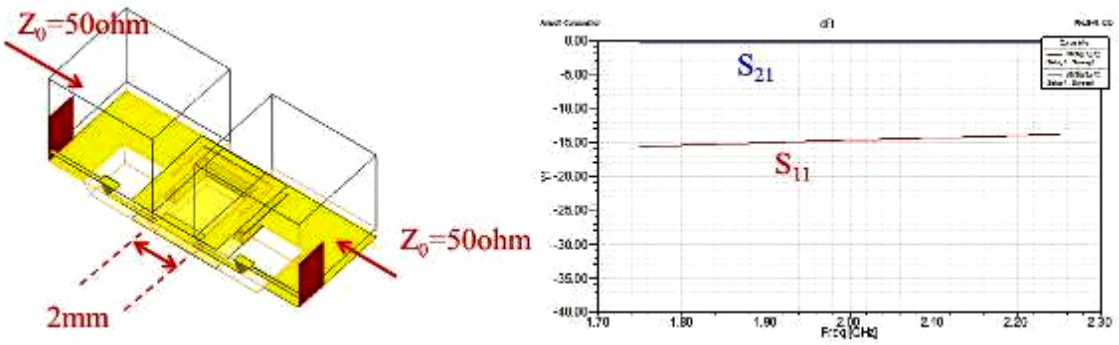


Figure 4.27: Layout and expected performance of test Structure LS 01: back to back input transition. Courtesy: UNIPG.

4.13.2 LS 02: 1-Port Resonator (S11 measurement and Q estimation)

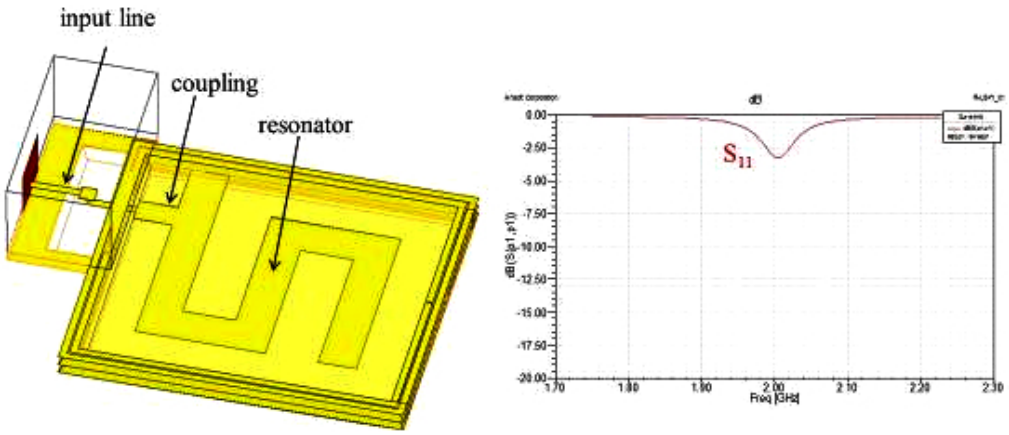


Figure 4.28: Layout and expected performance of test Structure LS 02:port resonator (reflection type measurements will be performed. Courtesy: UNIPG.

4.13.3 LS 03: 2^{nd} Order Filter(Test of internal coupling)

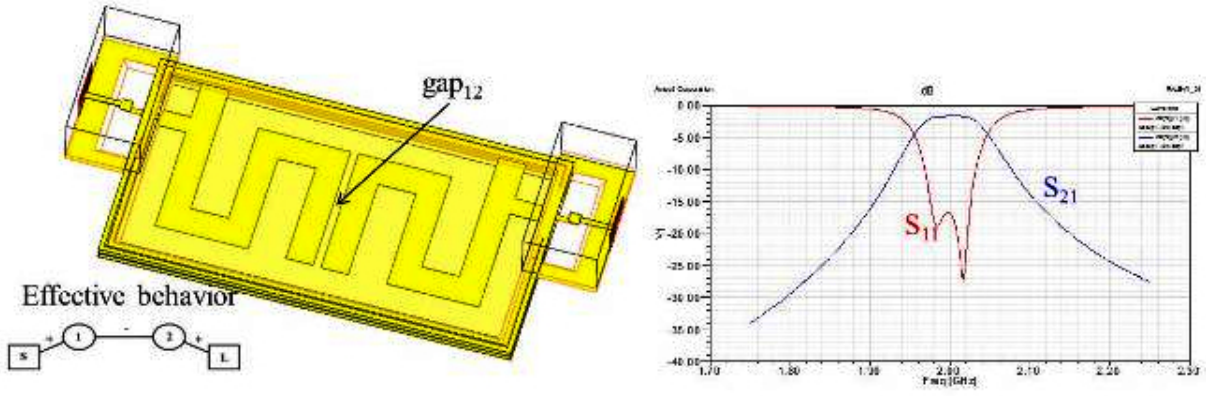


Figure 4.29: Layout and expected performance of test Structure LS 03: 2nd order Filter with a negative sign central coupling (capacitive coupling). Courtesy: UNIPG.

4.14 Fabrication of L/S Band Filter

This section gives an overview on the technology concept developed and optimized for the fabrication of test structures of L/S band filters presented in Sections 6.1 - 6.3. Two types of technology concepts were developed initial one for the fabrication of the preliminary design of the L/S band filter, the other one for the fabrication of the final prototype design on 1500 μm thick Si wafers. The idea behind the development of these technology concepts was to create the test structures with minimal development efforts and identify and rectify any shortcomings in the fabrication process. Therefore both (initial and revised) technology concepts are based on a modular approach that requires a minimum development time for each individual module.

4.14.1 Evolution of FBK Technology Concept for L/S Band Filters

The initial design of L/S band filter involved membrane supported electrodes, The connection between feeding lines and the first cavity resonator is pro-

vided by a via hole. Fig. 4.30 summarizes the technology concept introduced for the preliminary design of the L/S band filters.

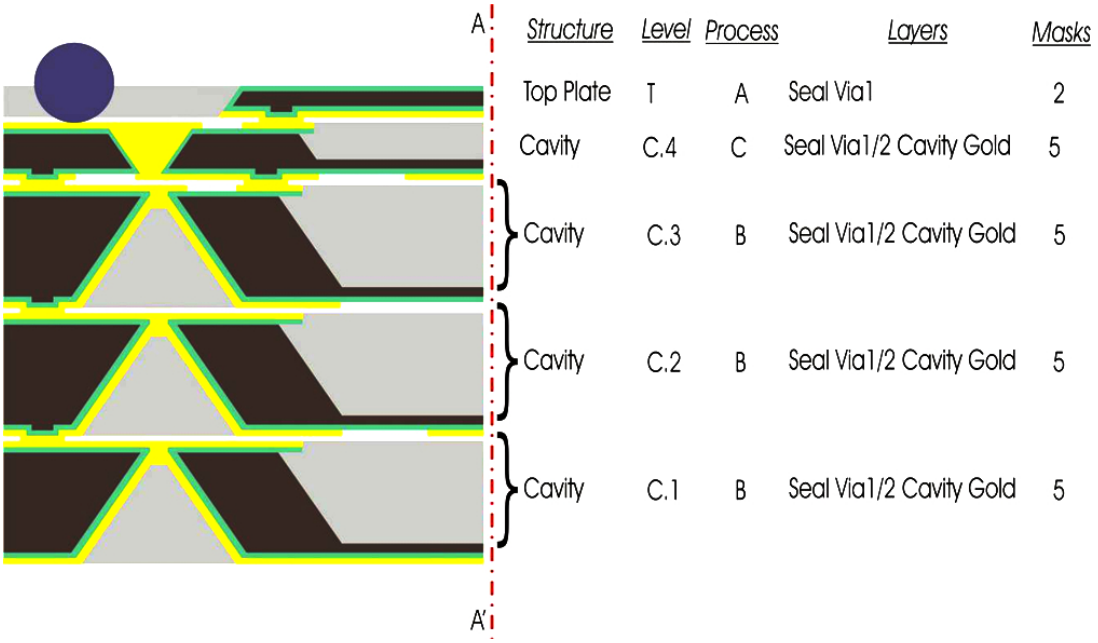


Figure 4.30: Sketch of the cross section of the L/S band filter. Only one half of the structure is shown. A - A' is the symmetry plane.

The figure shows only one half of the structure, which is symmetrical with respect to the vertical axis. In this approach the device is build up by 5 modules (wafers), which are bonded together by metal to metal thermocompression bonding. This concept requires the following three different processes to build the structure presented in Fig. 4.30.

Process A: has two mask layers and needs 200 μm HR <100> p type silicon wafers as substrates to build the top plate of the structure which provides the closure and an access to the feed lines.

Process B: based on 6 mask levels that provide membrane supported electrodes together with diaphragms and conductive viaÓş for the ground (and lateral shielding). This process required 1500 μm thick, <100>, p or n type HR grade silicon wafers for the final device. But for the first prototypes silicon wafers with standard thickness of 500 μm would be used to test the

technology.

Process C: also based on 6 mask layers providing membrane supported electrodes, a top cavity and conductive vias for the signal feed lines. Also for this process 1500 μm thick, <100>, p or n type HR grade silicon wafer are required.

With the development of the L/S band filter design the technology concept for the fabrication also evolved in order to meet the requirements.

4.14.2 Revised Technology Concept for L/S Band Filters

The revised technology concept for the 4^{th} order L/S band filter presented in Fig. 4.25 is summarized in the cross sectional view of Fig. 4.31. The figure shows only one half of the structure, which is symmetrical with respect to the vertical axis. As before, the revised concept of the complete filter is also build up by five modules, and vertically bonded by metal to metal thermocompression bonding but the revised version differs in many aspects from the previous one.

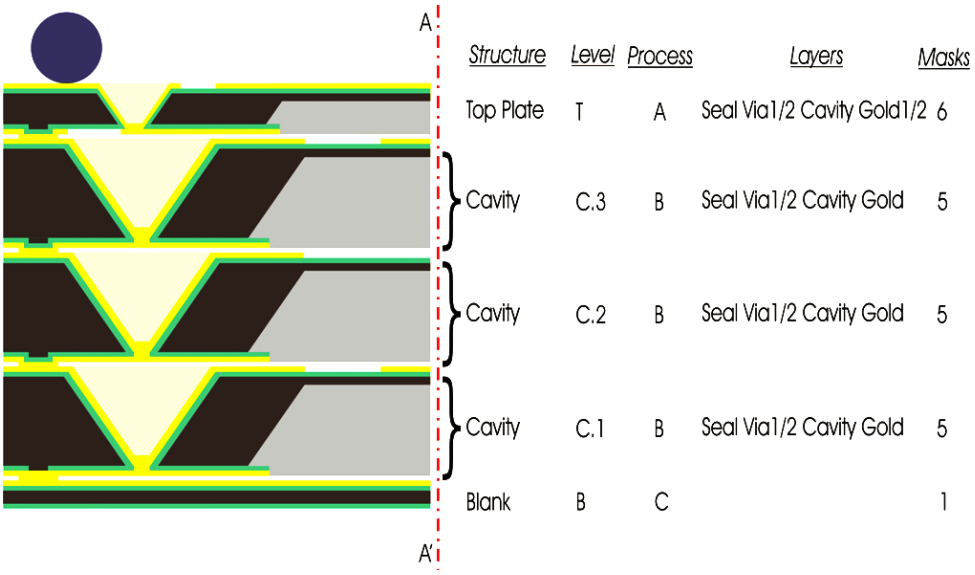


Figure 4.31: Sketch of the revised cross section of the L/S band filter. Only one half of the structure is shown. A - A' is the symmetry plane.

Starting from the bottom this revised concept is similar to the concept for Ka band filters that makes use of a blank bottom plate. The next major change is in the middle plates. In the revised concept the via holes are etched from the front side of the wafer and the deep cavity is etched from the backside. The biggest change occurs in the top plate which is now fabricated with the same process as the middle plates, i.e. it has a vertical via similar to the middle planes and a bottom cavity as well. This eliminates the need for an additional top plate and allows the solder bumps to be placed directly on top of the structure.

The great advantage of this concept is that only one fabrication process is needed for all parts of the filter instead of the three originally planned. In addition this arrangement also provides simplified electrical connections.

4.15 Fabrication Process Description

To test both the technology concept and the design methodology for the first fabrication cycle a simplified structure has been selected as shown in Fig. 4.32. All layers are fabricated out of 500 μm thick FZ silicon wafers, i.e. already in-house available wafers.

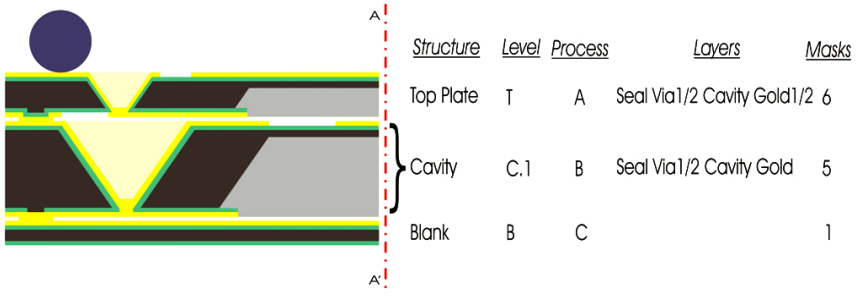


Figure 4.32: Sketch of the simplified cross section of the L/S band filter. Only one half of the structure is shown. A - A' is the symmetry plane.

The fabrication process starts with the crystal alignment module, details are given in **Appendix "C"**, for this purpose a 120 nm thin thermal oxide is

grown in steam at 975°C. In the next step markers for crystal alignment are defined by lithography and etched. After that in order to allow the precise identification of the crystal alignment $\approx$ 20 μm deep cavities are etched with a short anisotropic etch with TMAH at 90°C. In a subsequent step the sealing ring on the wafer backside is defined. This mask is aligned on the previously etched structures according to the individual off set of each wafer. The pattern is then transferred to the silicon by plasma etching with a DRIE recipe. A nominal step height of 2 μm has been chosen. Higher values can easily be obtained if necessary, see Fig. 4.33(a).

Next in order to build a hardmask for bulk etching of silicon on both side of wafers a 1 μm thick thermal oxide is grown in 385 minutes by steam oxidation at 975°C. This oxide is then coated by a 150 nm thick Si_3N_4 film deposited by LPCVD at 775°C, followed by an LPCVD medium temperature oxide deposition from Tertraethylortho-silicate (TEOS) at 718°C. This three layer coating forms the hard mask for the bulk silicon anisotropic etch. Then the hardmask at the wafer front side is patterned for TSVs and etched by dry etching till the silicon substrate is reached, as depicted in Fig. 4.33(b).

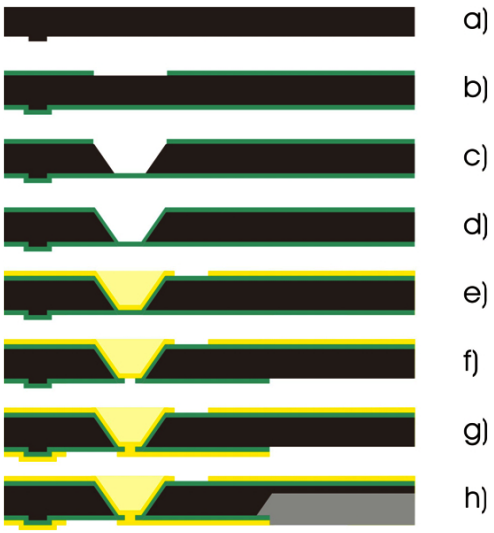


Figure 4.33: Processing sequence for the wafers of the L/S band filter based on the simplified cross-section of Fig 4.32.

Wet etching technique was employed to etch the via holes. For this purpose a 25% Tetra-Methyl-Ammonium-Hydroxide (TMAH):water solution was used and etching was performed in two steps. In the first step nearly 12 hours of etching at 90°C produced a ≈ 475 μm deep cavity which is measured in order to determine the precise etching rate. In a second step the cavity is deepened to the full wafer thickness with a little over etch. This exposes the bottom of the backside hardmask layer. Due to the small dimensions (less than 50x50 μm^2) the resulting membranes are sufficiently robust to tolerate the mechanical stresses during the last phases of the bulk-etch giving a very high yield of intact membranes, as illustrated in Fig. 4.33(c).

The fabrication proceeds by removing selectively the TEOS layer from the frontside with the help of buffered HF (hydrofluoric acid) and by covering the wafer backside with photo resist. After ashing the photo resist the nitride was stripped from the frontside with H_3PO_4 (phosphoric acid) at 150°C for 30 min, and during this etching the TEOS on the backside of the wafer protects the Si_3N_4 layer from etching. After stripping the front side thermal oxide the wafers were again oxidized for 385 minute in steam at 975°C in order to grow a 1 μm thick oxide layer on the sidewalls of the TSVs and on the wafer top. In order to reduce the trapped oxide charge at the interface with the silicon, the wafers are then annealed in nitrogen at 975°C for 1 h. This completes the isolation of the silicon substrate, as shown in Fig. 4.33(d).

In the following step the wafer frontside was coated with a seed layer. The seed layer was composed of chrome/gold/chrome (i.e. 2.5/25/2 nm thick) respectively. As in the case of the KaA and KaB processes the layers are deposited in a vacuum chamber by PVD with an e-gun without interrupting the vacuum. The first chromium layer acts as an adherence layer on the oxide for the gold layer, which otherwise would not adhere well to the substrate while the top chromium layer is the adherence layer for the photo resist, which adheres much better on an oxidized surface than on gold. The front

gold layer is than defined with a negative dry film. This masking layer defines the electrodes and the metallic closure of the cavity. The dry film resist is used because a standard resist would pool in the TSVs and led to a strongly inhomogeneous resist coating, while the lamination of the dry film is almost unaffected by the presence of the vias. After developing the dry film resist the top chrome layer was removed in the exposed areas with chromium etch (Balzers chromium etchant) and a 2.5 μm thick gold layer was plated from a cyanide based gold bath (Aurolyte 200) in a fountain plater from RENA. After the gold plating the resist mask was removed by wet etching with the proper solvent as well as the seed layer, which is removed with a sequence of chromium etch, gold-etch and chromium etch, as presented in Fig. 4.33(e).

Subsequently the via holes in the oxide on the wafer backside and the etch windows in the hardmask are defined by lithography and etched by oxide dry etching, as sketched in Fig. 4.33(f). These holes are needed in order to provide electrical connection to the top gold layer, while the etch window is required for the cavity etch. In this case the wafers can be processed with standard procedures because the thin membranes are very robust due to their small size.

Finally a second seed layer, identical to the first one, was deposited on the backside of the wafers and the pattern of the gold layer on the wafers backside for the ground plate was defined using standard resist for gold plating (AZ 1050). A 2.5 μm thick gold layer was deposited in the plater and the seed layer was removed afterwards as mentioned above, see Fig. 4.33(g).

After a quick dip in 2% HF acid that removes the native oxide in the etch window the deep cavities were etched with a 25% TMAH:water solution in two steps. A first etch of $\sim$ 11hours produces a $\sim$ 455μm deep cavity, which was measured in order to determine the precise etching rate. In a second step the cavity is deepened till $\sim$ 480 μm, leaving a 20 μm thick silicon membrane. In this way the resulting membranes are sufficiently robust to

tolerate the mechanical stresses during the last phases of the bulketch, as shown Fig. 4.33(h). Finally the wafers are annealed at 190°C for 30 min to sinter the gold layers.

4.16 Manufacturing of The Layers

The layout for the realization of the test structures is shown in Fig. 4.34. The wafer area is occupied by three design variants with only one repetition due to the large size. For fast and cost effective development of L/S band filters it was chosen to put different layers for top and middle plane on the same mask. Otherwise for the realization of the L/S filters at wafer level one has to fabricate each layer individually by using the same process but a specific mask set for each layer. This could have increased the cost, as two mask sets have to be acquired. The fabrication started by launching a first run under the name **"Process LSB1"**.

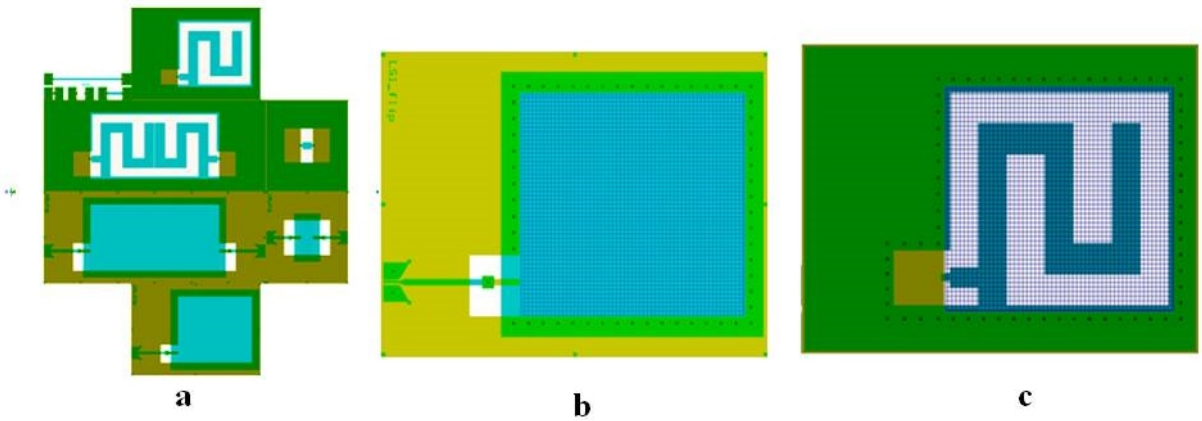


Figure 4.34: Layout for the LSB process for the top and middle plates of the filter. (a) wafer layout. The area is divided between three different filter types. The large size of the devices allowed only one repetition. (b) die layout of the LS1 top plate (c) die layout of the LS1 middle plate.

4.16.1 First Run (Process LSB1)

Like in the case of the KaA process also in this case the process flow described above was transcribed into a process sequence which resulted in 126 individual processing steps uploaded to the CAM program that controls the manufacturing of each wafer lot. For this first test run a total of 6 process wafers were selected together with 5 test wafers that are used to monitor the process sequence. As in the case of the KaA/B processes also in this case it was decided to include two splitting on the step height of the sealing ring, as reported in Table 4.6.

Table 4.6: Splitting scheme of run LSB1. The lot comprises a total of 6 wafers divided in two splits for different sealing ring height.

SPLITTING	**STEP**	**LOTS**					
		1			**2**		
		1	**2**	**3**	**4**	**5**	**6**
A	Std: substrate						
	HR substrate 500 μm	x	x	x	x	x	x
B	Sealing Ring 1 μm	x	x	x			
	Sealing Ring 2 μm				x	x	x

As starting substrates 500 μm thick high resistive (HR) 5000 Ω cm, p-type, <100> Si wafers were selected. Then the manufacturing followed the schedule described in the previous chapter. For defining crystal alignment marks a 120 nm thick masking oxide was grown and then the structures for the crystal alignment were patterned on the backside of the wafer and etched. After that a short anisotropic etch was performed in order to put into evidence the lattice planes.

Then, after stripping the mask oxide, the wafers were coated with PR and by the next lithography step the sealing ring was patterned on the bottom of the wafer. Also in this case two step heights were realized (1 and 2 μm) by a low roughness DRIE process for 45 sec and 1min 30 sec respectively.

After ashing and wet stripping the resist the sealing ring step heights were measured by a ZYGO optical profiler.

In the following step a hardmask, composed of 1000 nm of thermal oxide, 150 nm LPCVD $Si_3N_4$and 300 LPCVD deposited TEOS, was grown. After that the hardmask was patterned and etched to form the via's, which were then etched by silicon bulk etching in two steps to form the TSV's.

During the post etching inspection of the wafers a layout error in the sealing ring mask was detected. The small dimples required to electrically connect the bottom electrode of the top layer to the top electrode of the middle plane were missing, as shown in Fig. 4.35. To correct the problem a new mask with a proper design was ordered and the new run, namely "Process LSB2", was started with a new set of wafers.

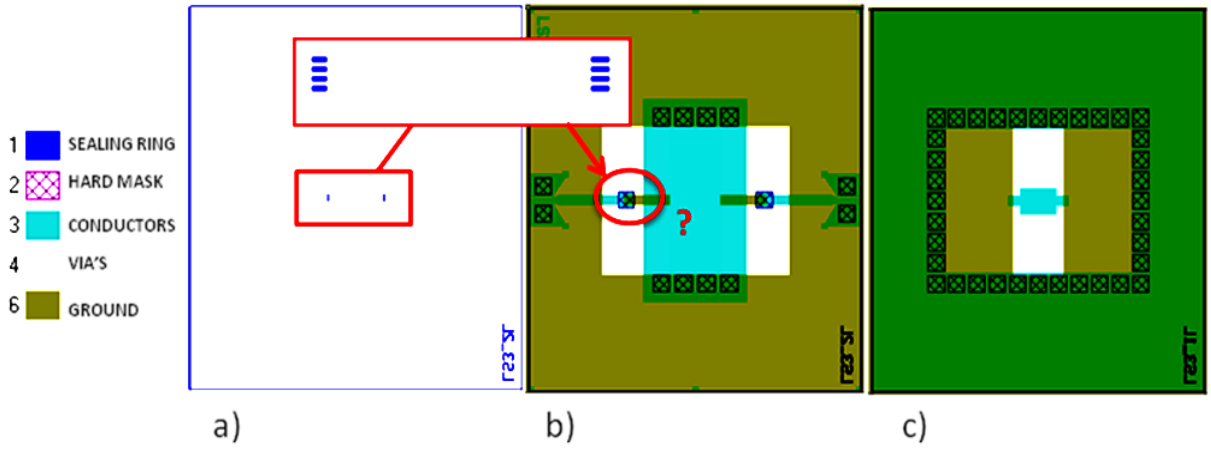


Figure 4.35: (a) layout of the sealing ring level of LS3 structure showing the missing dimples. (b) all layers of the top plate and (c) all layers of the middle plate showing the position where these dimples are needed to provide the electrical contact between the two layers.

4.16.2 Second Run (Process LSB2)

Also in the second run 6 wafers were used and an identical splitting scheme was adopted as in case of **"Process LSB1"**. The process followed the same

schedule till the formation of sealing ring. During the post sealing ring etching optical inspection again a mask error was detected, as illustrated in Fig. 4.36.

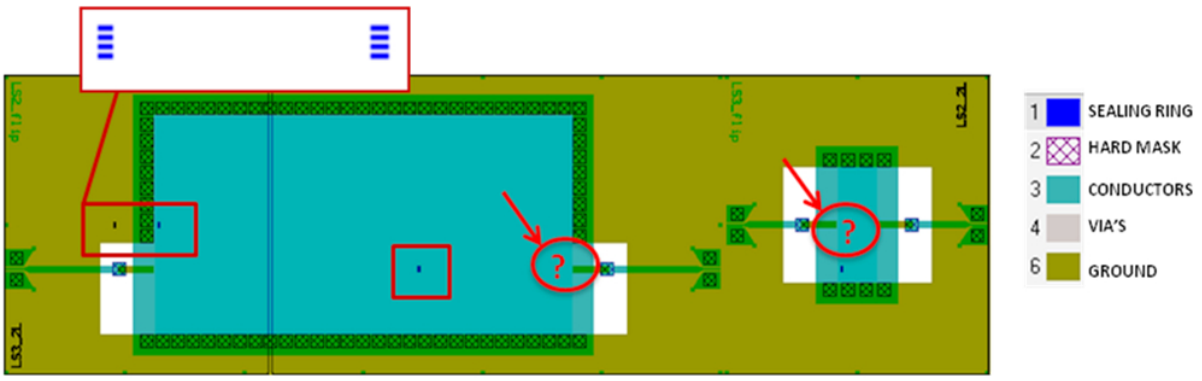


Figure 4.36: Layout of a LS2 structure showing the second mask error caused by a missing mirroring of the level. This time not only the electrical contact between layers is affected but also the sealing ring is only present on the long sides of the device.

This time the error was caused by a missing mirroring of the sealing ring layer. The reason for this error was that when the order for the mask was placed to the mask shop it was not specified that the mask was intended for the backside. Due to the missing mirroring not only the contact dimples were at the wrong position but also the sealing rings were misaligned in the horizontal direction. Despite this error in the sealing ring mask it was decided to continue with the processing in order to identify any pitfalls that could hamper the processing sequence in the following steps. Moreover, the processing on two wafers of the first lot (LSB1) was also continued.

The process was continued following the planned schedule. After the strip of the mask oxide in Buffered Oxide Etch (BOE) 7:1 the wafers were oxidized at 975°C in steam for 385 min in order to grow 1 μm of thermal oxide. This thermal oxide was then coated with 150 nm of Si_3N_4 and 300 nm of TEOS oxide, both obtained by LPCVD. The vias were etched overnight with a 1:4 TMAH:water solution at 90°C and the above mentioned problems were

solved. After this first step of approximately 15hrs a 350 μm depth was reached which was then brought to the final depth in a second etch again at 90°C, as depicted in Fig. 4.37.

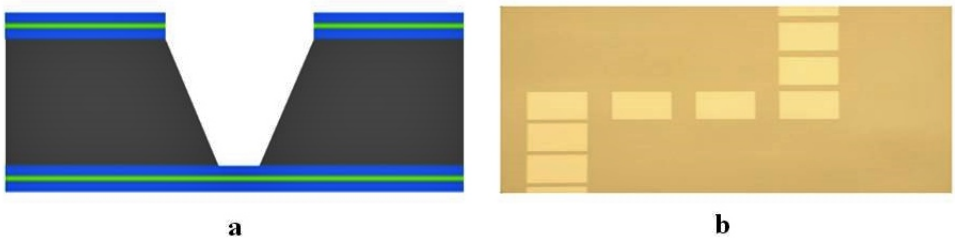


Figure 4.37: Through silicon via etch, (a) schematic cross section, (b) top view of the etched hard mask.

The hard mask on the wafer front side was removed by dry etching in plasma. Previous experience with run KaA has shown that plasma etching eliminates any under etching of the silicon on the bottom of the via hole which is an essential requirement for a continuous seed layer deposited by PVD, refer to Fig. 4.38(a,b).

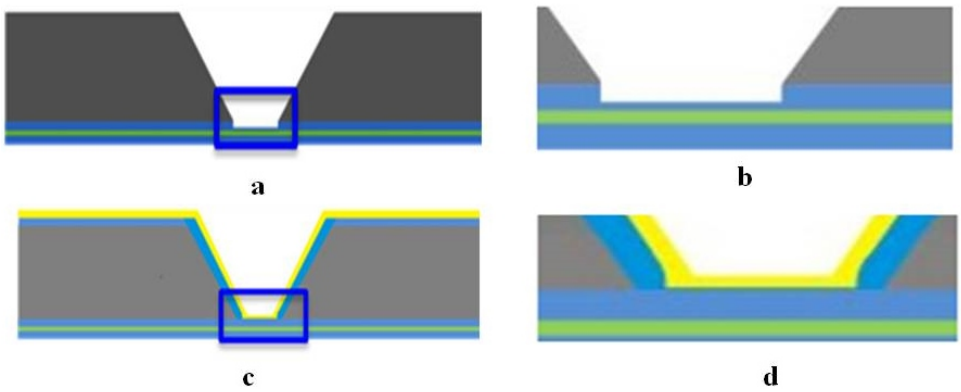


Figure 4.38: (a) Schematic cross-section for removal of the front side hard mask without under-etching the silicon, (b) magnified image. Conformal coating with seed layer (c) and (d).

The via holes were then passivated by growing a 1 μm thick thermal oxide in stem atmosphere at 975 °C for 385 min and coated with a standard

2.5/25/2 nm thick chrome/gold/chrome multimetal seed layer as illustrated in Fig. 4.38(c,d).

After the definition of the top metallization layer with dry film, see Fig. 4.39(d) a 5 μm thick galvanic gold layer was deposited on this seed layer. Next the via holes were plated with 100% yield and no membrane was lost.

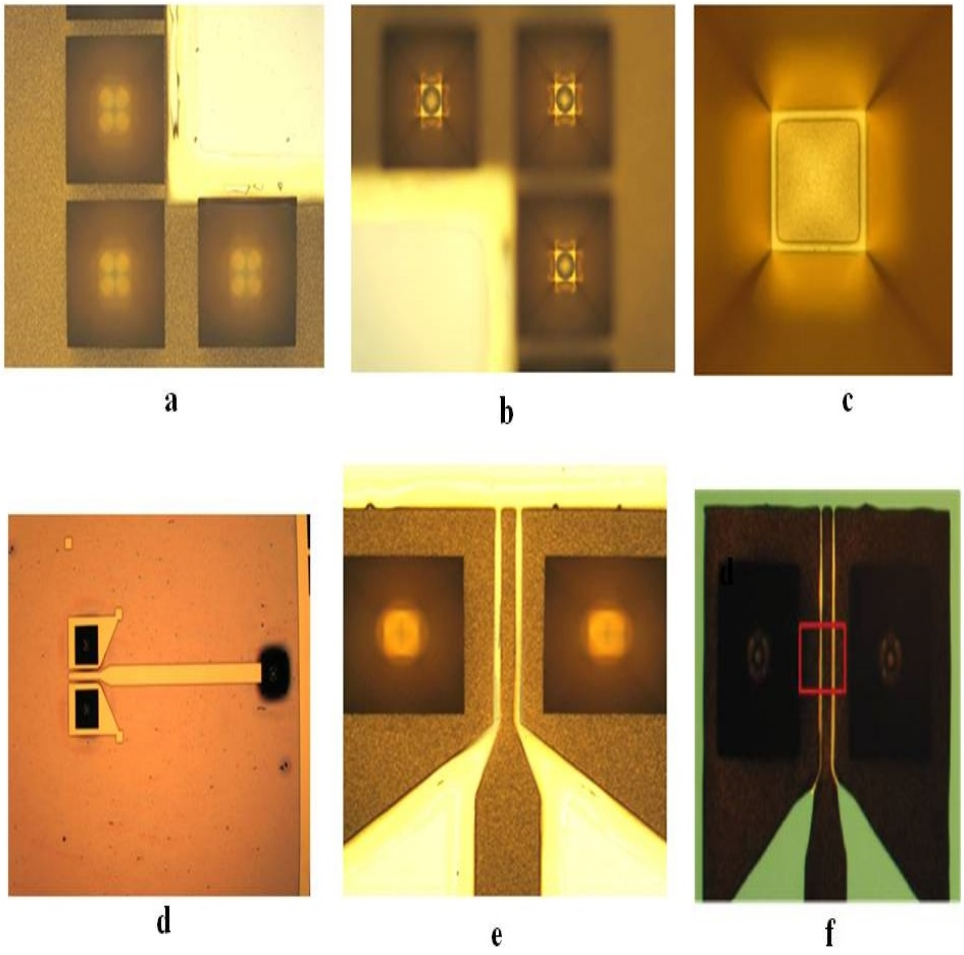


Figure 4.39: Top metal plating. (a) via holes, focus on wafer top, (b) via holes, focus on the wafer bottom and (c) close-up of the via base, (d) dry film after exposure, (e) top metallization after stripping resist showing the heavy under growth and (f) after seed layer removal, showing the residues in the CPW slot.

At this point a different problem appeared. It was found that all features of the CPW were showing a very strong under growth of gold, refer to Fig. 4.39(e), and it was impossible to completely remove the gold during

the following seed layer removal etch. Even with a large over etch it was not possible to clean the slots of the CPW lines, further over etching at this stage could affect the total thickness of gold, see Fig. 4.39(f). To avoid this and to recover one wafer. The wafer was coatted again with resist and the resist in the slots of the CPW lines manually was manually removed with a fine needle. By this technique the gold from the scratched area was etched off, and finally after removing the resist the seed layer was removed. But the problem could be solved only partially, as depicted in Fig. 4.40.

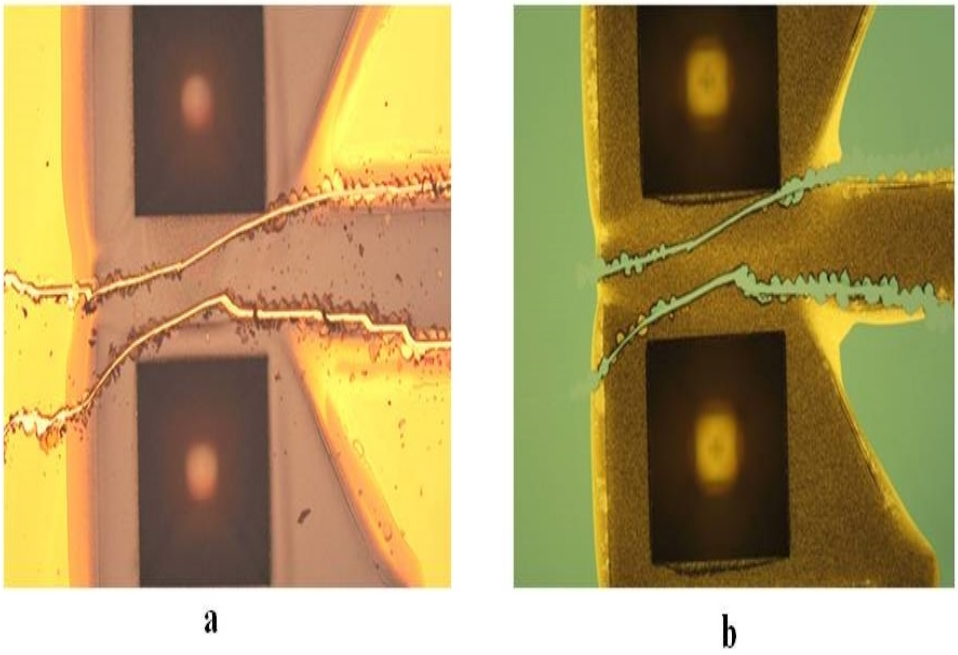


Figure 4.40: Partial recovery of a wafer affected by gold undergrowth. (a) slot line “opened" manually for gold etch, (b) after seed layer removal.

In due course the problem was solved by introducing a “wafer priming" step before the dry film lamination and a post exposure bake at 120° for 1 hour. The wafer priming is also known as adhesion promotion and normally hexamethyldisilazane (HMDS, (CH3)3 SiNHSi(CH3)3) is used as wafer primers. Primers form bonds with the surface and produce a polar surface. Most primers are based upon siloxane (Si-O-Si) linkages. In practce the

wafer is placed on a spinner where HMDS is sprayed onto the surface, which forms the bond with silicon surface and improves the resist adhesion. This procedure produced a well defined top metal, as presented in Fig. 4.41(a,c).

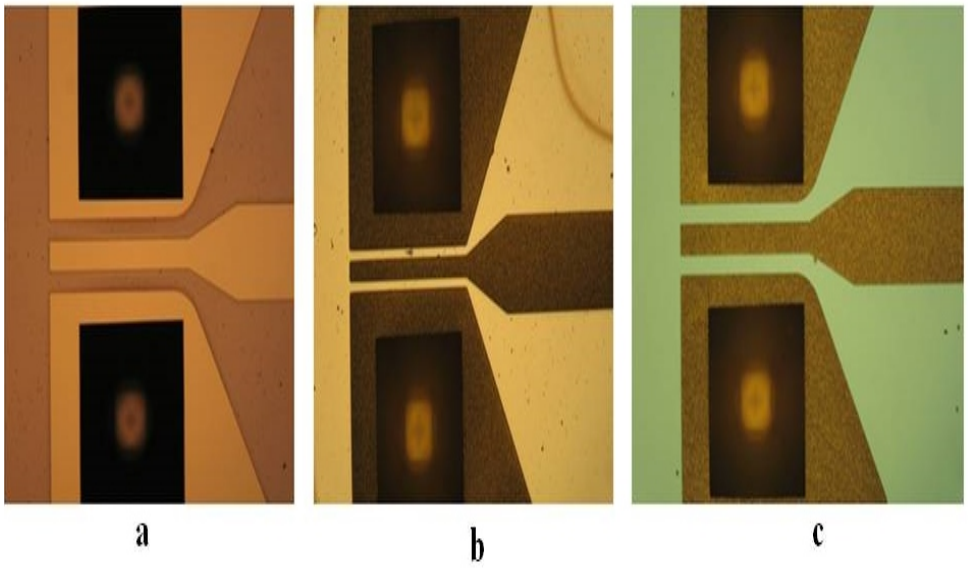


Figure 4.41: Top metal definition after improving the dry film adhesion. (a) after dry film definition, (b) after plating and (c) after seed layer removal.

The next problem was faced during the definition of the bottom via and the hard mask window definition. Unfortunately some of the membranes on the TSV's were broken while the wafer was clamped by the vacuum chuck of the resist spinner, see Fig. 4.42. This made the spinning of the resist problematic because some of the resist was suck by the vacuum into the TSVs. To overcome the problem two solutions were tried:

- filling of the metalized TSVs with solder balls
- and temporarily fixing the process wafer to a support wafer.

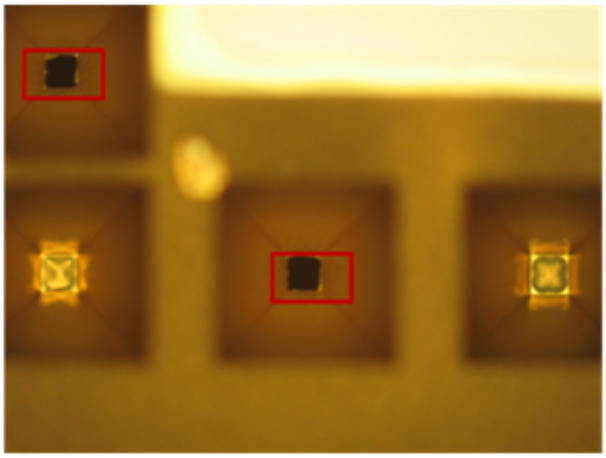


Figure 4.42: Broken membranes in the through silicon vias.

Next, the TSV's with broken membranes were filled with Ag-Sn-Cu alloy solder balls of 0.5 mm diameter. After that the wafers were subjected to controlled heat, which melts the solder ball. Unfortunately after reflow the solder soaked the bottom metal in an irregular way while on the frontside the solder protruded through the via hole producing an uncontrolled overgrowth of unpredictable height. Therefore this technique did not produce usable results, see Fig. 4.43.

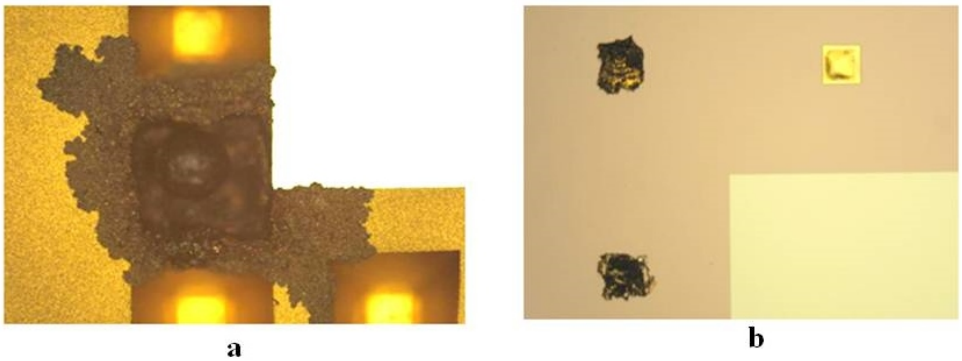


Figure 4.43: Through silicon via holes after filling with solder balls, a) back side and b) front side.

Finally the problem was solved by gluing temporarily the process wafer to a support wafer by four small drops of photo resist. This allowed completing

the processing of the lithography step (coating, exposure and developing). The wafer was then separated from the support wafer in a wet solution of sulfuric acid after the plating of the gold.

Finally the membranes were formed by an anisotropic bulk silicon etch with TMAH. The etching was performed in two steps in order to measure the etch rate in the first step and then, if required, correct the etch time in the last part of the etch. This allowed producing 20 μm thick membranes with good precision. Only one wafer was completed and Fig. 4.44(a,b) presents the final devices with top and middle plates respectively.

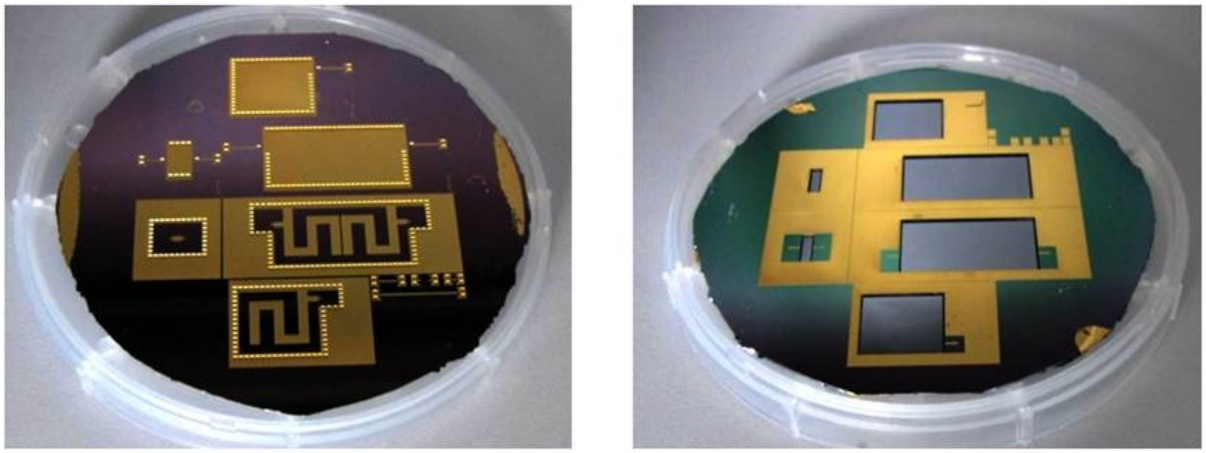


Figure 4.44: Completed wafer of process LSB2 (a) Top plate (b) Middle Plate.

Chapter 5

Structural Modeling

5.1 Introduction

MEMS devices are usually composed of many elastic structures including beams, cantilevers, plates, membranes and small forces (structural loads) can result in deformation, or possible damage of the structure. Also these structures can vibrate or be physically disturbed at certain natural frequency. Within a structure vibration or resonance is determined by the inertial and elastic properties of the materials. Especially in micro structures the vibration motion or resonance is a fundamental factor to many of the vibration and noise related problems. Therefore vibration and noise levels must be kept within acceptable limits. For better understanding of any structural vibration problem and to attain a robust and optimal design the resonance frequencies of a structure need to be identified and quantified.

5.2 Modal Analysis

In order to determine the susceptibility of the fabricated filters to vibration (a parameter of concern for the future space application) of these devices a modal analysis of the flexible structures (membranes) was carried out in order to determine the first natural frequencies and vibration modes of the devices.

To this purpose a FEM analysis of the basic structures, using ANSYS [86], has been made and the first 20 natural frequencies and mode shapes were extracted. In this simplified analysis any interaction between membranes of the device was not considered.

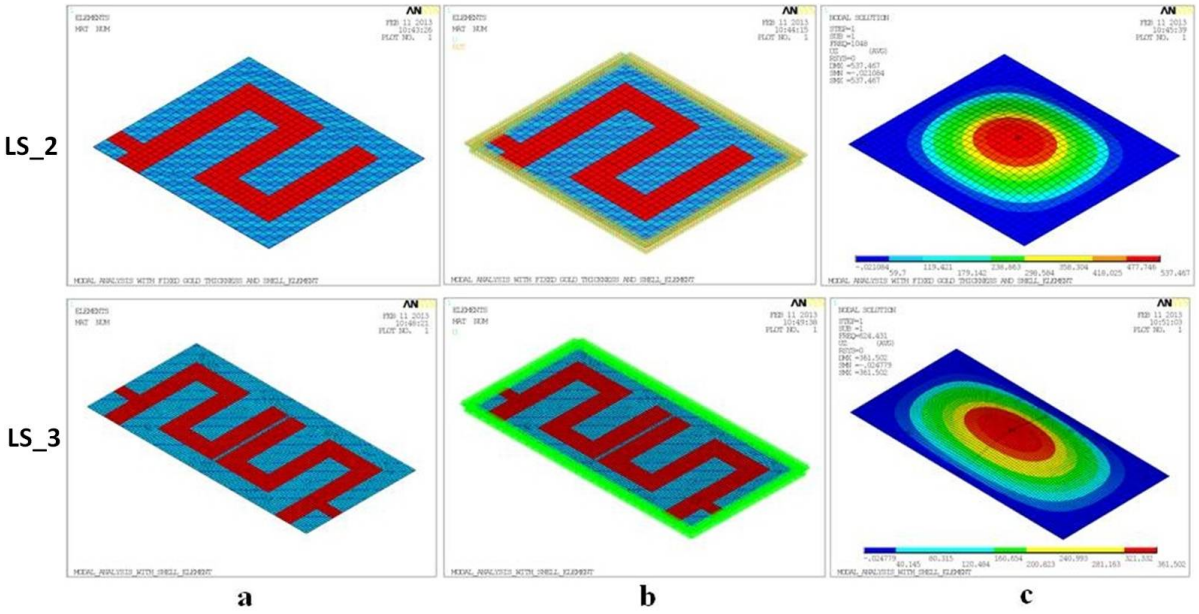


Figure 5.1: Modal analysis of two L/S oscillator structures (L2 and L3). (a) geometry, (b) constraints and (c) first mode.

Shell281 [87] was used as a basic element to model the mass-spring system formed by the multilayer membrane and the gold electrodes. The composition of the membrane assumed for the model is reported in Table 5.1.

Table 5.1: Table 5.1 - Structure of the membranes. Al values are in μm.

Layer	**L/S**	**Ka**
Gold	5	2
Silicon Dioxide (SiO_2)	1	1
Silicon	20	20
SiO_2		1
Gold		2

In case of the L/S oscillator the results obtained for this simplified model

are summarized in Fig. 5.1 while in Table 5.2. the frequencies and the simulation parameters are grouped. It can be seen that only a few of them are below 1500 Hz, the upper threshold for the vibration tests.

Table 5.2: Modal analysis of two L/S oscillator structures (L2 and L3), first 5 resonance frequencies of the FEM model.

	SET	**TIME/FREQ**	**LOAD STEP**	**SUBSTEP**	**CUMULATIVE**
LS2	1	1047.8	1	1	1
	2	1997.9	1	2	2
	3	2297.9	1	3	3
	4	3147.1	1	4	4
	5	3265.8	1	5	5
	SET	**TIME/FREQ**	**LOAD STEP**	**SUBSTEP**	**CUMULATIVE**
LS3	1	624.43	1	1	1
	2	894.5	1	2	2
	3	1288.4	1	3	3
	4	1539.5	1	4	4
	5	1878.3	1	5	5

Fig. 5.2 shows the results obtained for the three Ka band membrane structures. In this case the first resonating frequencies of the structures are well outside of the range of interest for the vibration tests, as shown in Table 5.3. Which implies that these structures are quite immune from vibrations.

In this case the first resonating frequencies of the structures are well outside of the range of interest for the vibration tests, which should imply that these structures are quite immune from vibrations.

These results can be easily understood from a qualitative point of view. In case of the L/S band oscillators the membranes, albeit quite thick and stiff, are very large which reduces their stiffness. In addition the gold electrodes on top are considerably thick and heavy. Considering that the resonance frequency of the first mode is proportional to the square root of the ratio between the spring constant and the mass of the mechanical oscillator the L/S oscillators are expected to have a low resonance frequency.

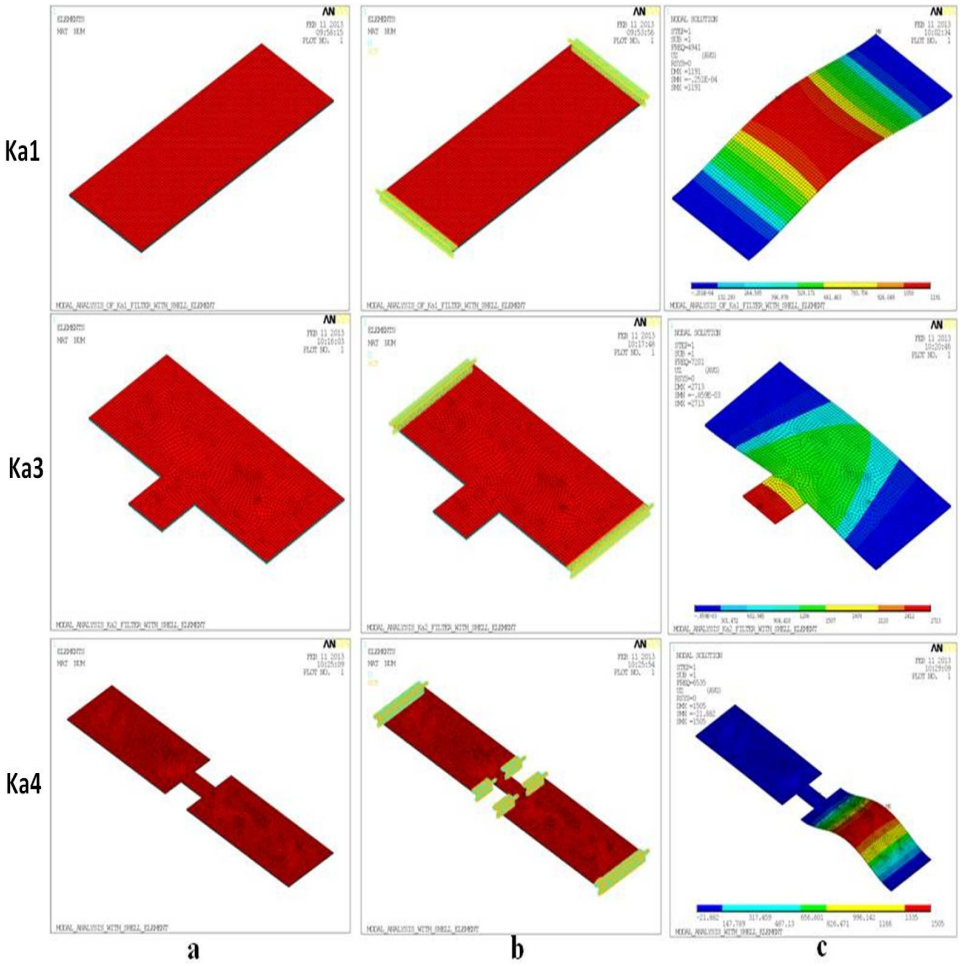


Figure 5.2: Modal analysis of three Ka oscillator structures. (a) geometry, (b) constraints and (c) first mode.

On the contrary the membranes of the Ka band structures are much smaller which makes them much stiffer. This is well reflected in the significantly higher values of the first resonance frequencies given by the numerical analysis.

In both cases (i.e. Ka and L/S) it can be assumed that the prototype structures will be stiffer than modeled due to the additional stiffening effect of the entrapped air in the structures which creates a force on the membranes that opposes the out of plane movement.

From this simple assessment following conclusions could be drawn:

Table 5.3: Modal analysis of three Ka oscillator structures, first 5 resonance frequencies of the FEM model.

	SET	TIME/FREQ	LOAD STEP	SUBSTEP	CUMULATIVE
Ka1	1	6634.8	1	1	1
	2	13167	1	2	2
	3	18288	1	3	3
	4	28771	1	4	4
	5	35871	1	5	5
Ka3	**SET**	**TIME/FREQ**	**LOAD STEP**	**SUBSTEP**	**CUMULATIVE**
	1	7201.1	1	1	1
	2	10858	1	2	2
	3	22359	1	3	3
	4	25811	1	4	4
	5	32621	1	5	5
Ka4	**SET**	**TIME/FREQ**	**LOAD STEP**	**SUBSTEP**	**CUMULATIVE**
	1	6535.2	1	1	1
	2	6903	1	2	2
	3	12123	1	3	3
	4	12572	1	4	4
	5	18021	1	5	5

- The L/S structures have Eigen frequencies in the 20 - 2000 Hz range (i.e. LS2 has 2 and LS3 has 5 respectively).
  - They behave as classical mass spring systems.
  - The resonance frequency could be higher if the electrodes could be designed with less metal.
- All Ka structures have Eigen frequencies well out of the critical frequency range.
- Therefore, it can be assumed that the complete structures of both Ka and L/S band filters will be stiffer due to the contribution of the entrapped air.

Chapter 6

Assembly of Filters

6.1 Introduction

This chapter focusing on the development of assembly of Ka and L/S band filters, presents the parametric study performed for the development and optimization of thermocompression technology for the filters in subject, and reviews the bonding technologies currently employed in microelectronics and MEMS industry.

Packaging, assembly and hermetic sealing is an indispensable part of microfabrication technology. Most MEMS devices contain fragile moveable parts or components which requires protection from the external environment, which could otherwise destroy the delicate device or affect its performance. Therefore a reliable and cost effective packaging is a major challenge for today's MEMS or Microsystems industry as packaging cost can reached above 70% of the total cost of the device [88] or even higher (i.e. 95%) varying from product to product. In general, the packaging of MEMS devices or microstructures involves various steps, which are:

- Dicing
- Assembly and packaging
- Testing

The assembly is also regarded as a part of packaging and for the present work. The assembly of the filters can be performed either at (a) wafer level packaging (WLP) or (b) at die level (using die bonding). While at wafer level this can be done either by thin film packaging (TFP) or by wafer bonding. In the following paragraphs a comparison of the two types of bonding techniques that can be used for the Ka and L/S band filters is given.

6.1.1 Wafer Bonding

At FBK the wafer level bonding can be done with the AML AB04 wafer bonder [89], which allows also the thermocompression gold to gold bonding. The machine can apply a total force of 15 kN and uses a topside camera for the alignment. In order to do the assembly at wafer level the following conditions are necessary.

All layers have to be manufactured separately, which requires a specific mask set for each. The alignment has to be done through holes in the top wafer because at the end of the process the wafers will be opaque even for Infra red (IR) radiation due to the metallization. For singulation the whole stack must be diced.

All the above mentioned conditions can be meet, even the most critical one, i.e. the dicing of a thick stack of wafers. However, the efforts in terms of hardware and cost are very high and probably beyond the limits of the project, which needs just the practical demonstration of a limited number of prototype filters.

6.1.2 Die Bonding

The assembly can also be performed at die level. FBK owns a flip-chip aligner and bonder (TRESKY), which is suitable for the task and possess in situ optical alignment system. In this case the alignment is performed by two

cameras face to face and the pressure is applied by a load cell, which delivers a maximum load of 2 kg. The key feature of this approach is that, as mentioned above, all layers can be produced with only two processes. Therefore only two mask sets are needed and no dicing is needed at the end of the stacking. Considering that for the bonding of smaller pieces the constraints on the flatness are much less severe, this seems the most practical approach for the prototype devices needed in this project.

Among the many types of bonding techniques only a few one apply to the present work. For Ka and L/S band filters assembly various bonding technologies relating to wafer or die bonding were analyzed. In the following a short overview of the commonly used bonding technologies in semiconductor and MEMS industry is given.

6.2 Overview of Bonding Technologies

Bonding is an adherence phenomena and can be defined as “Whenever clean, flat and mirror polished surfaces of any material at room temperature are brought into contact are locally attracted to each other by “van der Waals forces’ and form a bond".

Wafer bonding [90] is a technology that on one hand provides integration of CMOS and MEMS devices and on the other hand is also capable to enhanced the device functionality. At present it is the technology of choice for creating three dimensional geometries or structures [91]. Early research on wafer bonding was started in 1980’s and at present various bonding techniques are used for the packaging of semiconductor and MEMS devices. These techniques can broadly be categorized as: (a) direct bonding (b) indirect bonding.

6.2.1 Direct Bonding

Direct bonding is commonly known as bonding silicon on silicon. In this technique Si wafers are bonded together without any additional intermediate layer. For achieving void free bonding at room temperature direct bonding requires smooth, flat and clean wafer surfaces, which can be chemically treated before bonding. It is a two step bonding process; first bond is formed at room temperature with the aid of intermolecular interactions, hydrogen bonds and van der Waals forces. Second annealing at intermediate temperature to strengthened the bond. Depending upon the application the direct bonding can be performed under various conditions such as vacuum, regular atmospheric conditions of inert gases. Mostly it is used to bond silicon on insulator (SOI).

6.2.2 Indirect Bonding (using an intermediate layer)

Numerous bonding techniques belong to the category of Intermediate layer bonding, namely: eutectic bonding [92–94], glass frit bonding [95–97] and adhesive wafer bonding [98, 99]. While SiO_2, conductive adhesives, and soft metals [100, 101] such as, gold (Au), silver (Ag), copper (Cu), Aluminum (Al) are used as intermediate layer to connect separate surfaces, more often they can be bonded together by electrical, thermal and compression techniques. All these techniques can be highly productive but each has its distinct bonding requirements and limitations. Normally when the application requires hermeticity and good electrical conduction between the bonded surfaces a metal-to-metal bonding technique is used and among them the thermocompression bonding is an excellent choice. Therefore the work of this thesis focuses on the gold-gold thermocompression bonding.

6.3 Thermocompression Bonding

As appears also from the literature review in most approaches metal to metal bonding has been adopted, with a preference for gold-gold thermocompression bonding. Thermocompression bonding is a form of solid state welding in which temperature and pressure are simultaneously applied to join the two separate surfaces [102]. For the present work the choice of thermocompression bonding is determined on one side by the requirement to provide an internal metallization of the cavities together with the electrical continuity in case of cavities build by multiple staked wafers and on the other side by the requirement of hermeticity. In addition the filter designs require also TWV holes, which run eventually through more than one wafer level. The metal to metal bonding is the only one that matches all requirements and allows for a relative simple process scheme.

Thermocompression bonding is based on the fact that metallic bonds form when the distances between the two substrates are so small that it becomes energetically favorable for surfaces to coalesce in order to eliminate the interfacial energy. The surfaces can be brought together by the application of pressure. Due to surface roughness, bonds initially form where the surfaces touch near asperities. While the materials deform under pressure, the asperity height decreases, and more areas are brought into contact [103]. At room temperature, relatively high pressures are needed for inter atomic attraction to overcome surface asperities in metals. But dislocation mobility and diffusion increases with temperature, resulting in softening of the metal and viscoplastic deformation. Therefore the pressure requirement can be offset by increasing the processing temperature.

However, the required pressure and temperature may not be in a practical range for all metals. As a noble metal, gold is an ideal bonding material and a good example of thermocompression bonding is gold wire bonding. In case

of gold a comprehensive study on fabrication and characterization of gold-to-gold thermocompression has been done by Tsau et al. [104–107]. Other researchers [108, 109] have reported typical temperature ranges from 270°C to 340°C, while the applied pressure varies from a few MPa to up to120 MPa. The bonding time can be as short as 10 min and as long as 1h. Best bonding characteristics seems to be obtained at 300°C and 120MPa of pressure.

An interesting room temperature version of this process has been proposed by Decharat et al. [110] based on the strong shear forces that develop between two sealing rings with small overlap, but up to now the hermeticity is a problem with this approach.

As mentioned above the best conditions for stable and hermetic bonding require 120 MPa of bonding pressure. Achieving this pressure depends on the total force that the wafer bonder can apply and the bonding area. A simple way to achieve a specific bond pressure consists in reducing the bond area by fabricating a sealing ring, as shown in Fig. 6.1. This is achieved by selectively masking the sealing ring area with photo resist and dry etching of the silicon substrate for about 2 μm or higher. The optimum value of the sealing ring height and width and the optimum bonding conditions in terms of temperature and pressure were determined by dedicated test runs i.e. preliminary experimental work on thermocompression bonding [111] presented in the following section. In designing the sealing ring the minimum width

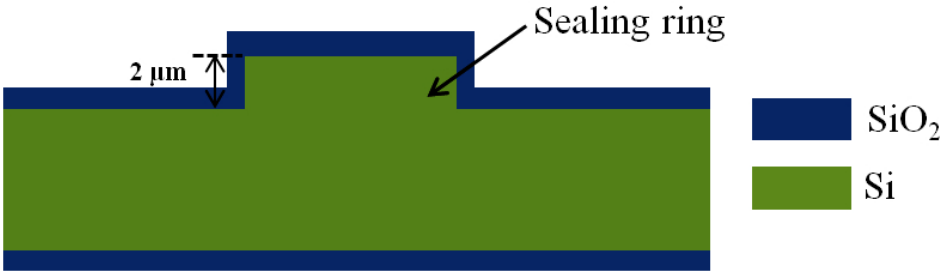


Figure 6.1: Schematic cross section of the sealing ring. On one wafer a protrusion is build, either by a spacing layer, e.g. a polysilicon ring, or by etching the structure in silicon.

of the sealing ring is an another important factor that has to be considered. Two aspects have to be addressed: (a) the width of the sealing ring should guarantee a minimum overlapping of all the sealing rings of a stack in order to avoid/minimize bending moments and (b) the number and flexibility of the single seals.

Overlapping: In order to reduce the bonding area it is important to assure that all bonding areas have a substantial overlap over the whole stack, see Fig. 6.2. Because any major misalignment between the wafers or dies could produce strong bending moments during the bonding process, which could eventually impair already formed bonds. Therefore the sealing ring width has to be chosen in a way that all sealing rings have a substantial vertical over lap. As a first approximation of the minimum sealing ring width one could use the ideal width for the optimum pressure augmented by 6 times (the maximum number of stacked layers) the alignment error of the bonder. As this error is in the order of 3 μm this implies an oversizing of $\approx$20 μm.

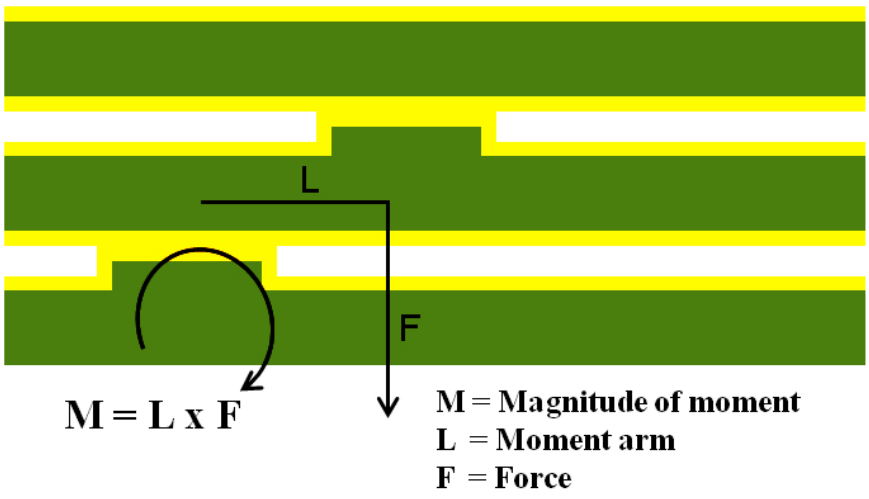


Figure 6.2: Misalignment in the stacking procedure could produce unwanted bending moments.

Force redistribution: The second point arises from the consideration that at each sealing the two gold layers will undergo plastic deformation and each will also behave in some way elastically. This implies that when a force is applied to the full stack actually not only the last seal is put under pressure but also all the others as well. In practice the stack of sealing rings will behave like a chain of springs, as illustrated in Fig. 6.3.

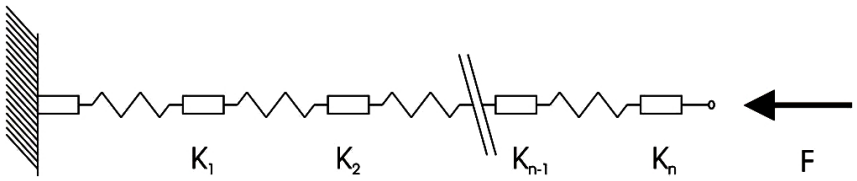


Figure 6.3: Model for the force redistribution within the stack of seals.

In this case each seal will experience a force that depends on the own spring constant as well as on those of all other springs involved, i.e. in case of identical springs the applied force will be distributed equally over all springs and the single spring will experience a force equal to the total applied force divided by the number of springs. This suggests to keep the number of stacked seals to a minimum and to reduce the seal width found to be optimum for a single seal by the number of seals that have to be stacked.

6.4 Experimental Procedure

From the beginning it was clear that a potentially critical step in the fabrication of both types of cavity filters is the vertical integration of the layers that form the final 3D filter structure. As explained above after the review of the relevant literature it was decided to opt for a direct bonding technique based on metal to metal thermocompression bonding. To this purpose gold (Au) and silver (Ag) were used as bonding materials and test vehicles were prepared for measuring the bond strength in the attempt to find the optimum processing conditions.

Au-Au thermocompression bonding is commonly used for MEMS and semiconductor devices, because Au has superior resistance to oxidation and provides good electrical and mechanical interconnection [108]. The gold joints are reliable, deliver higher bond strength and the risk of gold contamination is minimum even after the bonding process.

On the other hand, silver is a very ductile metal and also exhibits a lower yield strength. The higher electrical and thermal conductivity also makes Ag a good candidate for bonding applications [112, 113]. In addition Ag is a well accepted material for RF applications. In addition substituting Au with Ag can be more cost effective. Moreover, the formation of intermetallic compounds (IMCs) can easily be avoided by employing pure metals like Au and Ag in the bonding process. Table 6.1. shows some important properties of Au and Ag.

Table 6.1: Material properties.

Properties	**Gold (Au)**	**Silver (Ag)**
Thermal Conductivity (W/m.K)	312	429
CTE μm /°C	14.1	19
Yield Strength (MPa)	205	55
Young Modulus (GPa)	79	83
Melting Point (°C)	1064.4	961

Temperature, pressure and time are the main parameters, which determine the quality of the bond. This auxiliary study investigated the bond strength of Au and Ag electroplated sealing ring at 300°C and under a pressure of 11 MPa by varying the time. Shear tests were performed to estimate the mechanical strength of the bonded sealing ring, followed by the surface examination of the detached sealing ring joints by Scanning Electron Microscopy (SEM).

6.4.1 Sealing Ring Fabrication

Test sample were prepared by using 500 μm thick P-type <100> wafers with resistivity of 10-20 Ω cm. The test samples were both wafers with sealing ring and standard blank wafers. RCA cleaning was performed on all wafers and then photo resist was deposited, exposed with a test mask (square sealing rings of 1 cm lateral size, rounded corners with a sealing ring width of 50 μm) and developed to define the sealing ring of 50 μm width. An Alcatel DRIE system was used to etch a sealing ring with a step height of 2 μm. The step height and width was measured by optical profiler as shown in Fig. 6.4(a, b).

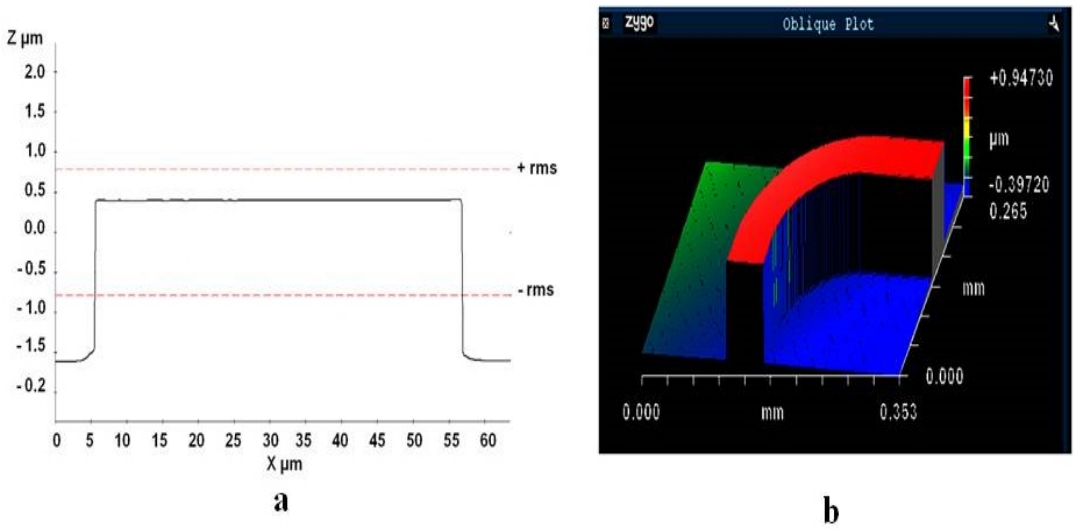


Figure 6.4: Sealing ring with step height of 2 μm. (a) graphical representation (b) 3D view of rounded corner.

After the fabrication of the sealing ring a 300 nm thick thermal oxide was grown on the wafer pairs (patterned and blank). Then a Cr/Au(5/25 nm) seed layer was evaporated by PVD followed by electroplating [114–116] to obtain a uniform 2 μm thick gold layer. The gold layer was then annealed for 30 min at 120°. Silver deposition was performed by using a Uniform Injection Cell (UIC) electroplating system [117, 118], as shown in Fig. 6.5.

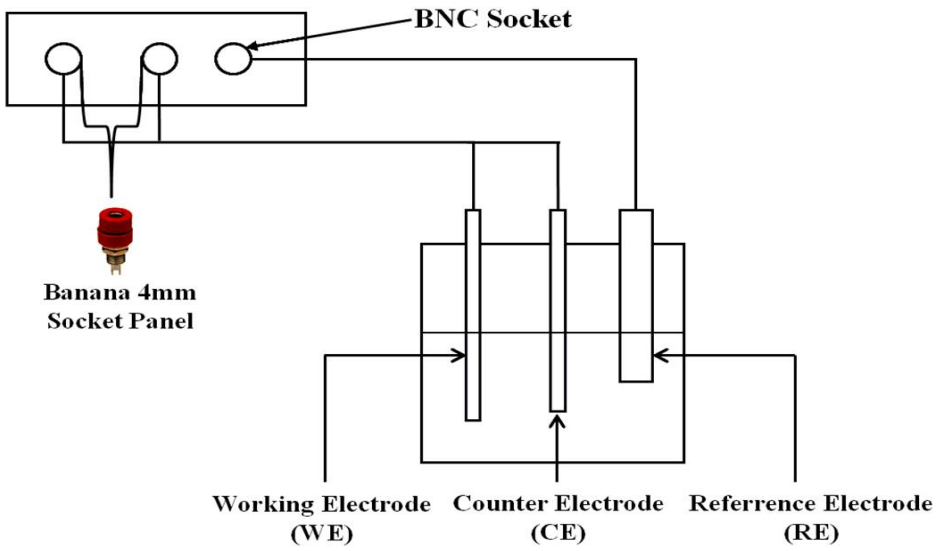


Figure 6.5: Schematic of Uniform injection cell (UIC).

After the oxidation process a Ti/Ag (20/150 nm) metal layer was evaporated and then the wafer pairs were immersed in the UIC and electroplated to accomplish a 2 μm thick Ag layer. In order to prevent silver plated wafers from oxidation and to enhance the solderability of the metallic surfaces, the wafers were immediately coated with a thin Cr/Au(2.5/50 nm) layer, as the presence of an oxide layer could preclude the formation of a strong bond.

For test purpose, from each electroplated wafer pair (patterned and blank) square dies of 1x1 cm^2 were diced and used as test assemblies for Au-Au and Ag-Ag thermocompression bonding, as depicted in Fig. 6.6(a, b).

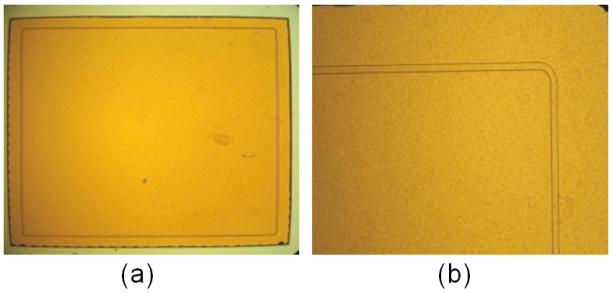


Figure 6.6: (a) Au electroplated 1x1 cm^2 die and (b) magnified image of sealing ring corner.

6.4.2 Thermocompression Bonding Tests

Thermocompression bonding tests were performed by applying heat and pressure at the same time. Surface contaminations were removed by applying an O_2 plasma treatment on the Au and Ag dies immediately before bonding. For convenience the bonding tests were made at die level instead of wafer level. After cleaning, the die with the sealing ring was placed on the heated plate with vacuum chuck. Next, the pick-up tool grasped the second die with vacuum and after proper alignment both dies were brought to contact. When the desired pressure was achieved the temperature was increased until the predetermined value of bonding. A conceptual illustration of thermocompression bonding process performed on the test samples is presented in Fig. 6.7.

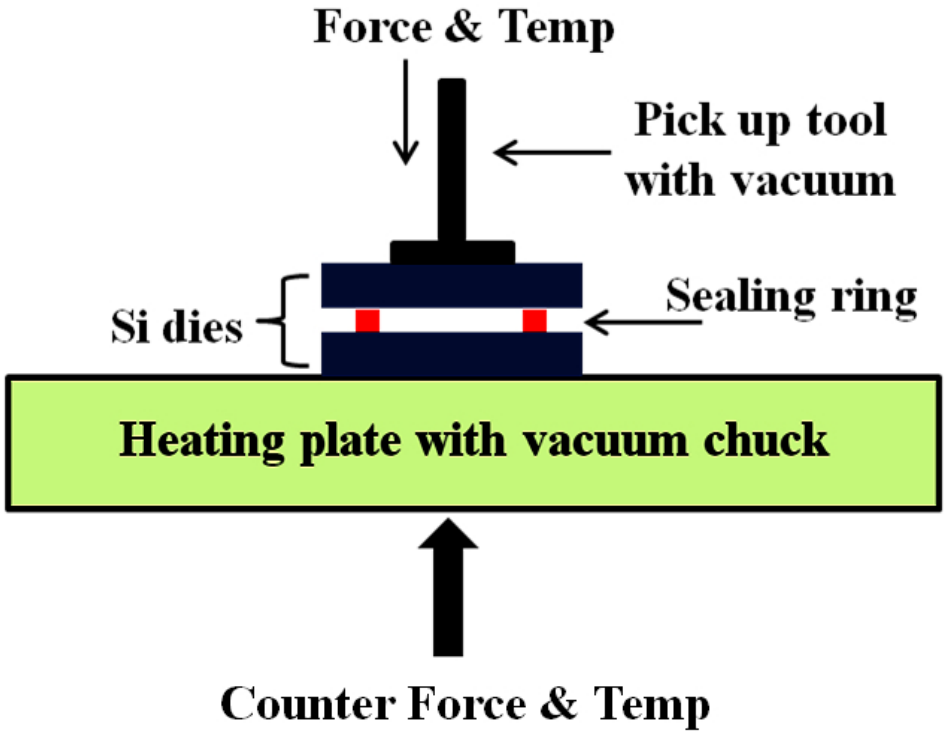


Figure 6.7: Conceptual illustration of the bonding process.

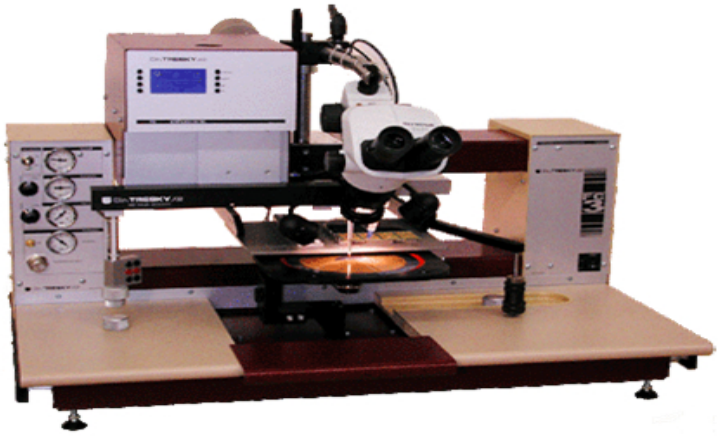


Figure 6.8: The flip-chip bond aligner TRESKY T-3000-FC3used for the die to die assembly of the filters.

Both Au and Ag plated specimens were bonded by a TRESKY T-3000-FC3 [119] pick and place bonder as shown in Fig. 6.8, while key features are given in Table 6.2.

Table 6.2: Key features of the TRESKY T-3000-FC3flip chip bond aligner.

Parameter	**Value/range**
XY- Movement (placement stage)	220mm x 220mm (manual)
XY- Movement (wafer stage)	220mm x 220mm (manual)
Z- Movement	95mm (automatic)
Spindle Rotation	360°
Bond Force (standard range)	20g - 400g (other force ranges available)
Bond Force (repeatability)	± 1g
Z-Measurement resolution	± 0.001mm
Max. PC Board-/ Substrate Size	400mm x 280mm
Max Plate Temp	450°C
Max Tool Temp	300°C
Placement accuracy	10μm; 1μm with high accuracy beam splitter

The bonding conditions under which the thermocompression bonding tests were performed for Au and Ag are reported in Table 6.3. Mechanical strength of the joints was measured by performing shear tests. A minimum of 3

samples were used for each bonding condition and the bond strength was computed by averaging the values.

Table 6.3: Bonding Conditions.

Materials	Time (min)	Temp (°C)	Pressure (MPa)
Gold	10,20,30,40,50,60	300	≈ 11
	60	350	≈ 11
	10,20,30,40,45,60.90	400	≈ 11
Silver	10,30,60	300	2.73
	10,30,60	300	5.47
	10,20,30,40,50,60	300	≈ 11
	10,20,30,40,50,60	350	≈ 11

6.5 Results

Fig. 6.9(a, b) presents the measured values of bond strength of the joints formed by Au-Au and Ag-Ag thermocompression bonding. The bonding process was carried out at constant temperature (300°C) and pressure (11 MPa) by varying the bonding time. The quality and reliability of bond is characterized by bond strength. Fig. 6.9(a) shows that a peak value of 18.12 MPa could be obtained at 50 min for Au-Au thermocompression bonding. This can be compared to the maximum bond strength of 18 MPa achieved by Nai et. al [120] at 400°C by applying the eutectic bonding technique. Others like Park et. al [102] have demonstrated qualitatively good bond strengths at 320°C by using thermocompression bonding. The lower bond strengths achieved on Au samples bonded below and above 50 min is probably due to the fact that bonding occurred only on some areas, as inspection after the shear test revealed. This was caused by use of a rigid “mushroom" like tool in combination with a slightly out of vertical application of the force, as will be explained more in detail in Section 6.6.

On the other hand, in the same conditions Ag samples bonded at 50 and

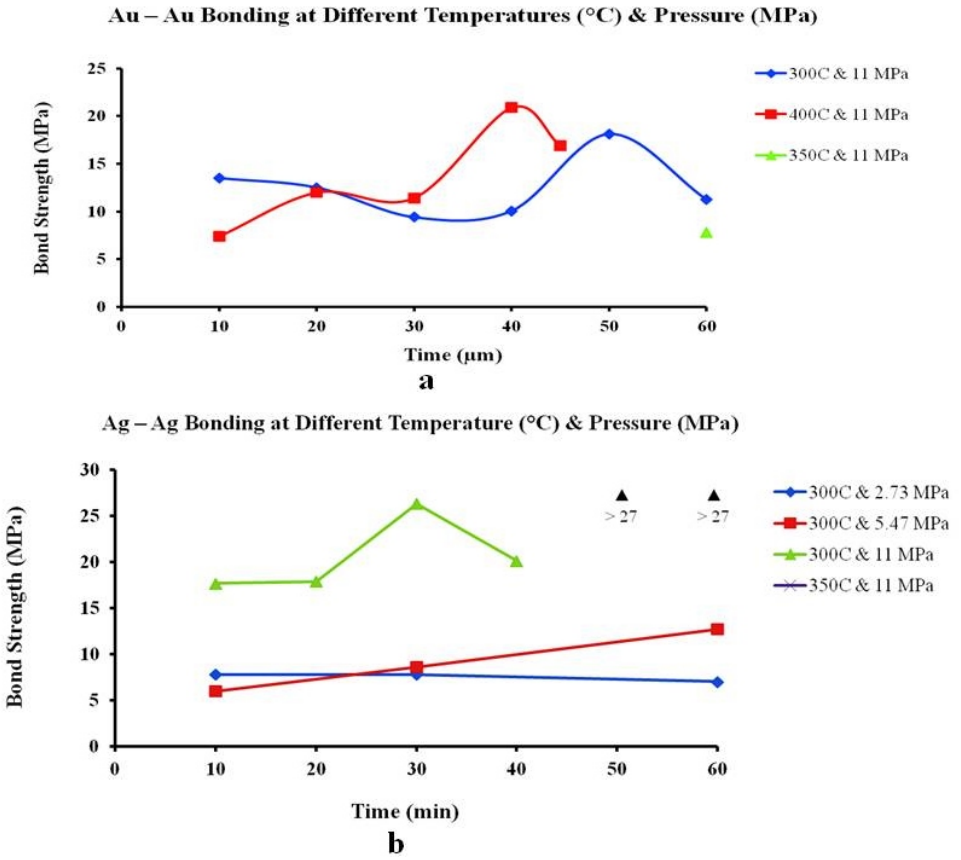


Figure 6.9: Bond strength plotted as function of bonding time at various temperature and pressure bonding results at 300°C with pressure of 11 MPa are considered for (a) Au and (b) Ag. Silver samples bonded at time higher than 40 min did not break at maximum applied shear force.

60 min did not detached at the maximum applied shear force. In this case the estimated bond strength is higher than 27 MPa at 300°C and under pressure of 11 MPa, as shown in Fig. 6.9(b).

For better understanding of this finding a comparison of the aspect of the fracture surface of Au and Ag sealing rings was made, using SEM pictures taken on the broken sealing rings after the shear test, see Fig. 6.10(a, b). Analysis of Fig. 6.10(a) reveals that in case of gold bonding occurs on a quite large area of the sealing ring and the aspect of the fractured surface of the sealing ring implies a strong plastic deformation while the shear force was

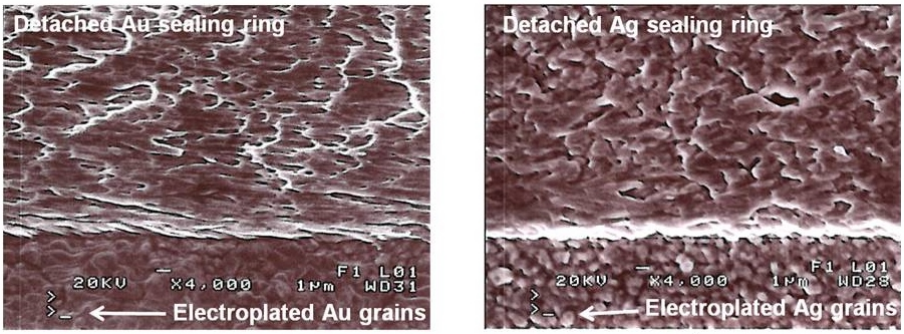


Figure 6.10: SEM images of (a) detached Au sealing ring joints with bonding time 50 min, (b) detached Ag sealing ring joint with bonding 30 min.

applied. The SEM image of Ag sealing ring joint interface in Fig. 6.10(b) shows that sealing ring was completely deformed and large area was bonded. In addition no voids and discontinuities can be seen. From this qualitative analysis it seems that Ag is subject to a stronger plastic deformation at the fractured surface. This can be correlated to the much lower yield strength of Ag with respect to Au.

6.6 Assembly of Ka Band Filters

The die to die assembly of the Ka band filters (test structures) was performed with a flip-chip bond aligner model TRESKY T-3000-FC3. The machine has in situ alignment capability. The alignment of the dies can be done with the help of two cameras that are capable of viewing the two surfaces (face to face) to be bonded together. Due to the variety in die sizes of the Ka band filters (these dies were much large than common IC dies) it was necessary to modify some of the machine parameters. The most critical one was widening the range of the camera stage in order to clearly view all corners of a device. For extremely large dimensions it was not possible to use the standard chuck. Instead an auxiliary chuck including heating elements was build for the largest device sizes. Finally the maximum load applicable by

the machine was increased up to 2 kg by an additional spring for the pre load.

The assembly procedure consisted in sample preparation, pre-assembly/stacking of the layers and final bonding. The sample of the individual layers were selected and cleaned with an oxygen plasma for 5 min at 80°C from both sides. This procedure eliminates any possible organic contamination from the gold surfaces, as presented in Fig. 6.11. The prepared elements of the filter were

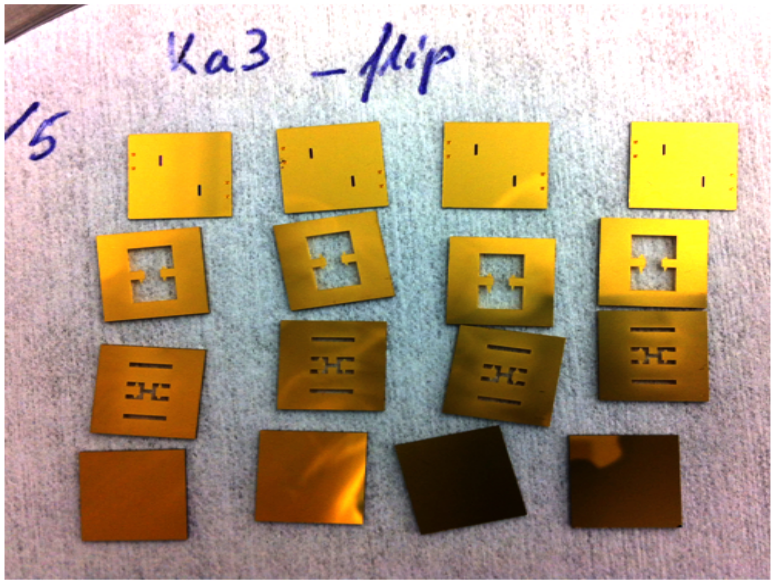


Figure 6.11: Elements of a Ka3 type filter ready for assembly. On the bottom there are the blank base plate. The next two rows are the middle plates L1 and L2 and the top row are the top plates (upside down).

first stacked starting from the blank bottom plate and adding successively the L1, L2 and the top plate. This preassembly was performed with the chuck at 25°C and a load of 2 kg for a few minutes. The alignment accuracy is in the order of 10 μm. The main error in alignment came from the misalignment of the cavities etched with the bulk etch. In any case the structures were aligned and placed on the chuck by centering the relevant structures with respect to each other. Once all elements have been stacked correctly a load of 2 kg was applied on the stack and temperature of the chuck was raised to 350°C for 45

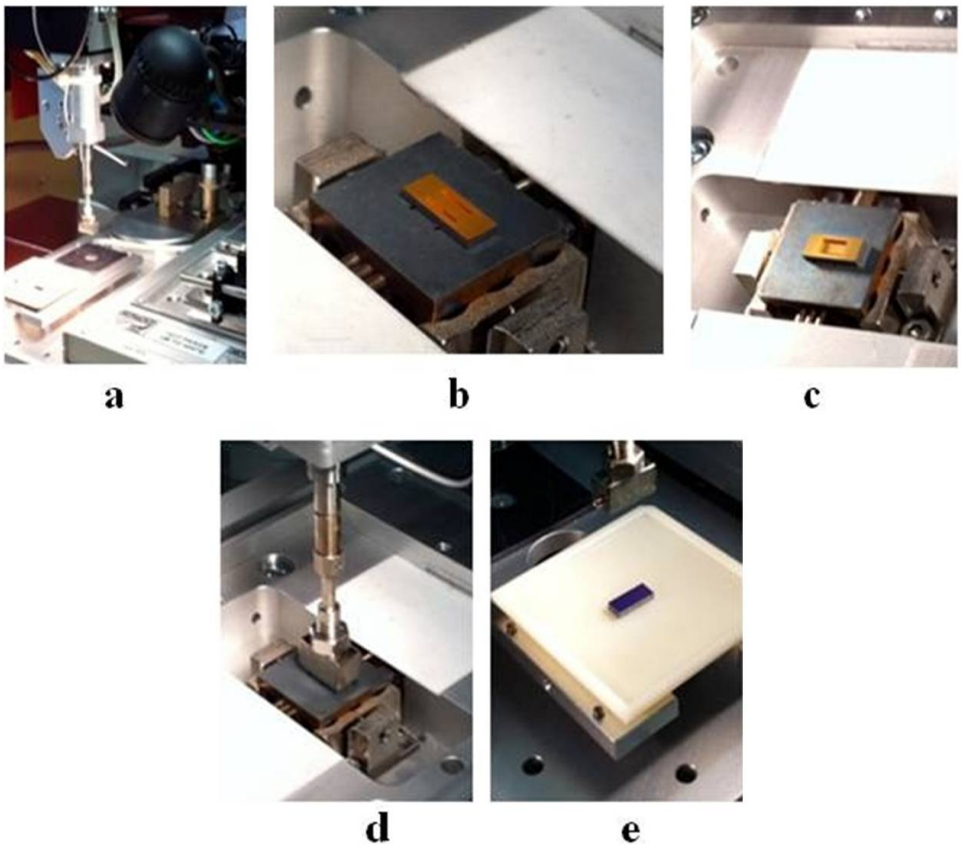


Figure 6.12: Assembly of a Ka2 type filter at different stages. (a) base plate positioned, (b) L1 layer in place, (c) L2 layer added, (d) top layer added and (e) finished device.

min. The assembly steps are depicted in Fig. 6.12. The prepared elements of the filter were first stacked starting from the blank bottom plate and adding successively the L1, L2 and the top plate. This preassembly was performed with the chuck at 25°C and a load of 2 kg for a few minutes. The alignment accuracy is in the order of 10 μm. The main error in alignment came from the misalignment of the cavities etched with the bulk etch. In any case the structures were aligned and placed on the chuck by centering the relevant structures with respect to each other. Once all elements have been stacked correctly a load of 2 kg was applied on the stack and temperature of the chuck was raised to 350°C for 45 min.

For stacking the individual layers and then applying the load on the full

stack a new pickup tool for the die bonder having the same size and shape as that of Ka filters plates was designed and manufactured. It was found later that this tool caused only a partial bonding along the perimeter of the device because of a small deviation from the true vertical axis in the flip chip aligner. As shown in Fig. 6.13 in case of a slight deviation from the vertical axis a large pickup tool applies the load only on one side of the die stack. This produced a bonding only on about 10% of the length of the sealing ring. As there is no means in the machine to correct this misalignment a different solution was adopted. A small metal block was machined with the same dimensions of the dies that features a small centering hole on top. By applying the load in this hole with a small rod the applied load could be evenly distributed over the full perimeter.

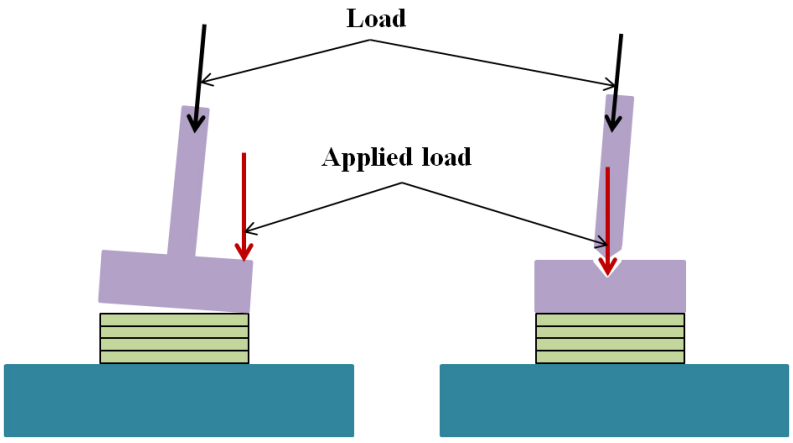


Figure 6.13: Schematic drawing showing (a) the effect of a non perfectly orthogonal applied load on the die stack and (b) how an interposer block loaded in the centre with a small round tool redistributes the force on the whole perimeter of the sealing ring.

Assembly was performed in two sessions. In a first series only 6 devices were assembled essentially to test the procedure. These devices had middle planes from run KaB2 where the insufficient corner compensation hampered the elements for the Ka3 and Ka4 type devices and limited the usable devices to the Ka2 geometries.

In the second session the elements from the KaB3 run were used. In this session a total of 55 filters were assembled and the number of devices were limited only by the availability of top plates.

6.7 Bumping

For trial purpose on a few Ka2_flip devices of the first series the flip chip mounting on small PCB boards, prepared for this purpose, was tried.

As a first option gold ball bumping were tried. By welding 3 gold balls on each pad it was possible to create small $\sim$150 μm high columns. The prepared chip was then flip chip mounted on the PCB by applying a load of 100gr at 350°C for 30 min. This approach was not successful, also because the PCB could not withstand such high temperatures. In a second attempt the chip with the gold bumps was mounted to the PCB board by applying 200 grams at 150°C together with ultrasound applied at maximum power but also in this case the chip could not be mounted reliably to the PCB.

The second option for flip chip mounting was the use of solder balls. Balls of SnAg 3.9 Cu 0.6 solder of 0.5 mm diameter were used but it proved to be problematic to apply them with the tools of the flip chip bonder very likely because the operating conditions were not optimized. At the end the solder balls were mounted manually by using a solder iron, which allowed then to be weld to the chip and to the PCB board.

6.8 Assembly of L/S Band Filters

As in the case of the Ka band filters also in this case the industrial implementation of the manufacturing and assembly of the devices will rely on the wafer to wafer bonding but, for the same reasons as above, in the development phase it was decided to rely on die to die bonding.

6.8.1 Dicing

The wafers were diced with a DAD-2H-6T dicing saw from DISCO® by using standard blades for silicon. The wafer was mounted to the "blue tape" bottom down. Also in this case it was feared that the water jet used to cool the blade could damage the large thin membranes. Therefore once mounted on "blue tape" the wafer was covered again with the cover sheet of the "blue tape". This procedure was successful and none die was lost. Afterwards the dies were cleaned in oxygen plasma for 5 min at 80°C prior to bonding.

6.8.2 Filter Assembly

The die to die assembly of the L/S band filter was also performed with the flip-chip bond aligner, shown in Fig. 6.8. In order to be able to assembly these devices with very large (with respect to common die sizes) dimensions some modification to the machine had to be applied. In particular it was necessary to enlarge the range of the camera stage in order to be able to view all corners of a device. In addition for extremely large dimensions of the dies it was not possible to use the standard chuck. Instead an auxiliary chuck including heating elements was build for the largest device sizes. Finally the maximum load applicable by the machine was increased up to 2 kg by an additional spring for the pre load. Fig. 6.14 shows assembly process of L/S band filter.

Again the assembly procedure consisted in sample preparation, pre-assembly or stacking of the layers and final bonding. The sample preparation consisted in selecting the individual elements and clean them with an oxygen plasma for 5 min at 80°C on both sides. This procedure eliminates any possible organic contamination from the gold surfaces.

The prepared elements of the filter elements were first stacked starting from the blank bottom plate and adding successively the middle plate and the top plate. This preassembly was performed with the chuck at 25°C and

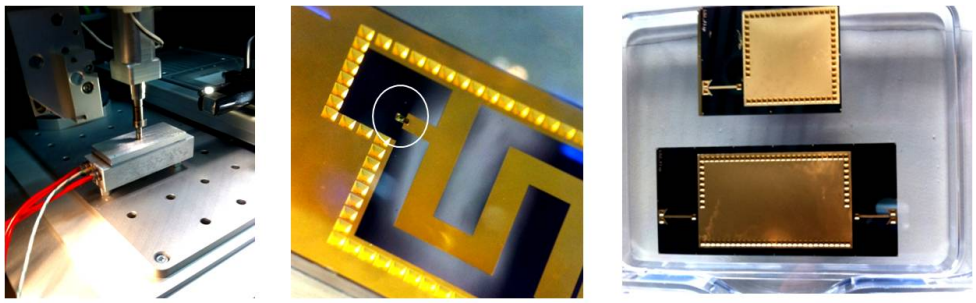


Figure 6.14: Assembly of the L/S filters. (a) the auxiliary chuck with heater, (b) 100 x 100 μm^2 gold leave 5 μm thick added to assure electrical contact between layers and (c) completed devices.

a load of 2 kg for a few minutes. The alignment accuracy is in the order of 10 μm. The main error in alignment came from the misalignment of the cavities etched with the bulk etch. In any case the structures were aligned by centering the relevant structures with respect to each other.

Due to the missing contact dimples, see above, it was necessary to assure the electrical contact between the middle plane and the top plane by adding a small spacer of gold. This was necessary to connect the signal feed line to the oscillator. This was achieved by manually cutting a roughly 100 x 100 μm^2 from a $\sim$ 5 μm thick gold leave with the aid of micro surgical scissors and a microscope. The gold leave derived from a non well adherent gold film. The small gold leaf of square shape were placed with the aid of a small needle in the relevant contact points, see Fig. 6.14(b).

Once all elements have been stacked correctly the stack was loaded with 2 kg by means of an interposer metal plate in order to apply the load uniformly and kept at 350°C for 45 min. Only the chuck was heated. The final outcome is shown in Fig. 6.14(c). A total of three devices were assembled successfully.

Chapter 7

Through Silicon Via

7.1 Introduction

This chapter focuses on the research activity carried out for the fabrication of conductive TSV's. A new method has been introduced for the development of via's employing the DRIE technique. This chapter also presents a detailed description of the via manufacturing method, along with experimental results and problems faced during the via metallization and how they were handled.

The research work for TSV's was origined by the 3D design of two filters. 3D integration is a cost effective solution in terms of miniaturization and system integration, like wafer-level packaging or vertical connections in multi-wafer devices [121, 122]. For the present work TSV's are viable solution that provide connection among different layers of the devices. As mentioned earlier in case of the L/S band filter the metallic wall is replaced by a fence of equally spaced TSV's obtained by standard silicon bulk micromachining. Unfortunately these via's are very large and have therefore a direct impact on the overall filter footprint. In order to reduce the size of the L/S band filter a supplementary activity on alternative ways to build the via holes was launched. DRIE was employed in a novel way for the manufacturing of tapered wall via holes with different aspect ratio [123,124] and a few different methods of metallization of the via holes were explored experimentally.

7.2 Short Overview of Enabling Technologies For TSV Manufacturing

Through Wafer Via (TWV) holes manufacturing can be done using different techniques, the most common being powder blasting, laser ablation or melt cutting and wet or dry etching. Each technique has its own distinguish characteristics and can be used according to the need. These includes chemical wet etching or plasma etching, laser drilling, powder blasting, and DRIE [125, 126]. A comparison of the results obtained using all these techniques showed that the DRIE technique is superior to all others mainly in respect of pattern transfer accuracy and minimum achievable dimensions, but also considering the side effects or wall roughness.

DRIE processes also have other advantages over competing technologies. Depending on the plasma recipe used, it is possible to obtain different degrees of isotropy during the processes. This can be used to obtain vertical walls with a high aspect ratio, up to 20:1 [127], tapered walls [121] or even isotropic etchings [128]. Moreover, due to the possibility of changing the degree of isotropy during the etching process by modifying the plasma composition, it is possible to manufacture structures which cannot be obtained using only isotropic or anisotropic processes [129].

7.3 Manufacturing Method

The manufacturing method consist in alternate repetition of anisotropic and isotropic etching processes. Each process has its own role during tapered via fabrication: anisotropic etching is used to achieve the depth, while the isotropic etching main role is to enlarge via's on one side in order to obtain the desired angle. Actually, the manufacturing process resides in successive anisotropic and isotropic etching cycles, step by step reaching the depth and

enlarging the via. A supplementary process is necessary before isotropic etching steps to achieve the desired shape i.e. an oxygen plasma cleaning. Anisotropic etching, based on the Bosch process, consist in successive short etching and passivation steps to achieve high etching rates and aspect ratio (up to 20:1). The Oxygen plasma is needed to remove the passivation deposit on the walls during the anisotropic etching without these steps cavities in bulk silicon will be obtained [130]. Fig. 7.1 shows schematically the main etching steps used for tapered walls manufacturing using the variable isotropy method.

A critical aspect is the wall roughness, which can affect the quality of barrier and seed layer deposition mainly when small angles are desired (in the order of a few degrees). Because the anisotropic etchings are based on a high etching rate Bosch process, a pronounced scalloping effect is expected over the walls, with a roughness of up to 1 micron. This residual roughness can be reduced either by selective corrugation (scalloping) removal using the method reported in [131](consisting in a short wet etching) or by using different anisotropic etching recipes that provide smaller roughness from the beginning. Also, isotropic etching processes can be employed to reduce the roughness, as they have a polishing effect over the surfaces, but only if there is enough space that allow large angles.

Via holes manufacturing begins with thermal oxidation of the wafers, followed by thick resist (10 μm) deposition and patterning; windows with diameters of 20 μm and 100 μm respectively were used for the TWV's manufacturing tests and RIE was used to remove the SiO_2 after resist patterning (Fig. 7.1a). Due to selectivity problems both SiO_2 and resist layers are used as masking layers during TWV manufacturing and the thermal oxide thickness should be chosen in function of the wafer thickness.

Via holes manufacturing continues with an anisotropic etching step, following the method described above: etching cycles mainly based on anisotropic

and isotropic etching steps, as shown in Fig. 7.1(b, c). Etching cycles are repeated until the opposite surface of the wafer is reached, see Fig. 7.1(d, e). The whole DRIE process starts and ends with anisotropic etching steps to obtain a good definition of the via holes on both sides. An Alcatel AMS200 deep plasma etching system [131] was used for via holes manufacturing.

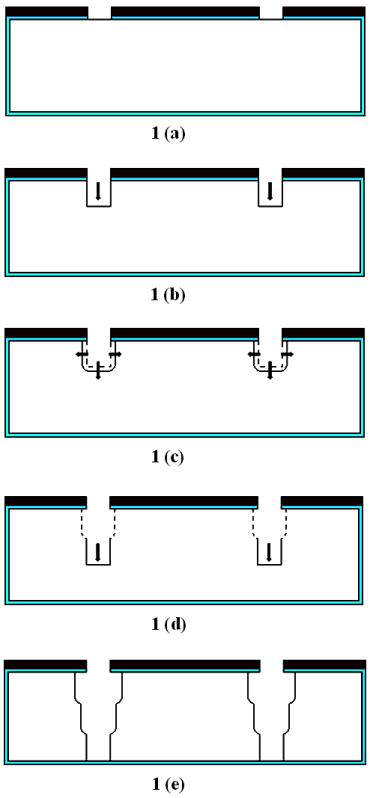


Figure 7.1: Schematic view of the dry etching method used for tapered via manufacturing: (a) Thermal oxidation, resist deposition and patterning; SiO_2 etching, (b) Anisotropic etching step (c) Isotropic etching step, used to enlarge the via on the top side, (d) New etching cycle start, (e) Etching cycles are repeated until the opposite side of the wafer is reached.

The TWVs profile is actually formed by vertical walls provided by anisotropic etchings and curvatures formed by isotropic etchings. Long isotropic etchings significantly change the hole shape, having a polishing effect over the walls and allowing to obtain a real continuous tilted wall; but, for small angles,

the obtained shapes are similar to that presented in Fig. 7.1(e).

The average tilt angle α is computed considering the front and bottom side via openings by using the following formula:

$$\alpha = \tan^{-1} \frac{L - l}{2h} \tag{7.1}$$

where (L) is the via diameter on the front side, (l) the via diameter on the bottom side and (h) the wafer thickness.

If the etching rates of both isotropic and anisotropic processes are known then the process recipe can be optimized in order to obtain a specific angle; to obtain an angle α on a wafer with thickness (h) a lateral etching (l_i) has to be obtained by the isotropic etching:

$$l_i = \frac{L - l}{2} = htg\alpha \tag{7.2}$$

considering (n) etching cycles, and a medium etching rate (r_i), etching time for each step $(t_{i/s})$ is given by:

$$t_{i/s} = \frac{l_i}{nr_i} \tag{7.3}$$

For anisotropic etching steps, the remaining wafer thickness $(h - l_i)$ should be etched in $(n + l)$ steps with an average etching rate of (r_a). Therefore the etching time $(t_{a/s})$ for each step is given by:

$$t_{a/s} = \frac{\frac{h - l_i}{n + l}}{r_a} \tag{7.4}$$

This process can be further optimized by considering also the etching rate reduction as function of depth, but in general full characterization of the process for aspect ratio higher than 10:1 (when this effect is important) requires a lot of individual etch tests for each via dimension. Instead using average etching rates a lower number of optimization steps is necessary to achieve the shape with a good control over the wall angles.

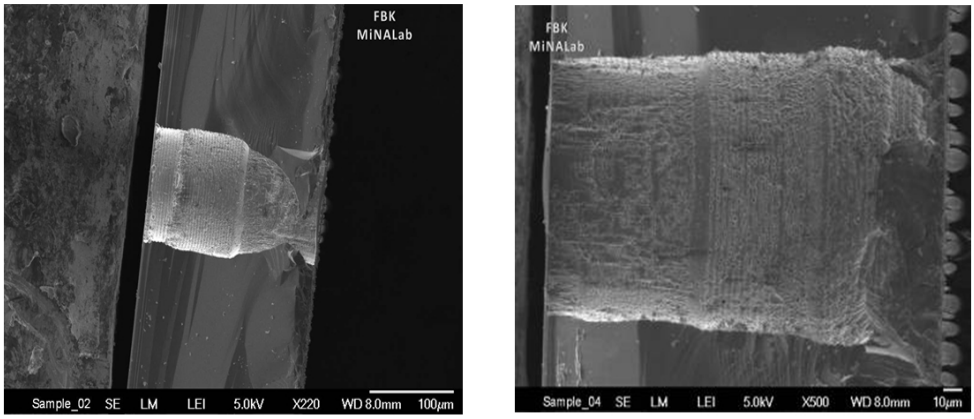
7.4 Process Optimization

Wafers with having thickness of: 200 μm, 300 μm and 500 μm were used in the TWVs manufacturing process. All wafers were <100> oriented. The resistivity range included > 5000 Ω cm, 0.01 - 0.02 Ωcm for and 8 - 10 Ωcm 200, 300 and 500 μm thick wafers respectively.

In order to obtain different via profiles three different anisotropic etching recipes were used, which are characterized by different etching rates and wall roughness:

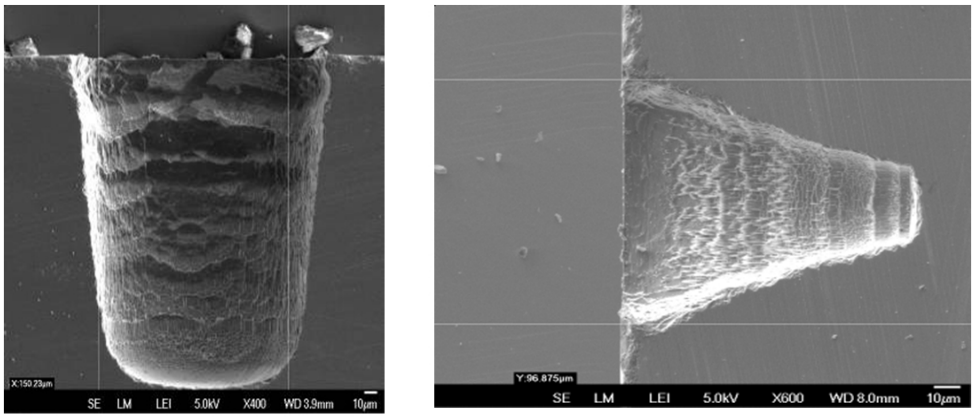
- a high etching rate recipe, characterized by rough walls
- a recipe with smaller gas flow and power that provides smoother walls but has smaller etching rates
- a recipe with very small gas flow, power and etching rate for very smooth walls.

Considering the Aspect Ratio Dependent Effect (ARDE) [132] each process was optimized for each via dimension. TWV's with 100 μm diameter were developed on 200 μm using two processes (anisotropic and isotropic) with a different number of cycles: two and four respectively. Fig. 7.2(a, b) shows anisotropic and isotropic etching steps. Measurements showed an etching rate of about 17 μm/min for the anisotropic etching and a lateral etching of about 6.5 μm when the smaller number of steps were used (Fig. 7.2a) and about 10 μm for the higher number of steps (Fig. 7.2b). Measured lateral etchings correspond roughly to 1.8° and 2.9° respectively.



(a) (b)

Figure 7.2: SEM photo of 100 μm diameter TSV manufactured on 200 μm thick silicon wafer: (a) 2 etching cycles, (b) 4 etching cycles.



(a) (b)

Figure 7.3: SEM photos of the manufactured holes in 500 μm thick wafers using second anisotropic etching recipe: (a) 100 μm diameter, (b) 20 μm diameter.

On 500 μm thick wafers via's with 100 μm and 20 μm diameters were developed, Fig. 7.3(a) and 7.4(a). Due to variations in the etching recipes and the corresponding etching cycles the mouth diameter of the via's were enlarged and related angles were in the range of 15° to 18°. Etching rates of the anisotropic processes were reduced with respect to first recipe by 50% for the second recipe ($\approx$8.5 μm/min) and at about 20% for the third one ($\sim$3.5 μm/min).

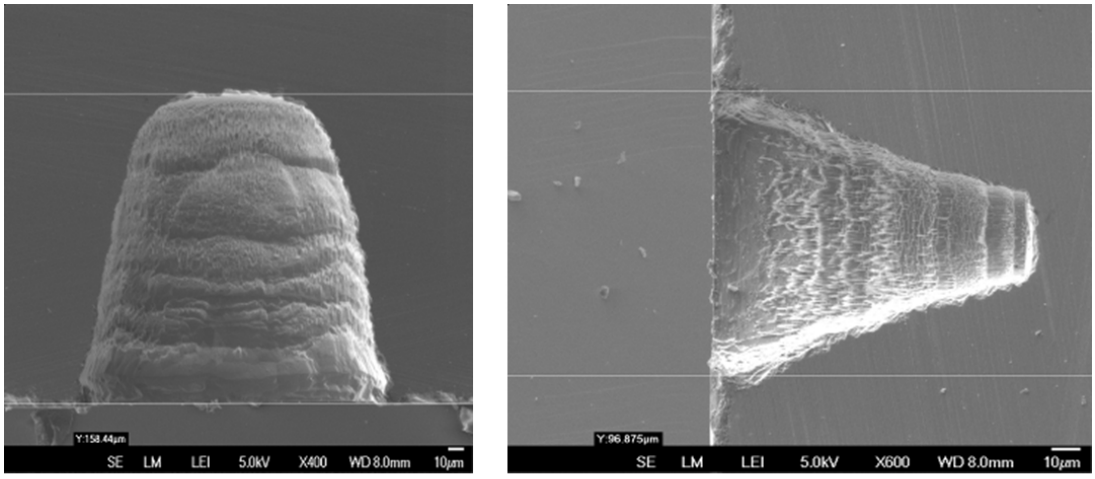


Figure 7.4: SEM photos of the manufactured holes in 500 μm thick wafers using third anisotropic etching recipe: (a) 100 μm diameter, (b) 20 μm diameter.

For 20 μm diameter holes (Fig. 7.3(b) and 7.4(b)), measured lateral etchings were about 30 μm around the mask (30 μm to 35 μm), but due to the ARDE effect etching depth was smaller (100 μm to 130 μm); computed angles were between 15° and 19°. Next the manufactured structures were used to verify the quality of seed layer deposition inside holes. Fig. 7.5(a) present a SEM photo after selective corrugation removal (TMAH 25%, 74°, 10 min.) using the solution provided in [131] and seed layer deposition (Cr/Au, 5/150 nm); in this case, due to the residual scalloping, the deposited layers are not continuous on the bottom part of the TWV's. On the other two samples a good coverage all over the walls can be seen, see Fig. 7.5(b, c), including nanometer spikes, even when depositing a thinner gold layer (100 nm instead 150 nm).

The optimized process was used for TSV manufacturing on 300 μm thick low resistivity (0.01-0.02 Ωcm) wafers. The DRIE processing used in this case consisted in seven anisotropic and six isotropic etching steps. 20 μm and 100 μm masks were used and target lateral etchings were 120 μm (60 μm each side), which obtained a 11.3° angle and 240 μm (120 μm each side)

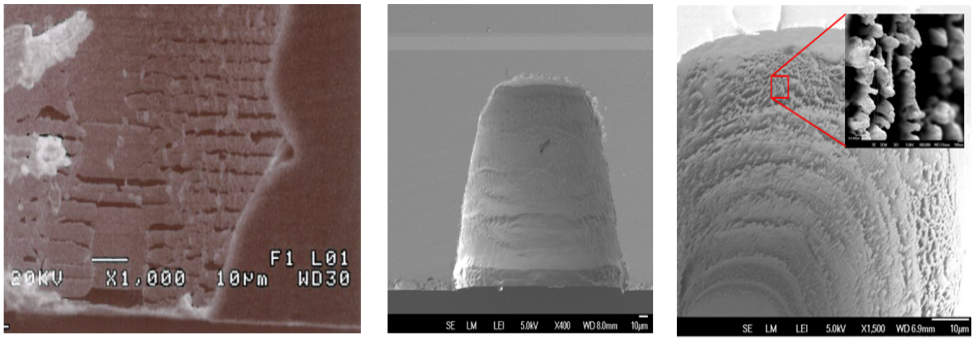


Figure 7.5: SEM photo after CrAu deposition: (a) Cross section of metalized 100 μm diameter via, walls angle $\approx 2°$, (b) Cross section of 100 μm diameter hole, $\approx 15°$ walls angle, (c) Top view of 20 μm diameter hole, $\approx 18°$ angle and detail of the internal surface.

which achieved a 22.8° angle.

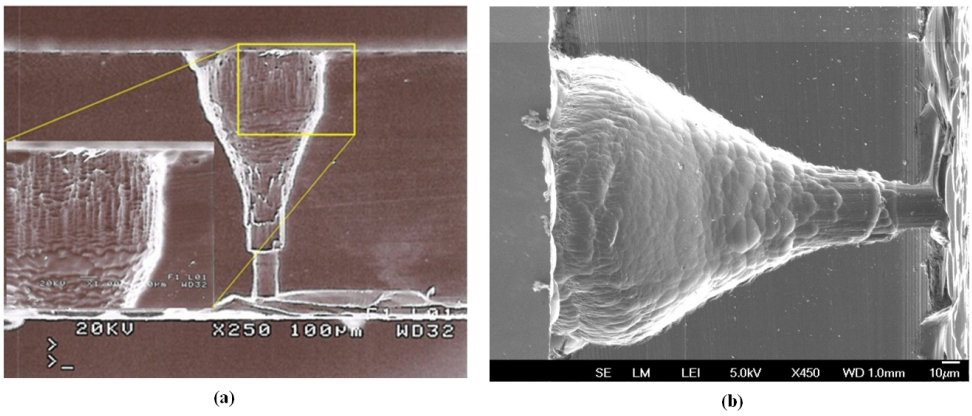
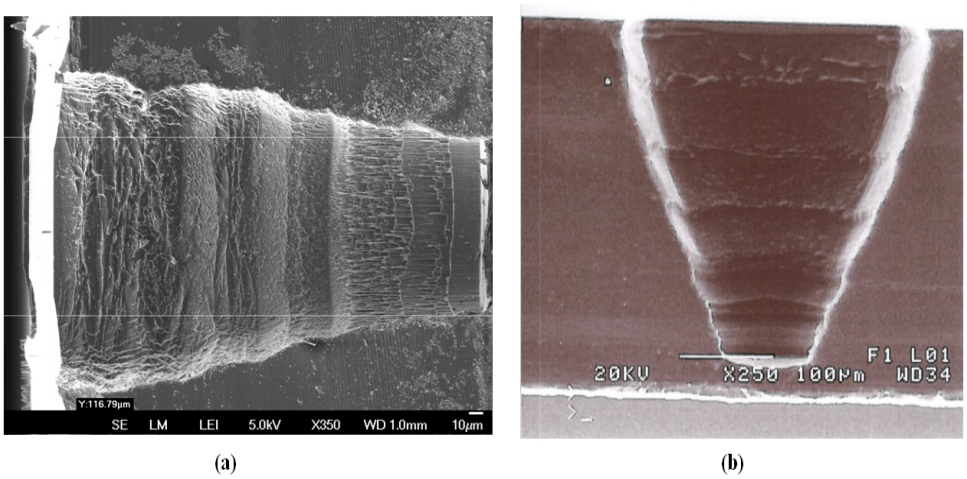


Figure 7.6: SEM photos of TWV's manufactured on 300 μm thick silicon using a 20 μm diameter mask: (a) TWV with wall angle of $\sim 10.3°$, (b) TWV with wall angle of $\approx 15.2°$.

Fig. 7.6 presents SEM photos of the cross section and detail of the wall surface of the 20μm diameter TWV; in this case the high etching rate recipe was used for the via manufacturing due to the substantially decrease of the etching rates for deep etchings of the other two recipes. The same effect can be seen also for isotropic etching steps on the bottom side enlargement the effect is very small.

The 100 μm diameter TWV's are presented in Fig. 7.7. Due to the smaller

aspect ratio, isotropic and anisotropic etching steps can be distinguished clearly for smaller angles, see Fig. 7.7(a), while for bigger angles an almost continuous shape can be seen in Fig. 7.7(b), without significant changes of etching rate.



(a) (b)

Figure 7.7: SEM photos of TSV's manufactured on 300 μm thick silicon using a 100 μm diameter mask: (a) TWV with wall angle of $\approx 10.6°$, (b) TWV with wall angle of $\approx 21°$ (before final anisotropic etching).

Measurements performed on TWV's designed to have 11.3° showed a good correspondence after process optimization: for 20 μm diameter via's angles obtained were $\sim$10.3°, while for 100 μm angles were $\sim$10.6°. These angles correspond to lateral etchings of about 54.5 μm and 56 μm respectively (instead of 60 μm), leading to errors of about 9.17% in first case and about 6.67% in the second one.

For tapered wall TWV's, designed for 22.8°, an excellent agreement was obtained for the 100 μm diameter mask: the lateral etching of about 115 μm (instead 120 μm) offers an angle of $\sim$21° with an error of about 4%. For 20 μm diameter mask isotropic etching rate decreased drastically due to the much higher aspect ratio (15:1), achieving only $\sim$82 μm lateral etching and an angle of about 15.2° with an error of 31.7%.

7.5 Metallization of TWV's

The metallization of the via's resulted in a challenging task and the level of difficulty increased with smaller via diameter and larger via depth. In order to optimize the via-filling process two types of plating materials were used, i.e. gold (Au) [133] and copper (Cu) [134–136]. Due to its unique characteristics (e.g. high thermal conductivity, low electrical resistance, oxidation resistance) Au is the preferable choice for applications at RF frequencies but on the other hand it is an expensive material and Au filled via's significantly increase the total cost of manufacturing of a device. In order to keep the cost low the use of Cu was also explored for via's filling. Both types of plating chemistries are briefly described in the following sections.

7.5.1 Gold (Au) Filled Via's

The fabricated tapered via holes were electroplated with gold in order to make the TWV's conductive. For this purpose via holes with 20 μm diameter were chosen. After thermal oxidation (about 300 nm), barrier and seed layers (Cr/Au, 50/100 nm) respectively were deposited by e-beam evaporation. These layers are necessary to improve adhesion and to reduce conductive layer diffusion into the substrate; the deposition was performed from the wafer front side and achieved a very good coverage of the walls, as illustrated in Fig. 7.8. On the same side a dry resist film with a thickness of 30 μm was applied and patterned to restrict the electroplating process on the via area, see Fig. 7.8.

After a long wetting, in order to allow the solution to penetrate into the holes, electroplating was performed for one hour using a medium current density of 5 mA/cm^2.

The result is shown in Fig. 7.9. The whole narrow part of the tapered via hole was filled to a depth between 50 and 70 μm for all via's allowing a

subsequent processing of the wafer at least on one side. On the remaining part of the tapered via hole the deposited layer on the side walls was much thinner, see Fig. 7.10.

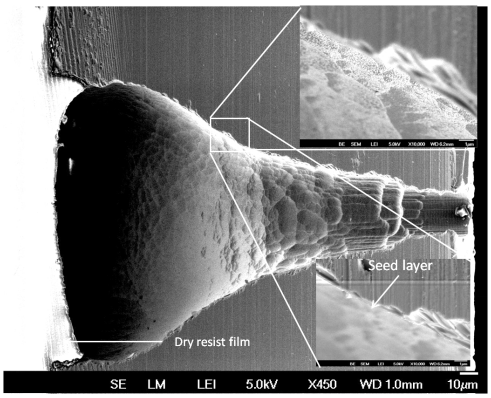


Figure 7.8: SEM photos of a TWV after seed layer deposition (details) and dry photo resist film application.

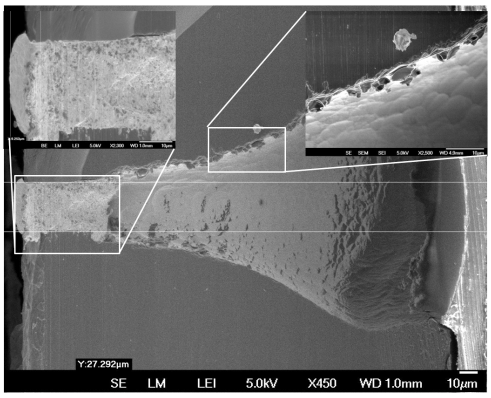


Figure 7.9: SEM photos of the TWV after gold electroplating.

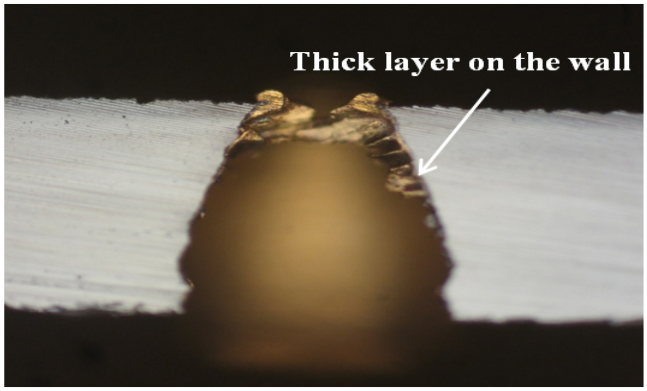


Figure 7.10: SEM image of TSV showing a thicker seed deposited on the side wall of via.

This may be due to the limited exchange (mass transport) of the plating solution between the inside of the via's and the bulk of the solution, determined by the small size of the via holes; in addition during the plating process these openings become smaller and finally the exchange of plating solution inside the via's was stopped completely.

7.5.2 Copper (Cu) Filled Via's

As pointed out above with gold electroplating it was possible to fill the via till to a depth of 50 - 70 μm. Two problems affect the approach to fill the via's completely with gold:

- due to the big quantity of gold needed to fill TSVs cost will increase too much making this solution inconvenient from the economical point of view.
- due to the use of DC electroplating, the uniformity and homogeneity of the deposited gold layers were poor.

In order to avoid the above mentioned problems an alternative metal for the via filling by electroplating was searched. Due to its much higher deposition rate in narrow spaces copper electroplating was selected.

Among the many different formulations commercially available two Cu plating solutions were tested, **InterVia^{TM} Cu 8540** (Rohm & Haas) and **Cuprum 33** (ELSY Research); the first one (using bath formula I, INTERVIA 8500) is expressively dedicated to via filling and therefore the main effort was focused in this direction. While the second solution is sold already prepared, the first one has 3 components: the main component, InterVia Cu 8500/8501/8502 (with different concentrations of copper sulfate) and two organic additives to control the brightness and plating properties, InterVia Cu 8540A & C respectively. Operating parameters for both solutions are presented in **Appendix "D"**.

Preliminary tests on TSV's were performed using Cuprum 33 plating solution, on vertical wall and tapered wall via's. For this tests the plating time ranged between 10 and 30 minutes and were performed with both sides of the via's opened or covering one side by dry resist. For all these tests the seed layer (Ti/Au/Ti 50/100/50 nm) was deposited from the top side. Results obtained are presented in Fig. 7.11 and Fig. 7.12 for vertical via's.

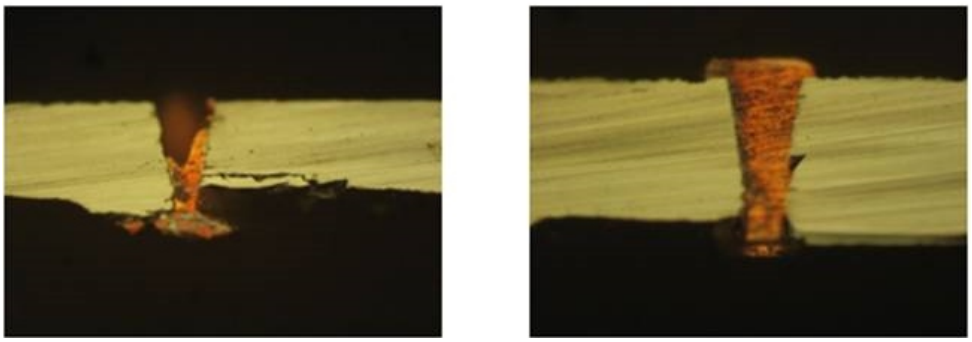


Figure 7.11: Cu DC plating using Cuprum 33 solution and both side open after 30 min of plating.

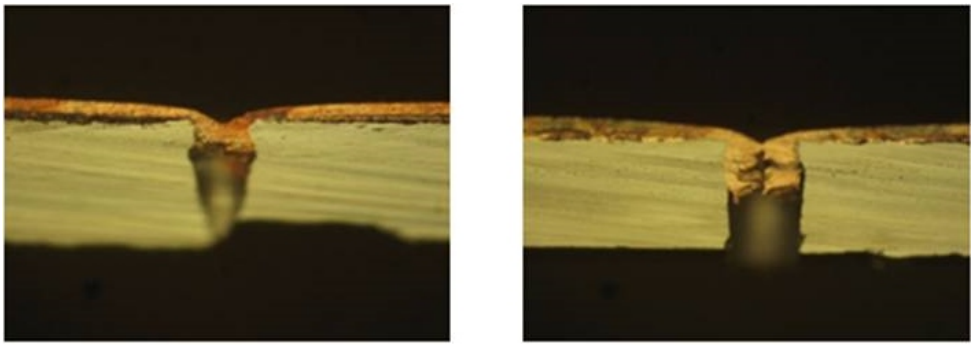


Figure 7.12: Cu DC plating using Cuprum 33 solution and one side covered after 30 min of plating.

In both cases there was a problem with the seed layer deposition inside the via's and due to this non-uniform Cu deposition inside the TSVs resulted. Another problem was Cu adhesion.

Fig. 7.13 shows the results obtained by using tapered wall TSVs having 20 μm diameter on the back side; the seed layer was deposited from the top.

There are some problems in the narrow part of the TSV. In this case the deposition parameters were modified to improve uniformity current densities used in this case ranged between 2.6 A/dm^2 and 3.3 A/dm^2. Also, pulse plating tests were performed using a current density of 2.6 A/dm^2 and time of 800 μs for forward pulse and 200 μs for reverse pulse.

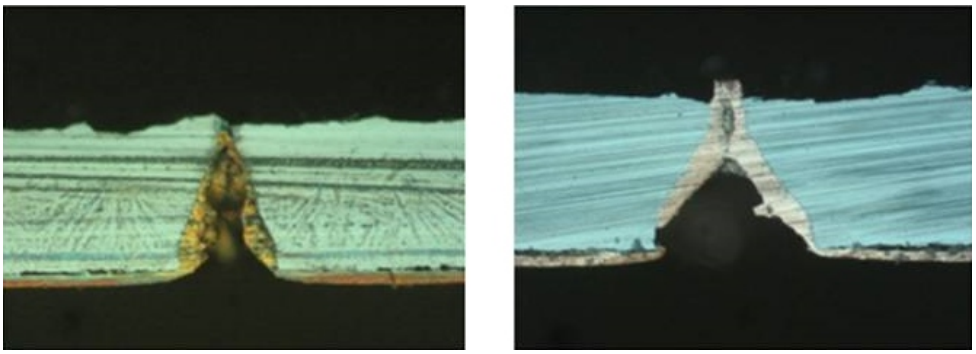


Figure 7.13: Cu deposition on DC tapered walls TSVs. (a) DC at 15 min and (b) Pulse at 20min.

In this case an improvement of deposition uniformity can be seen, but inside the via's the deposition is not homogenous, large holes are obvious in all cases with a slightly improvement for pulse deposition; adhesion of Cu remains a problem as for some wafers the deposited Cu layer was completely removed during wafer dicing. Poor adhesion was one of the main factors that pushed to consider the second plating solution.

First plating tests for **InterVia^{TM} Cu 8540** solution were performed in DC mode and results are presented in Fig. 7.14 showing the same problem of deposition homogeneity inside TSVs, but an improved adhesion of the deposited layers. The deposition parameters used were: temperature 23°C, agitation 60 rpm and a current density of 2.5 A/dm^2. The anode used for this plating solution was of the TiPt type because the plating surface was too large and in using a sacrificial Cu anode it is not possible to reach the needed current densities. The seed layer was deposited from the topside and was the same type as used before.

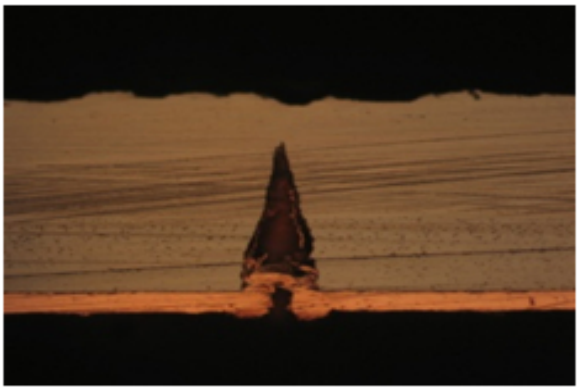


Figure 7.14: DC plating of tapered walls TSVs using InterVia^{TM} Cu 8540 solution for 40min.

Also this solution was tried first in DC conditions and later with pulsed current conditions. In DC plating conditions the deposition on TSVs having 100 μm diameter and with both sides open has a better uniformity of the deposition inside the via's, but on the backside a large amount of Cu is deposited (overburden), as demonstrated in Fig. 7.15.

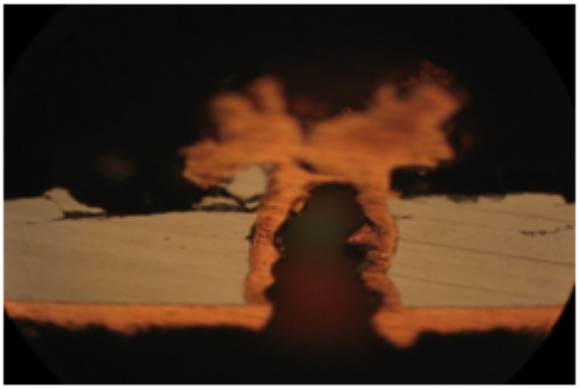


Figure 7.15: DC Cu plating on 100 μm diameter TSVs showing overburden for total deposition time 80 min.

Deposition in pulsed current condition was perform using wafers from the same manufacturing run, which implied that some of them had not an optimized profile. The seed layer used in this case was Cr/Au/Cr 2.5/25/2.5nm, unfortunately not thick enough for a good coverage of the TSVs walls as presented in Fig. 7.16.

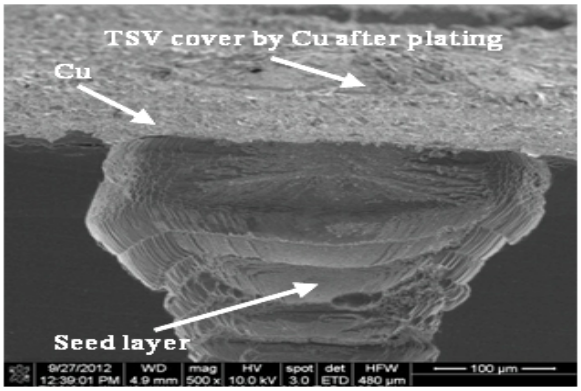


Figure 7.16: SEM photos of the seed layer deposited inside TSVs.

Parameters (e.g. temperature, agitation and forward current) for the pulsed current deposition were adjusted and Cu plating was performed. Results are presented in Fig. 7.17.

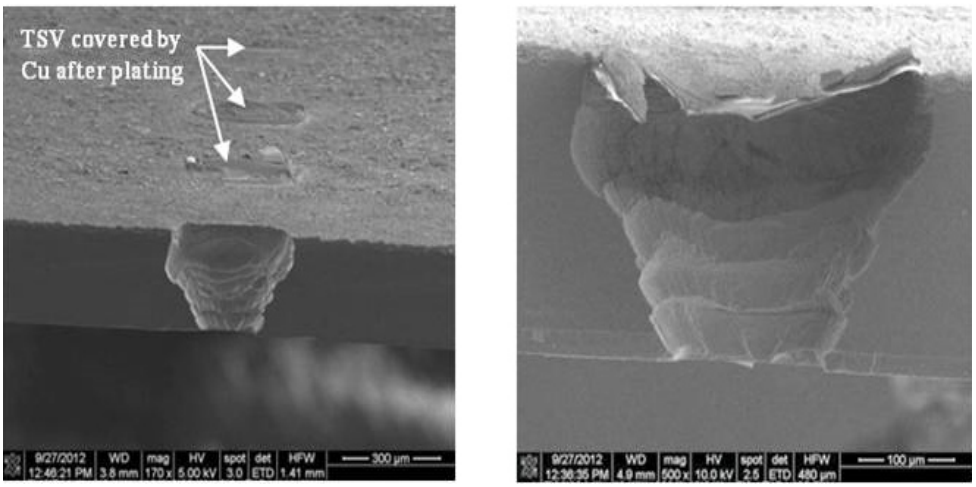


Figure 7.17: SEM photos of the TSVs after pulse Cu plating, 20 minutes.

SEM photos of the processed TSV's showed that many were covered by the deposited Cu layer, but the cross section reveled that only a superficial layer was deposited, with a thickness of about 8 μm, while the rest of the TSVs were actually empty.

7.5.3 Cu Etch Back

In order to find a viable way to overcome the overburden on one side of the TSV's a technique for Cu etch back was also studied on the prepared samples. For this diluted nitric acid (HNO_3, 65%) was used. Two diluted solutions were found to be suitable for our purpose:

- 1(HNO_3):4(H_2O), with an etching rate of about 0.1 mum/min
- 1(HNO_3):4(H_2O), having an etching rate of about 1.4 mum/min

Both solutions were used, first one for thin layers, second one for thicker ones, providing a good uniformity.

In conclusion the work so far performed on the development of a process module for TSV's produced a viable method to fabricate through wafer holes either vertical or tapered. This can be achieved by tailoring the etching recipes that mix in an appropriate way the isotropic and anisotropic etching recipes available for silicon etching. By smoothing the surface of the via walls with simple wet etching solutions it is possible to achieve the smooth walls suitable to be covered continuously by a metallic seed layer deposited by a simple PVD technique, without the need to use the more expensive sputtering technique.

The tricky part in the fabrication of metalized via holes turned out to be the metal filling. Still the most used technique world wide is the electroplating of suitable metals. Nonetheless plating is difficult due to the geometrical restriction represented by the via hole. This strongly influence the mass transport of the chemical components involved in the deposition process. Metals like gold, in principle very suited to the application due to its excellent physical characteristics, suffer from the fact that most plating solution have a low molar content of Au salt and are employed without sacrificial anode. This limits drastically the possibility to fill a deep and narrow via hole uniformly. To achieve this more sophisticated techniques like pulsed

current deposition are necessary in order to allow the solution in the via hole to exchange with the bulk solution outside. From this point of view a better-suited metal is copper as the typical plating solution has a much higher molar density and is typically used together with a sacrificial copper anode. In addition there exist on the market formulations for copper plating baths specifically developed for via filling. The first experiments performed with one of these plating baths showed better results but still put in evidence the shortcomings of a simple experimental set up for the plating.

In order to obtain a useful process module for TSV additional work and a better equipped plating facility is necessary.

Chapter 8

Results and Outlook

8.1 Introduction

After assembly both L/S and Ka band filters were characterized and tested in order to assess the technology and the designs. The original test plan foresees on the final fabricated output of both L/S and Ka band filters many different tests typically used to assess space compatibility as these are thermal shock and profiling, vibration, mechanical shock and both gross and fine leak tests. Due to technological difficulties pointed out above the assembly was finalized only for a relatively small number of devices and therefore the test plan for these test structures was revised accordingly.

Especially in case of L/S band filter, only 3 samples were completed as described in Section 6.8.2. 1 test transmission line on membrane (LS1), 1 single cavity device (LS2), and 1 double cavity (LS3). All samples are not hermetically sealed since a residual air-gap of about 2 μm is present on 2 sides of the structure due to a mask problem.

For the Ka band filter more samples were fabricated as described in Section 6.6, still a few with technological defects and not repeatable realization of the convex angles. For these reasons in phase 1 of the project the preliminary tests were focused only on the RF performance measurements and thermal shocks. The small number of items indeed discouraged to carry out any kind

of possibly destructive tests such leak test, vibration and mechanical shock.

Only a few test samples of single membrane resonators were submitted to a vibration test with an optical profiler in order to validate the mechanical simulations performed on the structure and to preliminary assess the sensibility of the structures to vibrations.

8.2 Radio Frequency Measurements on the Basic Devices

The RF measurements were performed by RF μtech at die level. The RF characteristics of the manufactured filters was evaluated by using the set up described in Fig. 8.1.

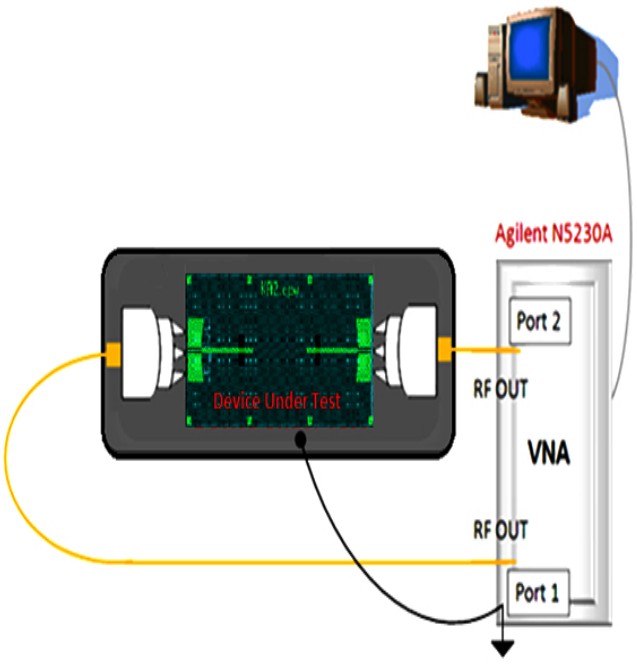


Figure 8.1: Test Setup for probe characterization of Filters with CPW access.

It consists of a 2 port Network Analyzer (PNA Network Analyzer - N5230A 10MHz-40GHz) connected to coplanar microprobes GSG (Ground-Signal-Ground, 200 μm pitch).

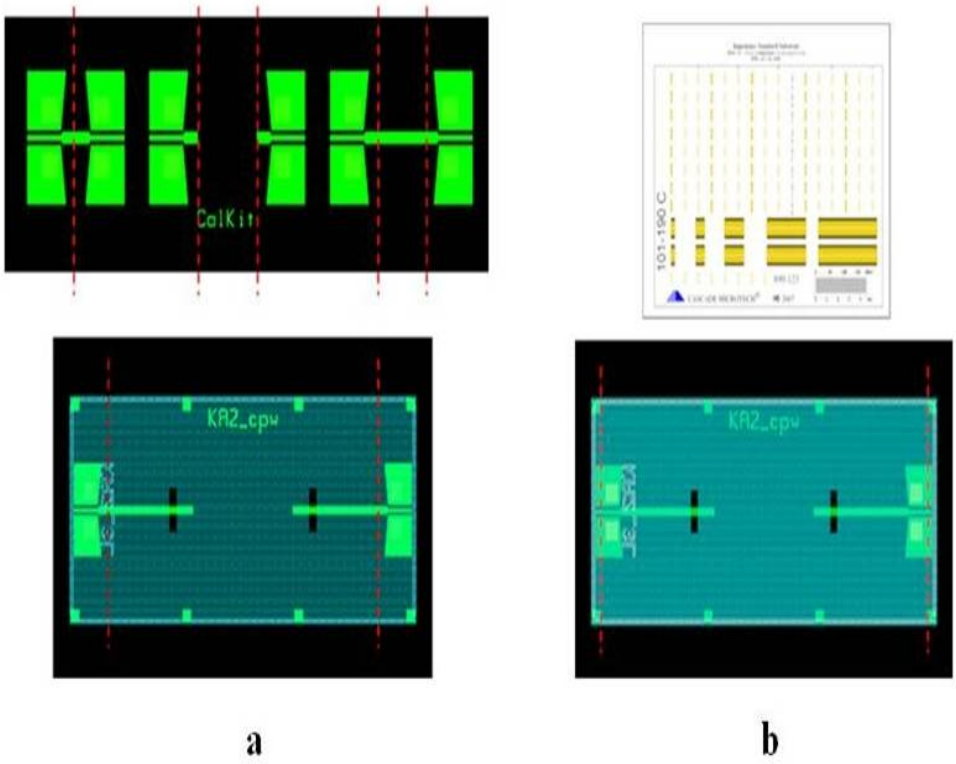


Figure 8.2: (a) TRL calibration kit and KA2_cpw with reference planes after TRL calibration (red dot line), and (b) SOLT calibration kit and KA2_cpw with reference planes after SOLT calibration (red dot line).

8.3 TRL and SOLT Calibration Techniques

For on-wafer measurements it was required to correct the measurements for the losses in the probes. Therefore calibration standards are needed in order to remove all the errors up to probe tip. Two types of calibration procedures, SOLT (Short-Open-Load-Thru) and TRL (Thru-Reflect-Line) were adopted. SOLT calibration was used to perform wideband characterizations and to remove from the measurement the contribution given by the connecting cables and microprobes. In SOLT calibration the reference planes are exactly at the RF probes position. While TRL calibration was performed to move the measurement reference plane at the microstrip filter ports (i.e. removing the loss contribution give by the coplanar-to-microstrip interconnections). How-

ever if the transitions (including the via's) are not exactly identical to each other, the TRL calibration is compromised and standard SOLT has to be preferred. The TRL calibration kit was realized on the same wafer with the filters while for the SOLT calibration a commercial calibration kit was used. The difference between the two types of calibration procedure is summarized in Fig. 8.2(a, b). For simplicity the measurements presented here are performed using SOLT calibration.

8.4 L/S Band Filter Testing

The filters were characterized in terms of insertion loss, return loss and group delay in the 10 MHz - 4 GHz range of the L/S band. Fig. 8.3 presents the devices on which the measurements were performed.

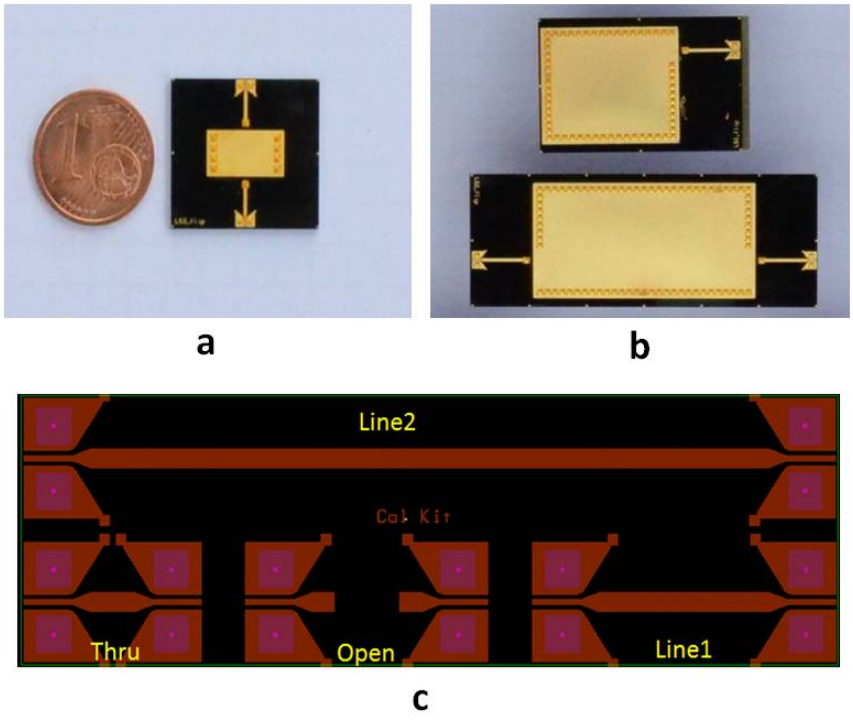


Figure 8.3: Photo of the L/S device: (a) LS1 flip, (b) LS2 flip (top) and LS3 flip (bottom), and (c) layout of the TRL Calibration Kit.

In case of L/S band filter three types of devices were realized. Therse devices are:

1. LS1: 2- port Back-to-Back Transition.

2. LS2: 1- port Resonator .

3. LS3: 2- port 2^{nd}-order filter with a negative sign central coupling (capacitive coupling).

In this case TRL calibration did not provide reliable results in the L/S frequency band due to some defects in the TSVs of line2 of the calibration kit. As an alternative standard SOLT calibration 0 - 10 GHz frequency range was employed to perform all measurements.

Firstly, "Thru" of the calibration kit was measured in order to evaluate the loss contribution of the coplanar-to-microstrip transition, which is included in all SOLT measurements. The measured insertion loss is 0.4 dB at 2 GHz. Next the LS3 structure was measured in order to verify the matching and the loss contribution of the filter input/output. A return loss of 16.6 dB and an insertion loss of 0.8 dB was measured for the back-to-back transmission line on membrane. The results are in line with the expectations, considering that 0.4 dB loss is due to the coplanar-to-microstrip interconnection.

The measured results for the LS2 and LS3 devices were compared with the HFSS simulations see Fig. 8.4 and Fig. 8.5. The poor matching between measurement and simulation is mainly due to the residual air gap created by the mask error, which is present on 2 sides of the structures. In order to verify this, a back simulation was done for the LS1 resonator considering the actual structure, i.e. including the air gap in the cavity walls. As expected the simulation (in magenta in Fig. 8.4) reproduces the trend of the measured performance much better.

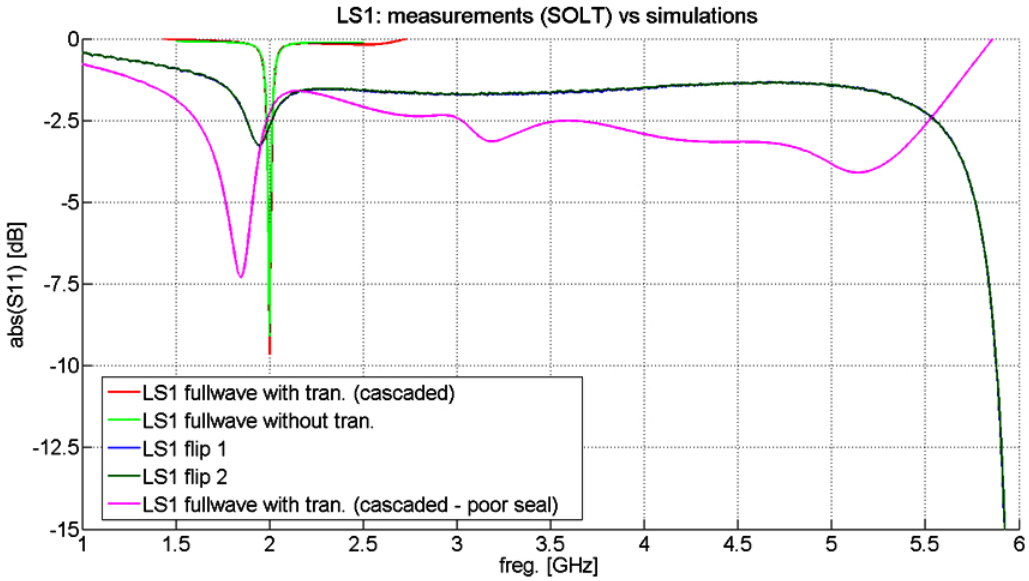


Figure 8.4: Measurement of the LS2 structure presented in (Fig. 8.3(a) bottom).

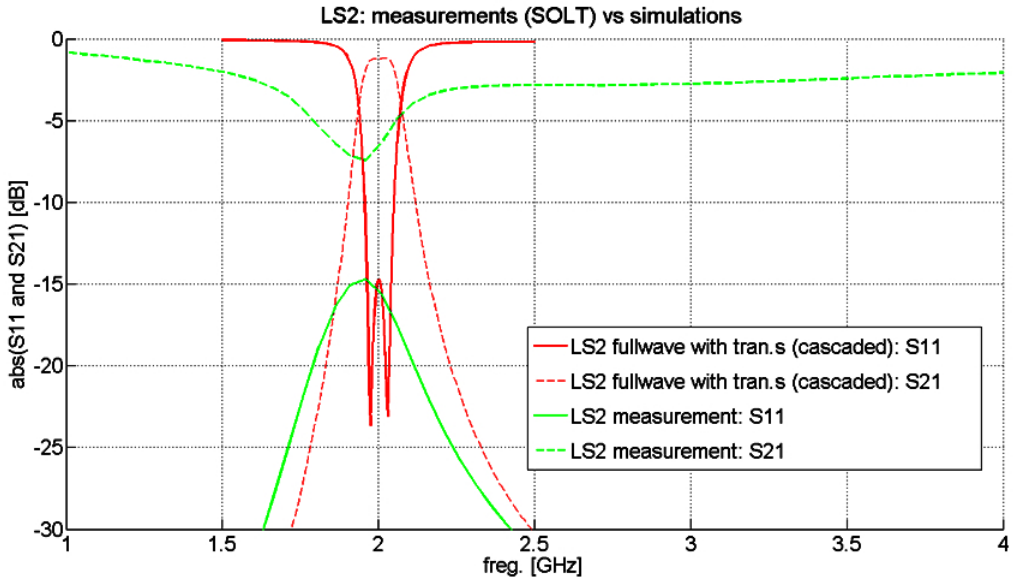


Figure 8.5: Measurement of the LS3 structure presented in (Fig. 8.3(a) up).

Thus, the reduced number of manufactured samples and imperfect enclosure did not allow to completely evaluate the filter performance. This is basically due to difficulties in the manufacturing process and because of

the large filter dimensions hampered the manufacturing of a significant number of devices within a standard silicon lot. Nonetheless it was possible to identify the critical processing aspects and how to correct them. With this information a successful implementation of these devices in the future is possible even if cost considerations may discourage the commercial exploitation of such a filter.

8.5 Ka Band Filter Testing

The Ka filters were also characterized in terms of insertion loss, return loss and group delay in the 20-40 GHz frequency band. The Q-factor was extrapolated from the loss response. 4 types of filters were realized:

- Ka 01: 1-port single half-wavelength reflection resonator.
- Ka 02: 2-port single half-wavelength transmission resonator.
- Ka 03: 2nd-order filter with a negative sign central coupling (capacitive coupling)-Filter A.
- Ka 04: 2nd-order filter with a positive sign central coupling (electric coupling)-Filter B.

Figs. 8.6 and 8.7 presents above mentioned filters. The measurement have been repeated on at least 2-3 samples for each filter type in order to preliminary monitor the measurement and process repeatability.

As mentioned in case of the Ka band filter a larger number of devices has been fabricated after preliminary screening of the building elements. In total 55 devices along with 4 repetition of calibration kit were handed over to RF μtech for performing RF measurements. RF tests were carried out on the “cpw" version, since the “flip" version needs first to be mounted on a test board. 3 types of MEMS Filters named KA1_cpw, KA2_cpw and KA3_cpw

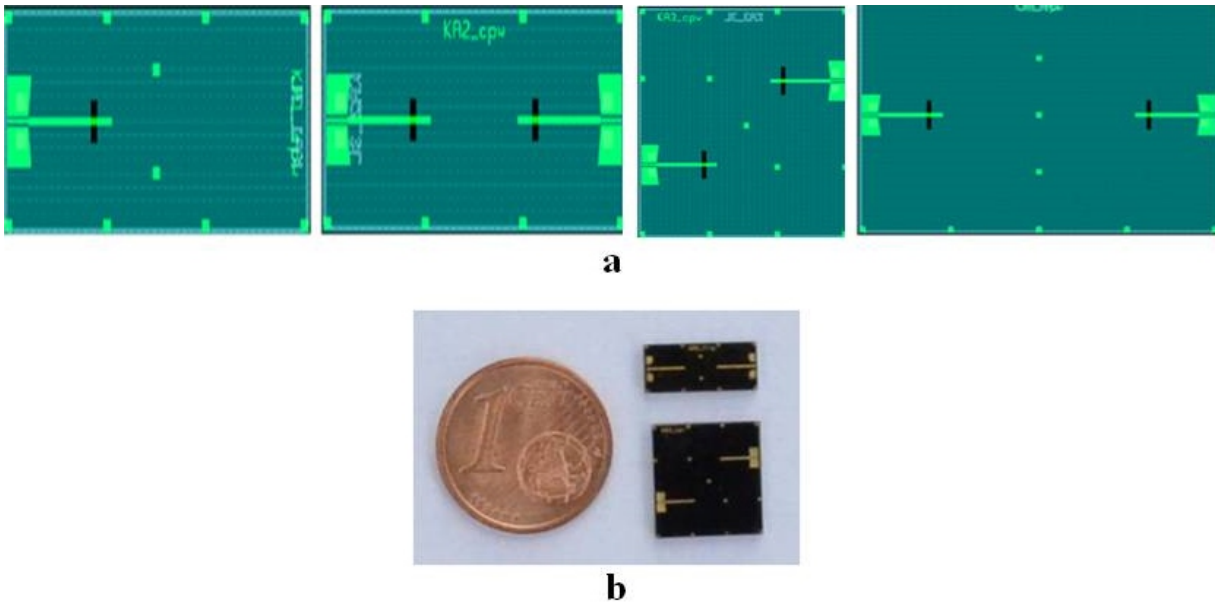


Figure 8.6: (a) Layouts of KA1_cpw, KA2_cpw, KA3_cpw and KA4_cpw to be measured using coplanar probes. (b) Photo of the Ka2_cpw and Ka3_cpw

were characterized using SOLT calibration and the set-up described in Section 8.2. KA4_cpw could not be measured since all samples present gold corrosions and defects in the RF input or output lines.

Initially a 3mm microstrip line with two coplanar-to-microstrip interconnections was measured in order to evaluated the loss contribution of the microstrip line and coplanar-to-microstrip transition. These losses are included in all SOLT measurements. The measured insertion loss is 0.525 dB at 30 GHz showing a good matching, see Fig. 8.8.

Then influence of the loss of the coplanar-to-microstrip transition on the filter response was analyzed. As expected the interconnections influence the “out of band" loss but not so significantly the Q-factor of the resonant cavity.

The first device to be analyzed was Ka2_cpw. The first sample namely “Ka2_cpw0" was measured and showed a pretty poor Q-factor and this was due to inappropriate bonding. After a re-bonding performed by FBK the device was measured again showing a significantly higher performance. The

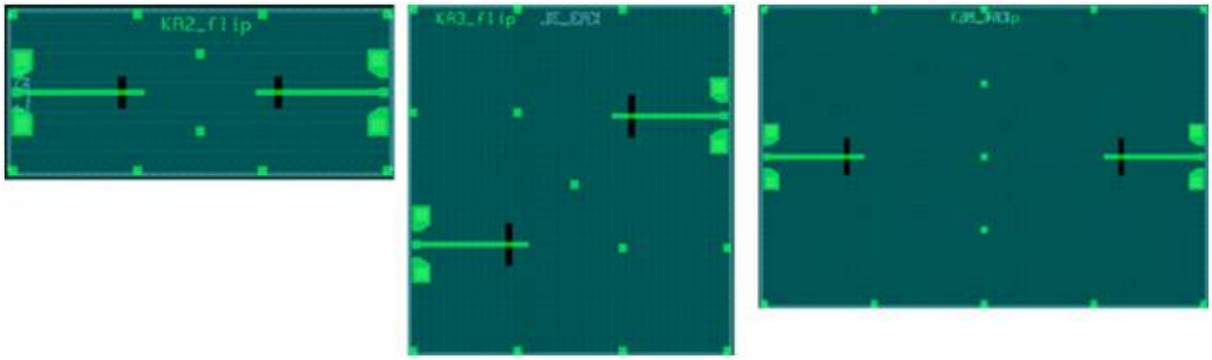


Figure 8.7: KA2_flip, KA3_flip and KA4_flip Layout to be ball-bumped on a test board (Surface Mountable Devices).

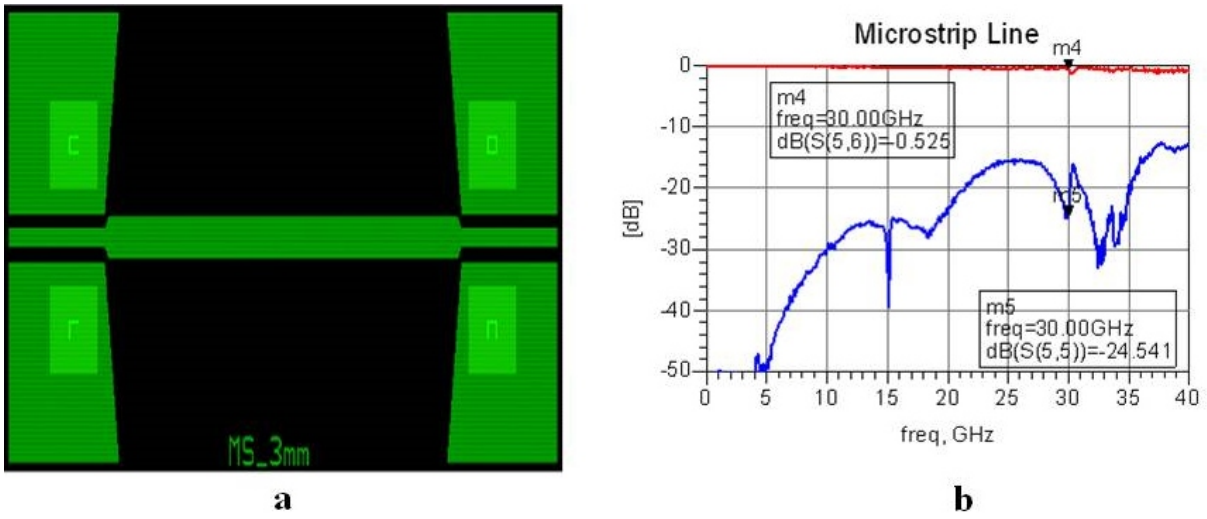


Figure 8.8: (a) Layout of the 3mm long Microstrip line and 1mm long cpw-to microstrip via transition. (b) Measured performance, return loss in blue and insertion loss in red.

fitted Q-factor of the device is about 500 (600 from HFSS simulations, considering: silicon permittivity =11; silicon tanδ = 0.005; gold conductivity = 4.1x10^7 S/m) and a relative frequency shift of less than 0.1 % was measured.

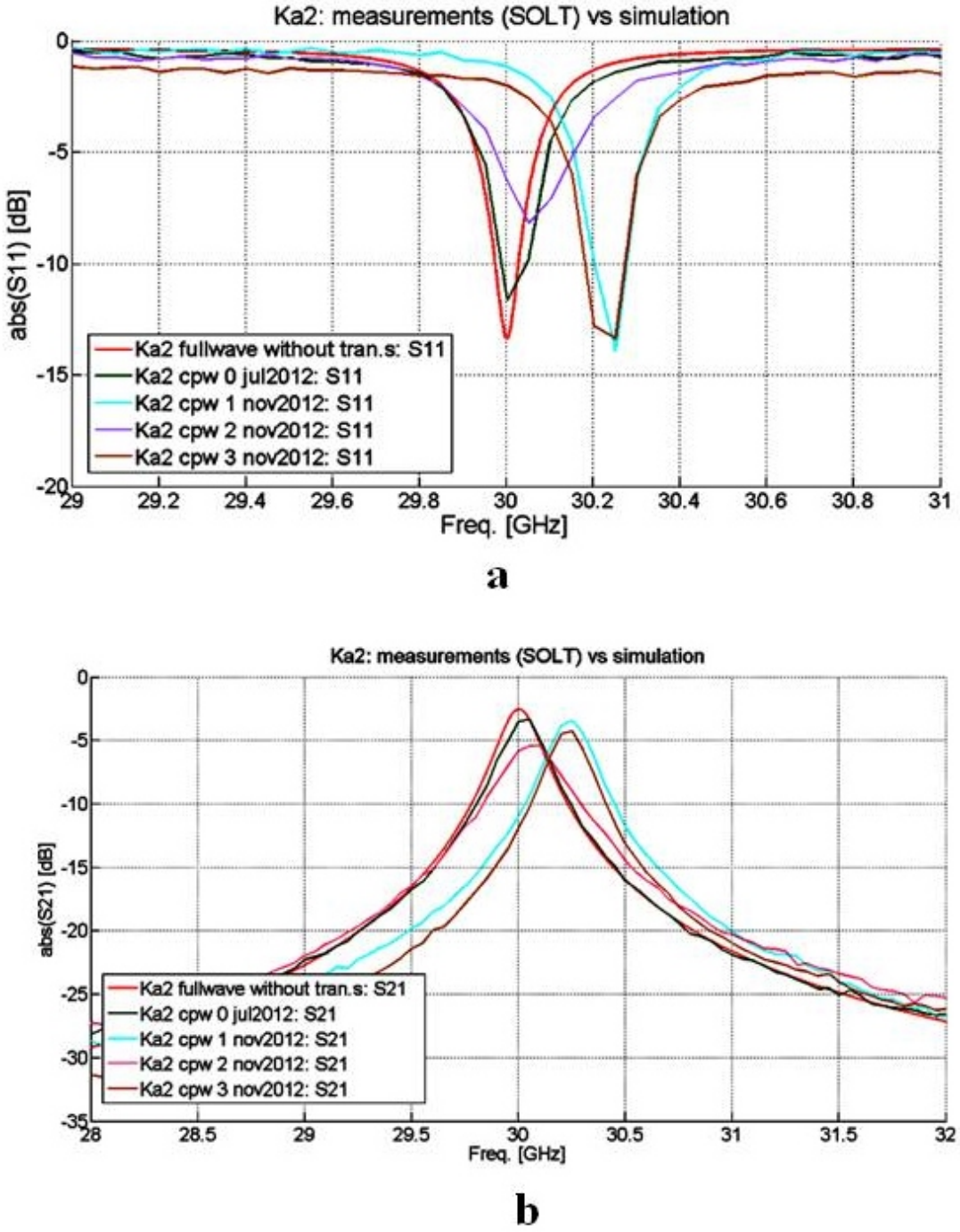


Figure 8.9: Ka2_cpw all samples. Comparison between simulation (in red) and measurements.(a) Return Loss, (b) Insertion Loss.

Fig. 8.9 shows the results of all “intact" Ka2_cpw samples, which are plotted in comparison with the simulation. With respect to the Ka2_cpw0

sample, the new ones showed similar Q-factors but a higher relative frequency shift ($\sim 0.7\%$). This shift is repeatable since it is present also in the Ka1 and Ka3 samples. This is very likely because larger etching time were employed for removing the "horns" from the cavities as explained above. The over etching may have modified the dimensions of the resonant section inside the cavity. To verify this one of the test device has to be "opened" so that the internal dimension can be measured. However in phase 2 very likely a different technique, based on DRIE is foreseen for the realization of the membranes and consequently this problem should not be anymore an issue.

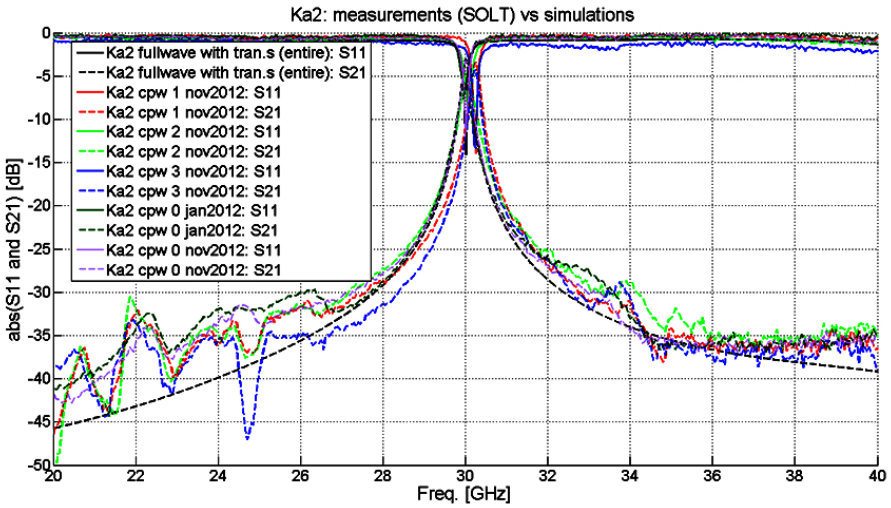


Figure 8.10: Ka2_cpw all intact samples, wideband performance.

Also wideband performance of the resonant cavity Ka2_cpw in Fig. 8.10 shows no spurious resonances in the 20 - 40 GHz frequency band.

A comparison with simulation for the Ka1_cpw and Ka3_cpw devices is presented in Fig. 8.11 and Fig. 8.12. The observations made for the Ka2 samples are also valid for these designs, indicating that the frequency shift is pretty repeatable. Also for these devices the fitted Q-factor is around 500 against the value of 600 predicted by the simulation.

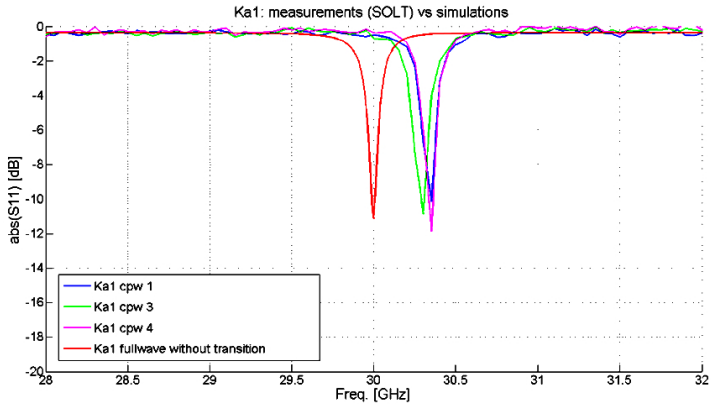


Figure 8.11: Ka2_cpw 3 samples. Comparison between simulation (in red) and measurements.

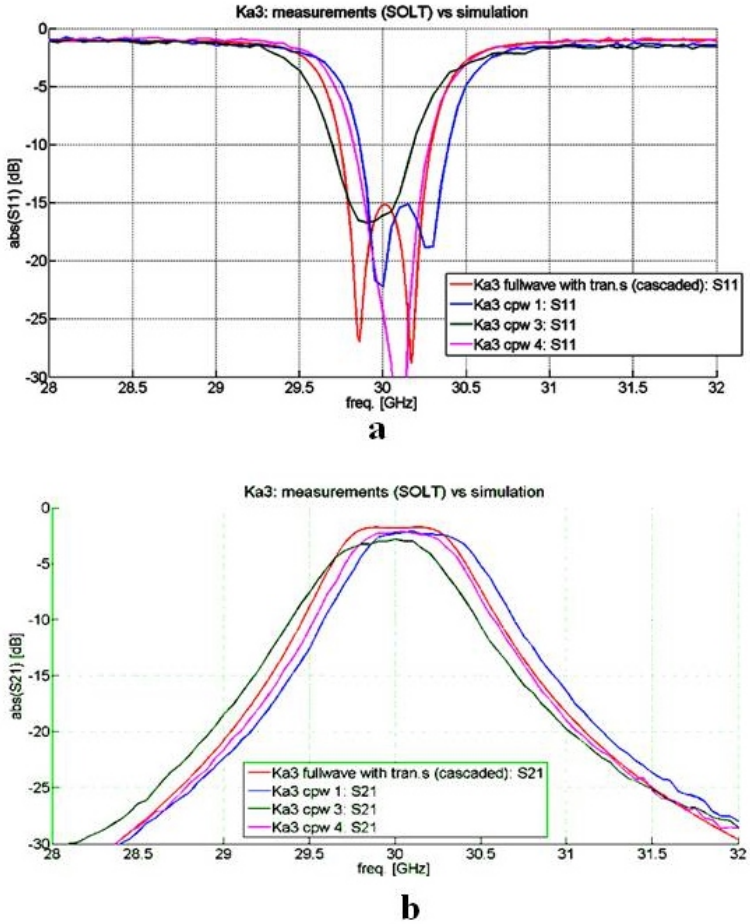


Figure 8.12: Ka3_cpw, all samples. Comparison between simulation (in red) and measurements. (a) Return Loss, (b) Insertion Loss.

8.6 Thermal Shock Test

After first RF measurements, the DUT (see, Fig. 8.13) was exposed to five thermal cycles from +90°C down to -30°C with a minimum period of 20 minutes for cycle. The transition from the hot ambient to the cold one should be as quick as possible and within 5 minutes at maximum. After the completion of the five cycles and the return of the DUT at ambient temperature a new RF measurement was performed in order to compare it with the first measurement.

Figure 8.13: DUTs in the climatic chamber after the completion of the last cycle.

The thermal shock test was done at Elital s.r.l. premises. An oven for the hot ambient and a climatic chamber set to -30°C for the cold ambient was used. The small oven can be accessed by a classic front door. The climatic chamber can be accessed by a small slit closed by thermal insulating material. A first attempt on items Ka2 cpw, Ka4 cpw n.1 and n.2 in the temperature range of (+60°C, -15°C) was done in order to evaluate the toughness of the MEMS increasing gradually the temperature range up to (+100°C, -30°C). After five complete cycles, a visual inspection at microscope highlighted no

cracks or mechanical deformations.

Due to a fall of roughly 10°C of the oven chamber temperature when the door is open, the set point was adjusted to 100°C to take some margins. The extraction of the tray from the oven to and from the climatic chamber was completed within 10 seconds, the DUT were subjected to two rapid temperature changes (100° to 18°, 18° to -30° and reverse), each within 2 seconds, with a mean rate of 13°C/s. After five complete cycles all items maintained their original aspect, as shown in Fig. 8.14.

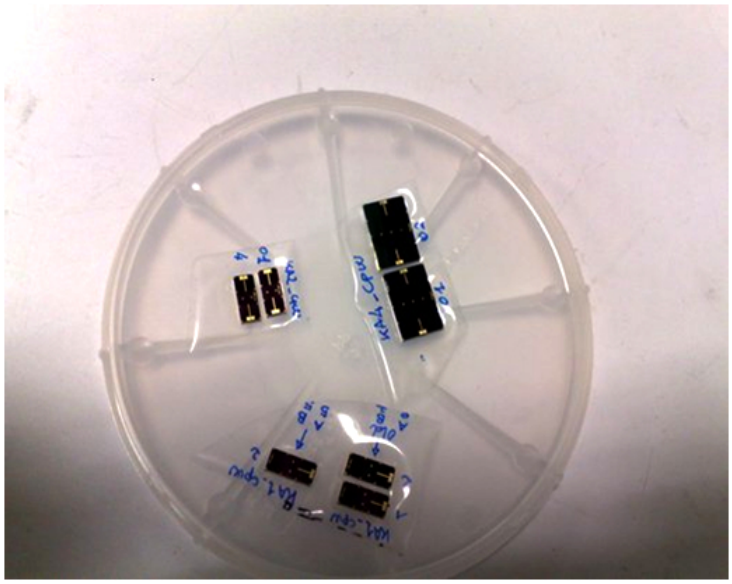


Figure 8.14: DUTs after the test.

8.7 Integration on Test Board and Thermal Profiling

To demonstrate the compatibility of the Ka band filters with Surface Mount Technology (see Fig. 8.15), a test board has been designed and manufactured for the Ka2_flip design. The test board in addition allows performing thermal profiling at Elital, since the monitoring of the S-parameters in the climatic chamber can only be done on connectorized devices.

The board characteristics are summarized in the following:

- Substrate: RogerRO4003C
  Er = 3.38 at 10GHz
  tanδ = 0.0027 at 10GHz
  CTE = 11(x) - 14 (y) - 46 (z) ppm/C°

- Metal frame for mechanical support

- RF Connectors: End Launch, Southwest

Ball-bumping techniques are required to mount the filter is series with respect to a microstrip line. After a first attempt at FBK, it was found that the machinery necessary for such high precision mounting cannot easily be set up by FBK in this moment. For this reason the ball-bumping service will be an external service to be completed in phase 2.

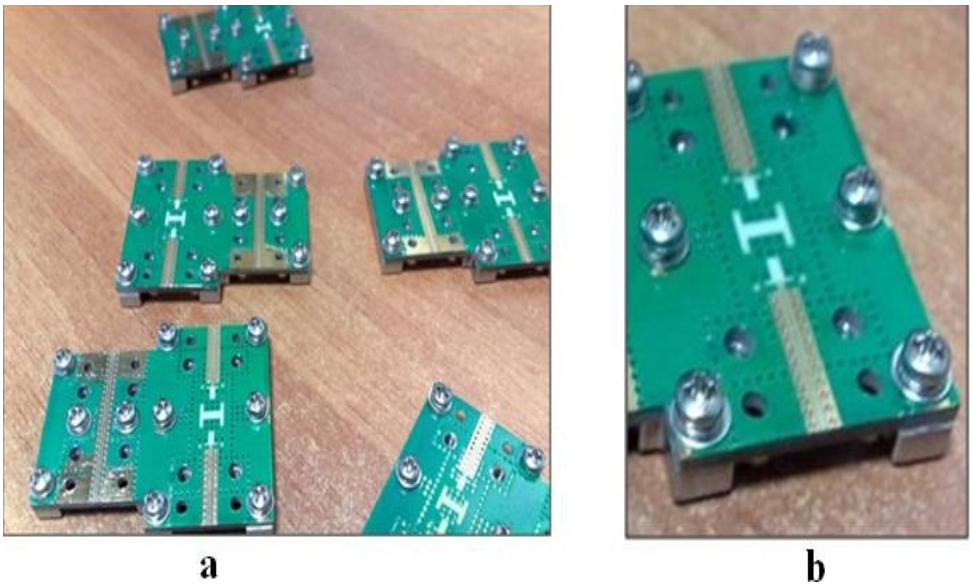


Figure 8.15: (a) The PCB boards with Ka filter footprint and the support carrier. (b) PCB detail.

8.8 Vibration Analysis of The Resonator Structures

In order to validate the numerical modeling once the first test samples were available a vibration test was performed on selected test structures of Ka band filters to experimentally verify that the prepared membranes are able to withstand the expected Sine and Random low frequency excitation of a typical launcher without any damage. The measurements were performed at the **"University of Padova"** with an optical profiler from Polytech^R equipped with a Doppler laser unit. The vibration test sequence is shown in Fig. 8.16.

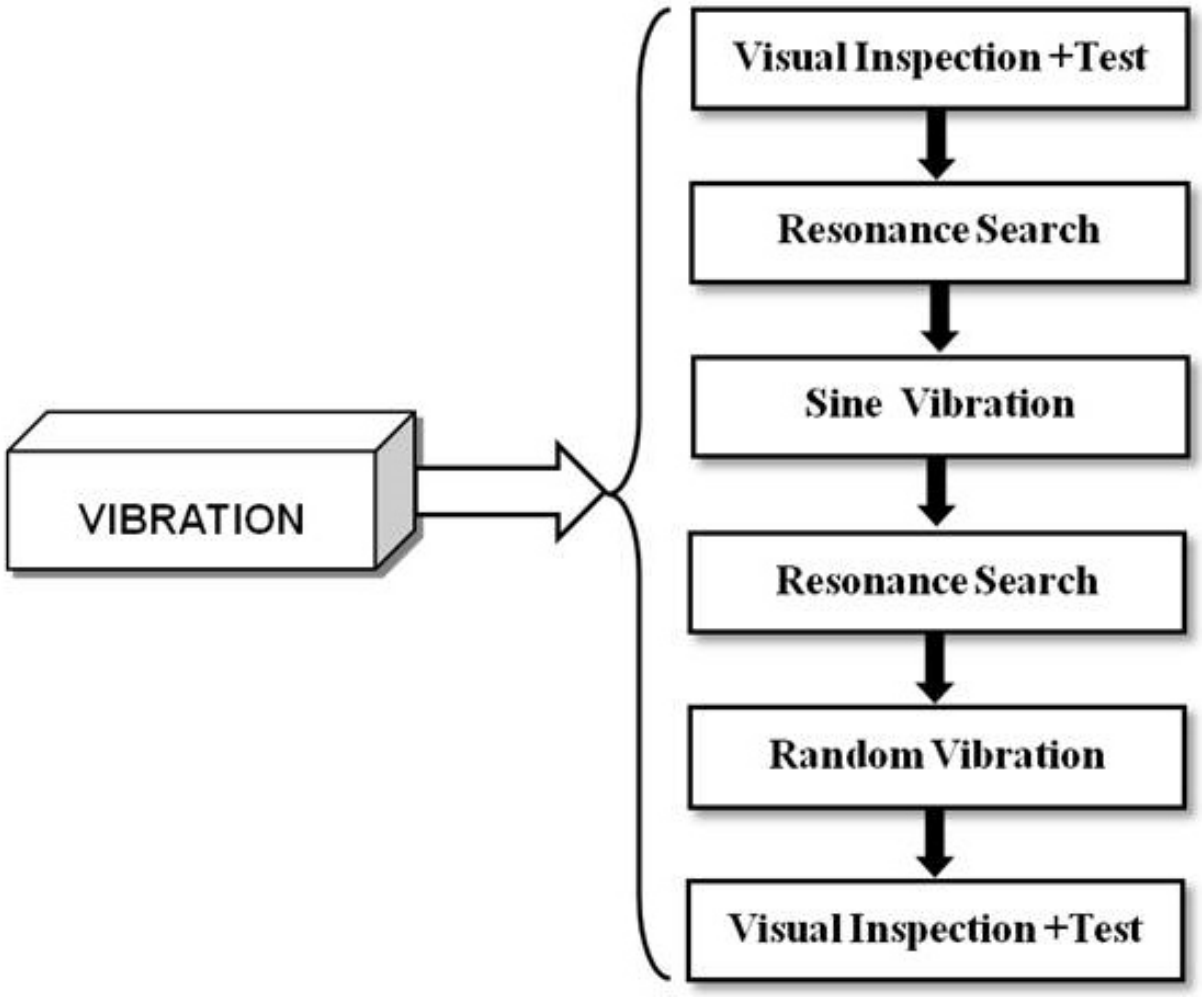


Figure 8.16: Vibration test sequence.

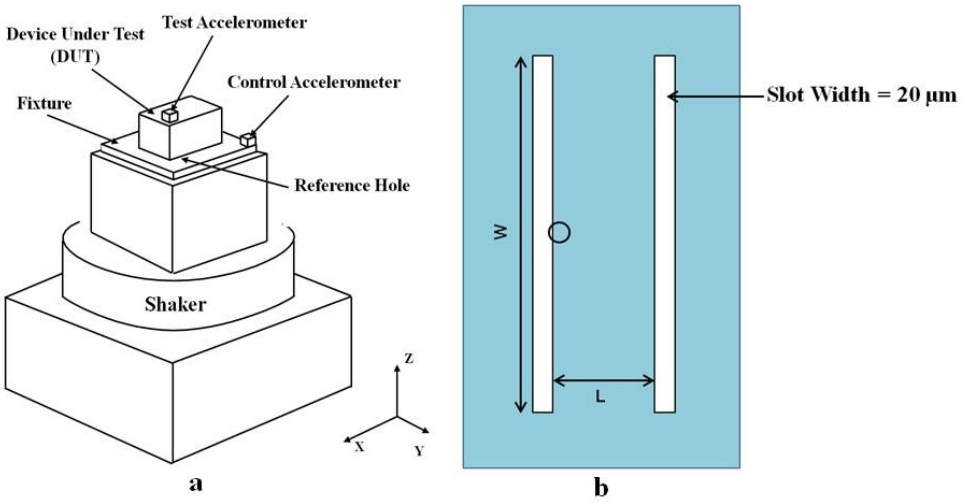


Figure 8.17: (a) Conceptual illustration of DUT on Shaker. (b) Ka2_Filter membrane (area b/w the two slots only) while the circle in the middle of the membrane shows the point at which measurement was performed.

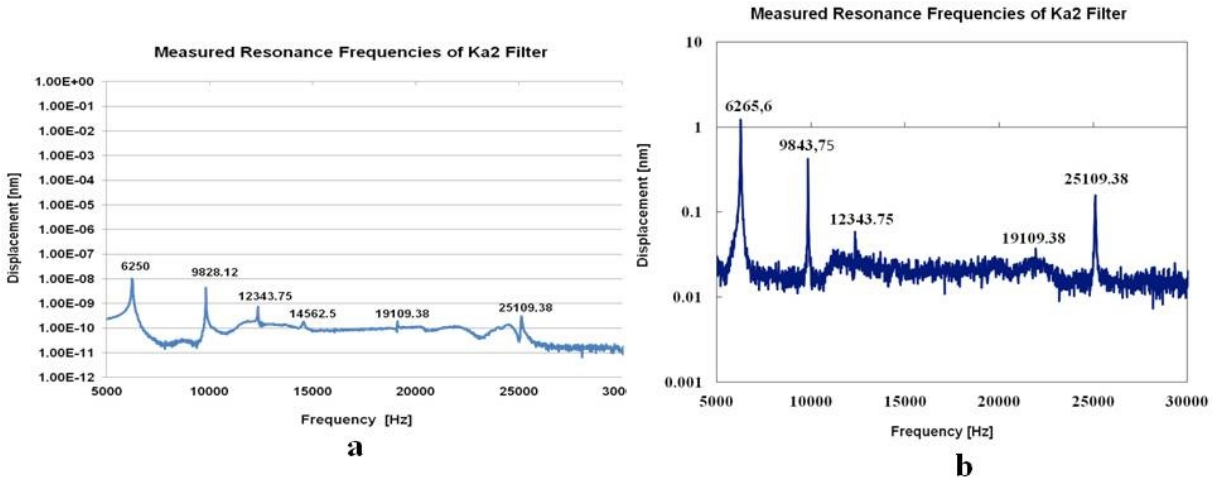


Figure 8.18: Resonance frequencies of the vibration test (a) Linear scale (b) logarithmic scale - 4^{th} Res_Freq is not apparent in log scale.

Fig. 8.17(a) shows the conceptual illustration of DUT on a shaker and Fig. 8.17(b) presents one of the membranes of the Ka band filter on which the test was performed. In the figure is also indicated the area where the laser was pointed and measurements were performed. The DUT was mounted

Table 8.1: Resonance freq of Ka_1 filter membranes with different thickness.

Mode Number	Measured Res_Freq	Tapered wall 16 μm	Tapered wall 17 μm	Straight wall 16 μm	Straight wall 17 μm
1	6250	4678.1	4941.1	4931.5	5208.7
2	9828.15	9323.1	9874.8	9494.7	10056
3	12343.75	12894	13619	13592	14356
4	19109.38	20425	21618	20937	22158
5	25109.38	25345	26766	26702	28199

on a fixture through its connector interface. A low level sine or low level random was applied separately in each axis and any significant resonant frequency (with amplification factor Q $>$ 3) was recorded, see Fig. 8.18 which graphically presents measured resonance frequencies.

In order to validate these findings a FEM model of Ka2 filter membrane simulated using ANSYS with the actual tapered walls. Simulations were performed on two types of membrane models: (a) Tapered side walls of membrane (with SiO_2 and Au gold layers), (b) Vertical side walls, refer to Fig. 8.19. Table 8.1. shows a comparison of measured resonance frequencies with simulated one are showing good agreement and graphically they are presented in Fig. 8.20.

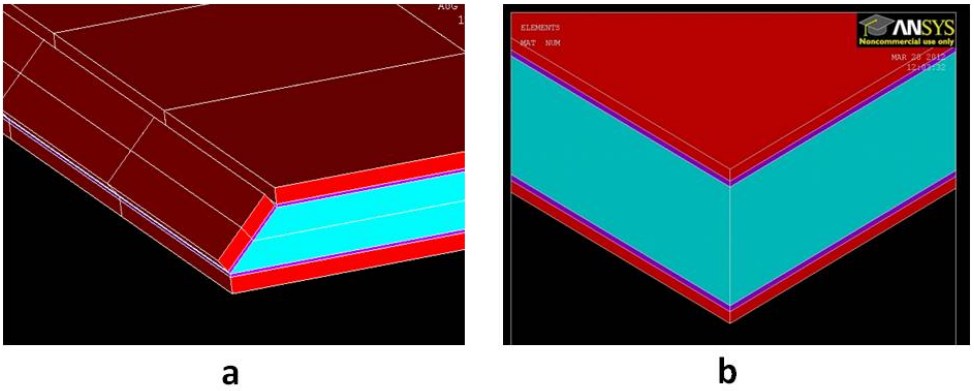


Figure 8.19: FEM model of Ka2 Filter (a) Tapered side walls covered, (b) Vertical side walls membrane.

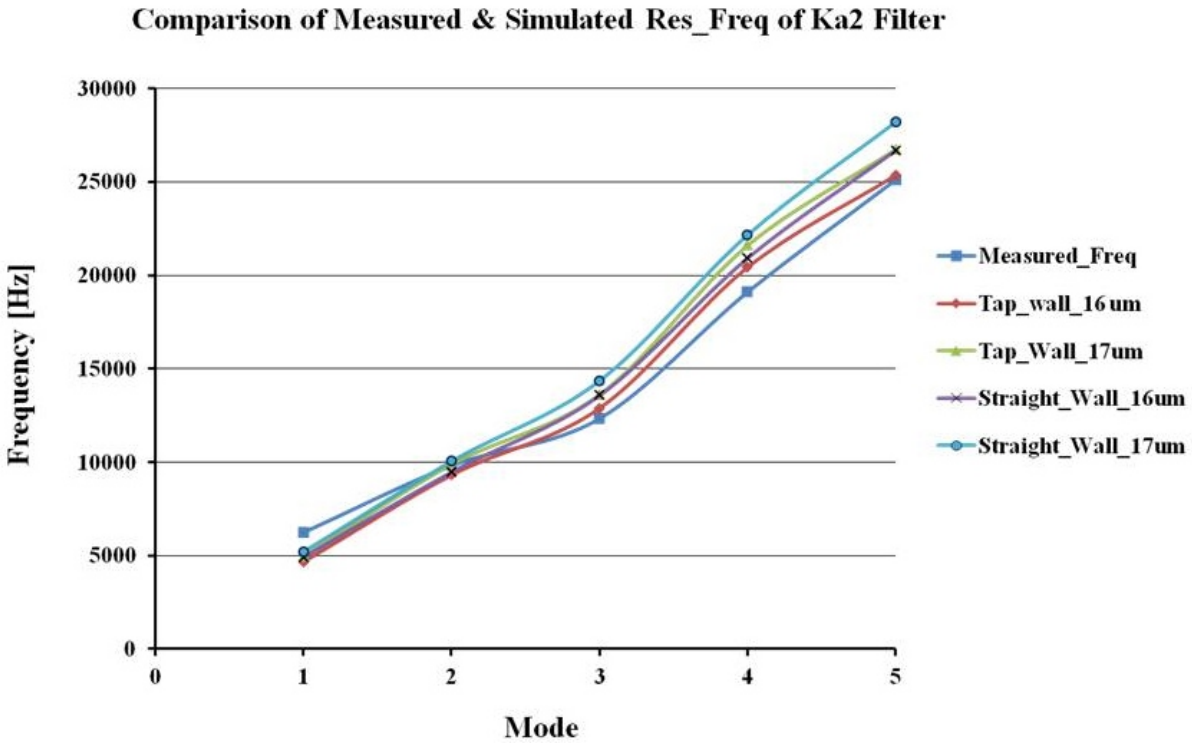


Figure 8.20: Comparison of measured and simulated resonance frequencies. Simulation was performed with various membrane thickness and also taking into account the actual tapered and ideally vertical walls of the membrane.

In conclusion these first measurements provided encouraging results. On one side the RF measurements showed that the EM design is basically sound and there is a good agreement between the design and the measurements on the realized prototypes. This also implies that the basic structure of the process is correct and provides usable structures. Moreover the small frequency offset found, even if not yet totally understood, indicates that the initial estimates of the process tolerances are correct and the process is accurate enough to allow the fabrication of the filters with high yield.

Finally also the mechanical project of the filter elements are robust enough for the intended application and the main elements that influence the mechanical stability are understood and controlled.

Chapter 9

Conclusions and Future Work

The research work summarized and presented in this thesis is a contribution to the broad field of RF MEMS devices which is seeing a growing interest and gaining importance due to the ubiquitous presence of RF applications in consumer electronics and telecommunication and the common trend towards applications at higher frequency. By and large Micro System Technology is a key sector for the technology innovation that sees a constantly growing commitment in Europe mainly to maintain the front edge positions in research and industry. Within this broad sector FBK has been involved already since years in the development of many different technology concepts regarding sensors, actuators and MEMS. In particular FBK has developed a proprietary technology platform for the realization of RF MEMS switches together with low loss RF components that allows the monolithic integration of complex RF circuits such as switching matrixes, phase shifters and tunable filters. In recent years filters for Radio Frequency and microwaves made with micromachining technologies have developed in a research field on its own and also FBK has been involved, as this is an opportunity to exploit the knowledge accumulated in time, on processing and designing RF devices in this new field.

This thesis is focused on the efforts to develop RF filters with micro-

machining technologies in two frequency bands, L/S and Ka, which is of great interest for on-board application in satellites but also for ground based stations. The main scope of this development is to enhance the filter performance by using the high precision achievable today with the micromachining techniques and to reduce overall size and weight of the devices which build with traditional mechanical techniques can be very bulky at the lower frequency spectrum.

The thesis gives a general overview of the field and the work performed by the development team of FBK and RFμTech, the two partners involved in the project funded by the ESA, and focuses on the processing and fabrication aspects of the devices, which is one of the critical aspects of the whole development work.

In the first part of the research work considerable time has been spent to define with the RF designers a concept for both filter types that on one side allows to achieve the demanding specifications of ESA and on the other side could be manufactured in an easy and cost effective way. At the beginning it was decided to rely for the Ka band filter on a design based on cavity filters and a specific process sequence was defined for this approach. In addition the fabrication tolerances were carefully assessed considering previous data and provided to the designers for a Monte Carlo analysis which gave a very poor yield estimate. So the filter design was modified and a TEM mode resonator was adopted while the technology concept was nearly the same. For the design of the L/S band filters a similar approach was adopted. Both technology concepts have common process aspects and both required the development and optimization of two basic process modules that were at the time not part of the capabilities of FBK. These are the wafer to wafer thermocompression bonding of two metal layers and conductive through silicon vias. For the thermocompression bonding, using for simplicity a flip chip bonder, the gold-gold system and silver-silver was investigated in a series

of experiments by varying load, temperature and time in order to find the optimum conditions for the higher bonding strength.

The research work on TSV's had the scope to reduce the area occupation of the TSV's based on simple bulk micromachining, especially important for the L/S band filters. It was possible to find a reliable method to fabricate through wafer holes with tapered sidewalls with angles that can be freely chosen in a wide range. Moreover, the metallization of these holes has also been studied. Different experiments were conducted with gold plating and copper plating which produced a partial success but also put into evidence the need of specific equipment for a successful implementation.

In parallel to these activities a number of process runs for the realization of prototype test structures for both filter types were performed. This work allowed the optimization of the process sequence and the correction for some errors in the initial fabrication concept and the fabrication of enough material to allow the full assembly of the test structures that could be characterized. The EM characterization showed that the fabrication process can reach the required precision, while vibration and thermal tests showed that the structures are suitable for on board applications. These tests have been accompanied with mechanical modeling activity that showed a good agreement with the measurement performed.

More specifically the major findings of this work on cavity filters with micromachining technologies can be summarized as follows:

- For both filter types viable process schedules have been developed and debugged.
- TSV's can be produced by bulk micromachining.
- Cavity etching and membrane formation can be done with anisotropic etching with the exception where structures have convex corners. In this case standard techniques for corner compensation are not so effective

and this will be even more worse for deep cavities.

- Thermocompression bonding of gold to gold gives reliable bonds. Thermocompression bonding of silver to silver has even higher bond strengths.
- Silver metallization is well accepted by the RF community and even more cost effective than gold coating.
- Vibrations will probably not be of much concern for these types of structures.
- Tapered TSV's can reduce the area occupation but due to the large size of these structures the resulting reduction in foot print is marginal.
- The tapered DRIE etch could effectively be used instead of the anisotropic etch to fabricate the cavities with convex corners.

The work performed in this PhD thesis allows also to make an outlook on the future activity in this field. Regarding the construction of the filter elements the future work should relay on the DRIE etching instead of the silicon bulk micromachining due to the problems with the corner compensation structures and also because of the area savings in the TWV fabrication. The thesis has also put into evidence that the use of silver for the metallization of the cavity is more convenient as it provides higher bonding strengths between the filter elements and is also more cost effective. The scope of the future work will also be to transfer the filter realization from die level to wafer level. To this purpose the operation conditions for the thermocompression bonding identified at die level by using a flip chip bonder will have to be transferred to the wafer to wafer bonding process in order to demonstrate the feasibility of the fabrication of micromachined filters at wafer level.

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Appendix A

Ka – A

Process for the top plate of the Ka band filters

Process Flow

1. Sealing Ring
2. Hard Mask Definition and Bulk Etch
3. Hard Mask Removal
4. Oxidation & Anneal
5. Slot definition and Ground Plating
6. 1st Seed Removal
7. Via
8. Micro Strip Definition and Plating
9. 2^{nd} Seed Removal

Starting material: HR 5 kΩcm, p-type Si, <100>, 200 μm, DSP

Step#	Type	Description
0.1	**Lithography (0)** **Mask #**	Define Wafer ID Use fibre pencil and Acetone. at wafer border!
0.2	Etch Rcp # POLY_2	Plasma Etch Wafer ID On wafer front side!
0.3	Ashing Rcp # Tepla NEW	Plasma Strip Resist -
1.1	**Lithography (1)** **Mask # SR**	Define Sealing Ring On the backside!
1.2	Etch Rcp # Poly_1	Plasma Etch Sealing Ring On wafer back side!
1.3	Ashing Rcp # Tepla	Plasma Strip Resist -
1.4	**Ashing**	Wet Resist Strip 5:1 H_2SO_4/H_2O_2 110°C 10 min
1.5	Diffusion Rcp # Thick_ox.	Grow Field Oxide (1000 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 385 Wet O_2
2.1	Diffusion Rcp # Nitride	LPCVD Nitride Deposition (150 nm) Deposition Temperature = 775°C
2.2	Diffusion Rcp # TEOS_uD	LPCVD Undoped TEOS Deposition (300 nm) Deposition Temperature = 718°C
2.3	**Lithography (2)** **Mask # VIA_DOWN**	Define Hard Mask On the backside!
2.4	Etch Rcp # High Sel	Etch Backside Oxide On the backside!
2.5	Ashing Rcp # Tepla	Plasma Strip Resist 20 min
2.6	Wet Etch	1^{st} Bulk-Si Etch (-175 μm) TMAH 4:1 90°C. Use holder!
2.7	Wet Etch	2^{nd} Bulk-Si Etch TMAH 4:1 90°C.
3.1	Wet Etch	Strip Backside TEOS Coat front side of wafers with resist, hard bake 7:1 buffered HF

3.2	Ashing Rcp # Tepla NEW	Plasma Strip Resist On wafer frontside!
3.3	Wet Etch	Wet Etch Nitride Surface oxide removal ? 7:1 buffered HF Strip nitride in HP_3O_4 - 180°C
3.4	Wet Etch	Strip Backside Oxide 7:1 buffered HF
4.1	Diffusion Rcp # Thick_ox.	Grow Field Oxide (1000 nm) ***Temp° C*** ***Time min*** ***Gas*** 975 10 N_2 975 385 Wet O_2
4.2	Diffusion Rcp # Thick_ox.	Anneal ***Temp° C*** ***Time min*** ***Gas*** 975 50 N_2
4.3	Wet Etch	Wet Etch Nitride Surface oxide removal ? 7:1 buffered HF Strip nitride in HP_3O_4 - 180°C
5.1	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2.5 nm) Deposition Temperature = RT Flash before deposition!
5.2	Deposition Rcp # ULVAC Au Fast	Deposition of Au (25 nm) On wafer backside! Deposition Temperature = RT
5.3	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2 nm) Deposition Temperature = RT
5.4	**Lithography (3)** **Mask # GND**	Define Slot On the bsackside! Dry film 15 μm thick Flash before coating!
5.5	Wet Etch	Etch Chrome 2 Wet the wafers before etch with DI water! 15 sec Cr etch
5.6	Deposition Rcp # rcp1	Gold Electro-deposition (2.5+ μm) Flash before deposition!
5.7	Ashing Rcp # Wash	Wet Strip Resist -
6.1	Wet Etch	Etch Chrome 2

		Wet the wafers before etch with DI water! 15 sec Cr etch
6.2	Wet Etch	Etch Au Seed layer Wet the wafers before etch with DI water! 25 sec Au etch
6.3	Wet Etch	Etch Chrome 1 Wet the wafers before etch with DI water! 15 sec Cr etch
6.4	Wet Etch	Chrome de-freckle 1 Wet the wafers before etch with DI water! 10 sec Au etch used
6.5	Wet Etch	Chrome de-freckle 2 Wet the wafers before etch with DI water! HF 2% 20 sec
7.1	**Lithography (4)** **Mask # VIA_UP**	Define Via's -
7.2	Wet Etch	Open Via's 1 7:1 buffered HF For ∼2/3th of the thickness
7.3	Etch Rcp # LS 40 sec	Open Via's 2 -
7.4	Ashing Rcp # STRIP2	Plasma Strip Resist 20 min
8.1	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2.5 nm) Deposition Temperature = RT Flash before deposition!
8.2	Deposition Rcp # ULVAC Au Fast	Deposition of Au (25 nm) Deposition Temperature = RT
8.3	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2 nm) Deposition Temperature = RT
8.4	**Lithography (5)** **Mask # MS**	Define Micro Strip AZ positive resist 4 μm thick Flash before coating!
8.5	Wet Etch	Etch Chrome 2 Wet the wafers before etch with DI water! 15 sec Cr etch
8.6	Deposition	Gold Electro-deposition (2.5+ μm)

	Rcp # rcp1	Flash before deposition!
8.7	Ashing Rcp # Wash	Wet Strip Resist -
9.1	Wet Etch	Etch Chrome 2 Spry coat the back side of the wafer Wet the wafers before etch with DI water! 15 sec Cr etch
9.2	Wet Etch	Etch Au Seed layer Wet the wafers before etch with DI water! 25 sec Au etch
9.3	Wet Etch	Etch Chrome 1 Wet the wafers before etch with DI water! 15 sec Cr etch
9.4	Wet Etch	Chrome de-freckle 1 Wet the wafers before etch with DI water! 10 sec Au etch used
9.5	Wet Etch	Chrome de-freckle 2 Wet the wafers before etch with DI water! HF 2% 20 sec
9.6	Ashing Rcp # Wash	Wet Strip Resist -
9.7	Diffusion Rcp # Prog 6 Au	Gold Sintering $\boldsymbol{Temp^{\circ}C}$ $\boldsymbol{Time\ min}$ $\boldsymbol{Gas}$ 190 30 N_2

Appendix B

Ka – B

Process for the middle plate of the Ka band filters

Process Flow

1. Lattice Alignment
2. Sealing Ring Formation
3. Diaphragm Definition
4. Cavity Formation
5. Hard Mask Removal & Reox
6. Plating

Starting material: HR 5 kΩcm, p-type Si, <100>, 500 μm, DSP

Step#	**Type**	**Description**
0.1	Diffusion Rcp # Thick_ox.	Grow Mask Oxide (120 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 22 Wet O_2
0.2	**Lithography (0)** **Mask # MASK-0 MF5**	Define Lattice Alignment Marks -
0.3	Etch Rcp # POLY_1	Plasma Etch Alignment Marks On wafer front side!
0.4	Ashing Rcp # Tepla	Plasma Strip Resist -
0.5	Ashing	Wet Resist Strip 5:1 H_2SO_4/H_2O_2 110°C 10 min
0.6	Wet Etch	Bulk-Si Etch (-20 μm) TMAH 4:1 90°C.
1.1	**Lithography (1)** **Mask # SR**	Define Sealing Ring On the backside!
1.2	**Etch** Rcp # POLY_1	Plasma Etch Sealing Ring (-1 μm) On wafer front side!
1.3	Ashing Rcp # Tepla	Plasma Strip Resist -
1.4	Ashing	Wet Resist Strip 5:1 H_2SO_4/H_2O_2 110°C 10 min
2.1	Diffusion Rcp # Thick_ox.	Grow Thick Oxide (120 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 22 Wet O_2
2.2	**Lithography (2)** **Mask # CAV_UP**	Define Diaphragm -
2.3	Etch Rcp # High Sel	Etch Backside Oxide -
2.4	Ashing Rcp # Tepla	Plasma Strip Resist 20 min
2.5	Wet Etch	1^{st} Bulk-Si Etch (-20 μm) TMAH 4:1 90°C.
3.1	Diffusion	Grow Oxide (300 nm)

	Rcp # Thick_ox.	***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 60 Wet O_2
3.2	Diffusion Rcp # Nitride	LPCVD Nitride Deposition (150 nm) Deposition Temperature = 775°C
3.3	Diffusion Rcp # TEOS_uD	LPCVD Undoped TEOS Deposition (300 nm) Deposition Temperature = 718°C
3.4	**Lithography (3)** **Mask # CAV_DOWN**	Define Hard Mask On the backside!
3.5	**Etch** Rcp # High Sel	Etch Hard Mask On the backside!
3.6	Ashing Rcp # Tepla	Plasma Strip Resist 20 min
3.7	Wet Etch	1^{st} Bulk-Si Etch (-455 μm) TMAH 4:1 90°C. Use holder!
3.8	Wet Etch	2^{nd} Bulk-Si Etch (Final trimming) TMAH 4:1 90°C. Use holder!
4.1	Wet Etch	Strip Top Oxide 7:1 buffered HF
4.2	Wet Etch	Wet Etch Nitride Surface oxide removal ? 7:1 buffered HF Strip nitride in HP_3O_4 - 180°C
4.3	Wet Etch	Strip Base Oxide 7:1 buffered HF
4.4	Diffusion Rcp # Thick_ox.	Grow Field Oxide (1000 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 385 Wet O_2
4.5	Diffusion Rcp # POLY_drv	Anneal ***Temp°C*** ***Time min*** ***Gas*** 975 50 N_2
5.1	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2.5 nm) Front Deposition Temperature = RT Flash before deposition!
5.2	Deposition Rcp # ULVAC Au Fast	Deposition of Au (25 nm) Front Deposition Temperature = RT
5.3	Deposition	Deposition of Cr (2.5 nm) Back

	Rcp # ULVAC Cr thin	Deposition Temperature = RT
5.4	Deposition Rcp # ULVAC Au Fast	Deposition of Au (25 nm) Back Deposition Temperature = RT
5.5	Deposition Rcp # rcp1	Gold Electro-dep. (2.5+ μm) Front Spray coat backside with AZ positive resist 4 μm thick!
5.6	Ashing Rcp # Wash	Wet Strip Resist On the backside!
5.7	Deposition Rcp # rcp1	Gold Electro-dep. (2.5+ μm) Back Spray coat backside with AZ positive resist 4 μm thick!
5.8	Ashing Rcp # Wash	Wet Strip Resist On the frontside!
5.9	Diffusion Rcp # Prog 6 Au	Gold Sintering ***Temp°C*** ***Time min*** ***Gas*** 190 30 N_2

Appendix C

LS

Process for the cavity sections of the LS band filters

Process Flow

1. Lattice Alignment
2. Sealing Ring
3. Hard Mask Definition and Bulk Etch
4. Hard Mask Removal
5. Oxidation & Anneal
6. Define Conductors
7. 1st Seed Removal
8. Via & Hard Mask
9. Ground

Starting material: HR 5 kΩcm, p-type Si, <100>, 500 μm, DSP

Step#	Type	Description
0.1	Diffusion Rcp # Thick_ox.	Grow Mask Oxide (120 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 22 Wet O_2
0.2	**Lithography (0)** **Mask # MASK-0 MF5**	Define Lattice Alignment Marks -
0.3	Etch Rcp # POLY_1	Plasma Etch Alignment Marks On wafer front side!
0.4	Ashing Rcp # Tepla	Plasma Strip Resist -
0.5	Ashing	Wet Resist Strip 5:1 H_2SO_4/H_2O_2 110°C 10 min
0.6	Wet Etch	Bulk-Si Etch (-20 μm) TMAH 4:1 90°C.
1.1	**Lithography (1)** **Mask # SR**	Define Sealing Ring On the backside!
1.2	Etch Rcp # High Sel	Etch Backside Oxide On the backside!
1.3	Etch Rcp # POLY_1	Plasma Etch Sealing Ring On wafer backside!
1.4	Ashing Rcp # Tepla	Plasma Strip Resist -
1.5	Ashing	Wet Resist Strip 5:1 H_2SO_4/H_2O_2 110°C 10 min
1.6	Wet Etch	Strip Oxide 7:1 buffered HF
1.7	Diffusion Rcp # Thick_ox.	Grow Field Oxide (1000 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 385 Wet O_2
2.1	Diffusion Rcp # Nitride	LPCVD Nitride Deposition (150 nm) Deposition Temperature = 775°C
2.2	Diffusion Rcp # TEOS_uD	LPCVD Undoped TEOS Deposition (300 nm) Deposition Temperature = 718°C
2.3	**Lithography (2)** **Mask # LS_VIA_UP**	Define Hard Mask -

2.4	Etch Rcp # High Sel	Etch frontside oxide -
2.5	Ashing Rcp # Tepla	Plasma Strip Resist 20 min
2.6	Wet Etch	1^{st} Bulk-Si Etch (-475 μm) TMAH 4:1 90°C. Use holder!
2.7	Wet Etch	2^{nd} Bulk-Si Etch TMAH 4:1 90°C.
3.1	Wet Etch	Strip Frontside TEOS Coat back side of wafers with resist, hard bake 7:1 buffered HF
3.2	Ashing Rcp # Tepla NEW	Plasma Strip Resist On wafer back side!
3.3	Wet Etch	Wet Etch Nitride Surface oxide removal ? 7:1 buffered HF Strip nitride in HP_3O_4 - 180°C
3.4	Wet Etch	Strip Frontside Oxide 7:1 buffered HF
4.1	Diffusion Rcp # Thick_ox.	Grow Field Oxide (1000 nm) ***Temp°C*** ***Time min*** ***Gas*** 975 10 N_2 975 385 Wet O_2
4.2	Diffusion Rcp # POLY_drv	Anneal ***Temp°C*** ***Time min*** ***Gas*** 975 50 N_2
5.1	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2.5 nm) Front Deposition Temperature = RT Flash before deposition!
5.2	Deposition Rcp # ULVAC Au Fast	Deposition of Au (25 nm) Front Deposition Temperature = RT
5.3	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2 nm) Back Deposition Temperature = RT
5.4	**Lithography (3)** **Mask # CAV_COND_UP**	Define Conductors Dry film 15 μm thick Flash before coating!
5.5	Wet Etch	Etch Chrome 2 Wet the wafers before etch with DI water!

		15 sec Cr etch
5.6	Deposition Rcp # rcp1	Gold Electro-deposition (5+ μm) Flash before deposition!
5.7	Ashing Rcp # Wash	Wet Strip Resist -
6.1	Wet Etch	Etch Chrome 2 Wet the wafers before etch with DI water! 15 sec Cr etch
6.2	Wet Etch	Etch Au Seed layer Wet the wafers before etch with DI water! 25 sec Au etch
6.3	Wet Etch	Etch Chrome 1 Wet the wafers before etch with DI water! 15 sec Cr etch
6.4	Wet Etch	Chrome de-freckle 1 Wet the wafers before etch with DI water! 10 sec Au etch used
6.5	Wet Etch	Chrome de-freckle 2 Wet the wafers before etch with DI water! HF 2% 20 sec
7.1	**Lithography (4)** **Mask # LS_VIA_DCAV**	Define Via's & Hard Mask On the wafer backside!
7.2	Etch Rcp # LS 40 sec	Open Via's & Hard Mask On the wafer backside!
7.3	Ashing Rcp # STRIP2	Wet Strip Resist On the wafer backside! 20 min
8.1	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2.5 nm) Deposition Temperature = RT Flash before deposition!
8.2	Deposition Rcp # ULVAC Au Fast	Deposition of Au (25 nm) Deposition Temperature = RT
8.3	Deposition Rcp # ULVAC Cr thin	Deposition of Cr (2 nm) Deposition Temperature = RT
8.4	**Lithography (5)** **Mask # LS_COND_D**	Define Ground On the wafer backside! AZ positive resist 4 μm thick

		Flash before coating!
8.5	Wet Etch	Etch Chrome 2 Wet the wafers before etch with DI water! 15 sec Cr etch
8.6	Deposition Rcp # rcp1	Gold Electro-deposition (5+ μm) Flash before deposition!
8.7	Ashing Rcp # Wash	Wet Strip Resist -
9.1	Wet Etch	Etch Chrome 2 Spry coat the back side of the wafer Wet the wafers before etch with DI water! 15 sec Cr etch
9.2	Wet Etch	Etch Au Seed layer Wet the wafers before etch with DI water! 25 sec Au etch
9.3	Wet Etch	Etch Chrome 1 Wet the wafers before etch with DI water! 15 sec Cr etch
9.4	Wet Etch	Chrome de-freckle 1 Wet the wafers before etch with DI water! 10 sec Au etch used
9.5	Wet Etch	Chrome de-freckle 2 Wet the wafers before etch with DI water! HF 2% 20 sec
9.6	Ashing Rcp # Wash	Wet Strip Resist -
10.1	Wet Etch	Dip in HF 2% 50:1 HF
10.2	Wet Etch	1^{st} Bulk-Si Etch (-455 μm) On the wafer backside! TMAH 4:1 90°C. Use holder!
10.3	Wet Etch	2^{nd} Bulk-Si Etch Membrane trimming TMAH 4:1 90°C.
10.4	Diffusion Rcp # Prog 6 Au	Gold Sintering ***Temp° C*** ***Time min*** ***Gas*** 190 30 N_2

Appendix D

Operating parameters of Cu plating solutions

	InterVia™ Cu 8540	**Cuprum 33**
Temperature	20-27°C 23°C recommended	22-33°C 27°C recommended
Cathode current density	2-4 A/dm^2 2.5A/dm^2 recommended	2-6 A/dm^2 4A/dm^2 recommended
Agitation	Critical factor to obtain excellent filling performance, good throwing power, low stress deposits with good elongation	
Anode	Phosphorus content Copper anode (0.02%...0.06%) or TiPt	Phosphorus content Copper anode (0.02%...0.06%)
Deposition rate (μm/min)	TBD	1.0 μ/min. at 4 A/dm^2
Bath maintenance	InterVia Cu 8540A: 2.5-20 ml/l, recomended: 5 ml/l, consumption: 0.5-2ml per 1Ah. InterVia Cu 8540C 2.5-20 ml/l, recommended:5 ml/l, consumption: 0.05-0.2ml per 1Ah.	For 400Ah: 80ml Cuprum 33 Additive 35ml Cuprum 33 Leveling 80ml Cuprum 33 Brightener

Index of Terms

BPF Bandpass Filter.

EM Electromagnetic.

ESA European Space Agency.

IC Integrated Circuit.

ICT Information and Communication Technology.

LTCC Low Temperature Cofired Ceramics.

MEMS Micro-Electro-Mechanical-System.

PR Photoresist.

PVD Physical Vapor Deposition.

RF Radio Frequency.

RIE Reactive Ion Etching.

Si_3N_4 Silicon Nitride.

SiO_2 Silicon Dioxide.

SIW Surface Integrated Waveguide.

TMAH Tetra-Methyl-Ammonium-Hydroxide.

TSV Through Silicon Via.

TWV Through Wafer Via.

UNIPG University of Perugia.