UNIVERSITY OF TRENTO

Department of Physics

PhD Thesis

Erbium and Silicon Nanocrystals based Light Emitting Devices for lightwave circuits

Supervisor

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Candidate

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XXVI Cycle

(Defended November 11, 2013)

A Chi mi guarda da Lassù,

A mamma e papà,

A Anna, Luca e ...

Agisci in modo da trattare l'umanità,
sia nella tua persona
che nella persona di ogni altro,
sempre anche come un fine
e mai soltanto come un mezzo.
[Immanuel Kant]

C'è una forza motrice più forte del vapore,
dell'elettricità e dell'energia atomica:
la volontà.
[Albert Einstein]

Fate il bene senza comparire.
La violetta sta nascosta ma si conosce
e si trova grazie al suo profumo.
[San Giovanni Bosco]

List of publications

Portions of this thesis have been drawn from the following publications:

- **International Journals**

D. Di, I. Perez-Wurfl, L. Wu, Y. Huang, A. Marconi, **A. Tengattini**, A. Anopchenko, L. Pavesi, G. Conibeer, "Electroluminescence from Si nanocrystal/c-Si heterojunction light-emitting diodes," Applied Physics Letters, Vol. 99, Issue 25, 251113 (2011).

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- **National Journals**

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- **Conference Proceedings**

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Chapter 1

Introduction

"Silicon is likely to remain the basic material. Silicon will predominate, because of the technology which has already evolved around it and because it is an abundant and relatively inexpensive starting material. […] The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65.000. I believe that such a large circuit can be built on a single wafer" [Gordon E. Moore - 1965]

1.1 The Silicon Technology

To say that we live in a world based on photonics nowadays would be an understatement. In fact, photonics is present in all the aspects of our everyday life. The modern life, based on electronics and telecommunications more than the past years, has been possible by the presence of innumerable products that rely on integrated electronic circuits based on silicon wafers. A good example is the growth of the Internet communication, with the number of users continuing to double every few months. Microelectronics and photonics have tremendous implications for industry, employment, strategic position of the country, and even for the future organization of the society. It is natural that everyone wonders which new applications of microelectronics and photonics

are most likely to come into the everyday life in the near future and which differences these applications might make for the 21st century. Gordon Moore was the precursor of the silicon technology as we can see in his paper published in 1965 [1]. This is the reason why I have chosen one of his sentences to introduce my thesis. The complexity is usually equated to the transistor count, and by that measure the exponential progress predicted by the Moore's law has been maintained through the present day. Figure 1.1 shows the original plot of the Moore's paper, which represents the number of components per integrated function as a function of the years, between the 1959 and the 1975. I have decided to put this original plot, in order to give an historical hint to my thesis. Figure 1.2 shows instead the actualization of the Moore's law, up to the beginning of the new century. The number of transistors per chip has exponentially increased as a function of the year. The key point is that it has become cheaper over time to pack more and more transistors into integrated circuits because each individual transistor is always being made smaller. This continuous scaling process allows more powerful chips with more transistors to be made for a reasonable price. The scaling process is the engine of progress in silicon microelectronics. It is sustained only by a continue research and development in the silicon technology itself. Goals and benchmarks for scaling are established and monitored in the International Technology Roadmap for Semiconductors (ITRS), a public document drawn up every year by a consortium representing the global semiconductor industry [2].

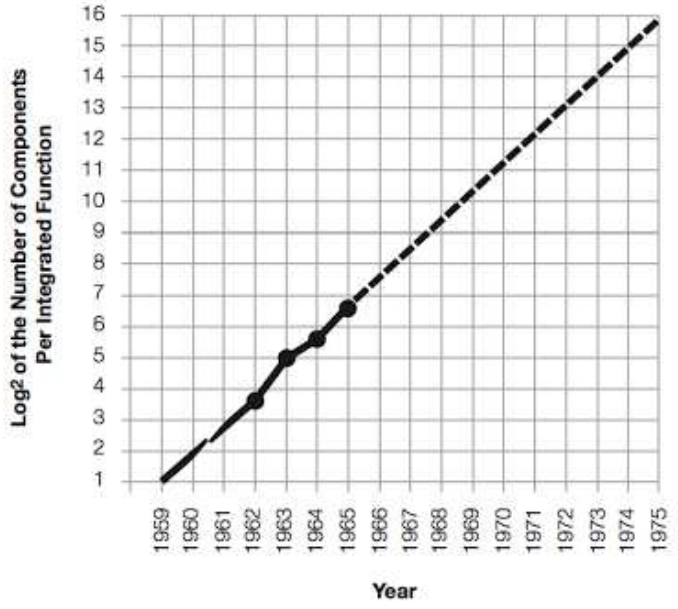


Figure 1.1. Number of components per integrated function as a function of the year. (After Gordon Moore [1]).

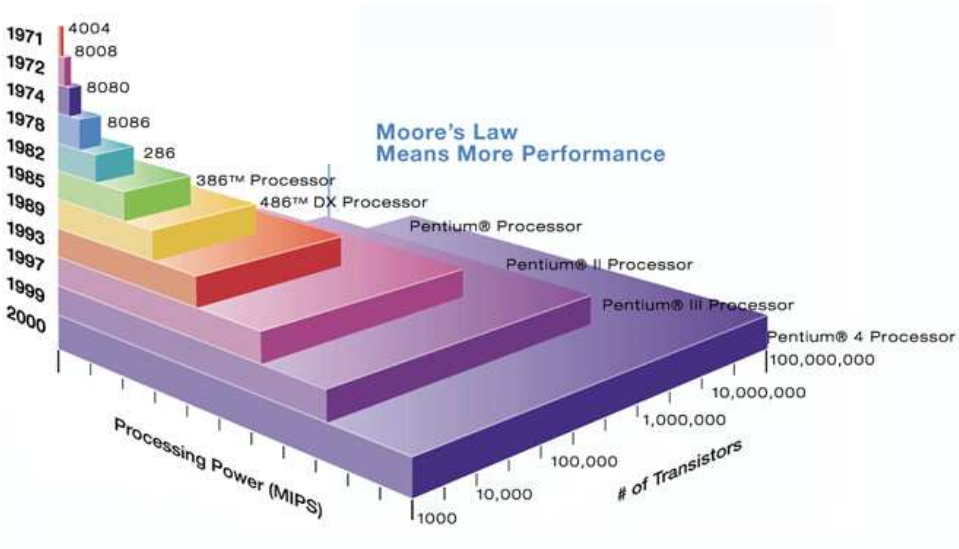


Figure 1.2. Transistor counts for integrated circuits showing the historical accuracy of Gordon Moore's prediction of exponentially increasing integrated circuit complexity.

The roadmap is intended "to provide a reference of requirements, potential solutions, and their timing for the semiconductor industry" over a fifteen-year horizon. For many years in the past, the ITRS has highlighted one threat to continue scaling in particular that must be addressed in the short term future in order to avoid slowing down the pace of the Moore's law.

1.2 Optical Interconnects

Photonics will be the answer to provide the long term solution for many open problems. In the so-called optical interconnect schemes, the copper wires between regions of an integrated circuit would be replaced by a system of lasers, modulators, optical waveguides and photo-detectors. In his paper, Miller gives a brief historical summary of the development of the field of optical interconnects to silicon integrated circuits [3]. The potential benefits of the silicon technology in the optical communication scenario include the virtual elimination of delay, cross talk, and power dissipation in signal propagation, although significant new challenges will be introduced in signal generation and detection [4]. Stable laser sources, interferometric modulators, dense wavelength division multiplexing (DWDM), and low loss planar waveguides will all be necessary components of an optical interconnect [5]. These photonic technologies are now applied primarily in the long-haul telecommunications industry, where individual component cost and size do not drive the market. Data transfer rates and the cost per transmitted bit through optical

fiber networks have improved dramatically in performance over the last few decades [6], following the exponential progress curves that can compound even faster than Moore's law. Microphotonics refers to efforts to miniaturize the optical components used in long distance telecommunications networks so that integrated photonic circuits can become a reality [7]. Work in this field spans many subjects, including planar waveguides and photonic crystals, integrated diode detectors, modulators, and lasers. Advances in the related and often overlapping field of nanophotonics suggest the possibility of eventually controlling optical properties through nanoscale engineering [8]. Some progresses have also been made in efficient silicon photonic device development. On the transmit side, carrier-depletion microdisk [9] and microring [10] modulators have demonstrated an energy efficiency of a few 10s fJ/bit at 10 Gb/s. Optimized racetrack ring modulators with reduced voltage swing can further improve efficiency to about 10 fJ/bit [11]. This fact is very important, because these devices became compatible with voltage supply levels associated with the switch power of the transistors. On the detection side, very low parasitic Ge photodetectors have reported high responsivity and bandwidth [12].

1.3 The Silicon Photonics

The goal of silicon photonics is to create high performance optical devices from the set of the Complementary Metal Oxide Semiconductor (CMOS) compatible materials used in electronic integrated circuits so that the photonic components can be made using the already existing silicon fabrication technology. Nowadays, in fact, the CMOS circuits have tremendous power efficiency advantages and are the basic building blocks for all the microprocessors. It is important to ensure that all materials used in a CMOS facility do not contaminate these fundamental components of the circuit. One key word of the silicon photonics itself is the CMOS compatibility. Of course, silicon is a CMOS compatible material. Many of the properties that make silicon a good choice for electronic chips are helpful in optical applications as well. It is an abundant material, with good thermal conductivity and good mechanical strength. It also has a high index of refraction and a small intrinsic absorption at infrared photon wavelengths. Silicon-based device solutions have been already demonstrated for planar waveguides and for high-speed detectors. On the other side, silicon is a poor material for making modulators or lasers, which together comprise the necessary signal transmission source in optical communication. The two main problems, which are limiting the use of silicon in the photonics scenario, are its

centrosymmetric lattice and its indirect band structure. Now, I will briefly describe the first problem, while I will enter more in the detail of the second one, object of my thesis work and study. The silicon crystal, in fact, is centrosymmetric (i.e. it has inversion symmetry, so the points at (x, y, z) are indistinguishable from those at (-x, -y, -z)), which means it lacks the 2th order non linear susceptibility $\chi^{(2)}$, which is the responsible for the linear change in refractive index with an applied electric field. Last years, here in Trento, both second-harmonic-generation experiments and first-principle calculations produced values of strain-induced bulk second-order nonlinear susceptibility, up to 40 pmV^{-1} at 2300 nm. So, the nonlinear strained silicon could provide a competing platform for a new class of integrated light sources spanning the near- to mid-infrared spectrum from 1.2 to 10 µm [13]. Moreover, on the other side, silicon has an indirect band structure, as shown in Figure 1.3. This means that the top of the valence band and the bottom of the conduction band are not aligned in the momentum space. In order to absorb or emit a photon at the visible wavelengths, an electron must undergo a band-to-band transition between two of these states. This transition requires the simultaneous absorption or emission of a phonon to accommodate the momentum mismatch, making it much less likely to occur than in a direct semiconductor.

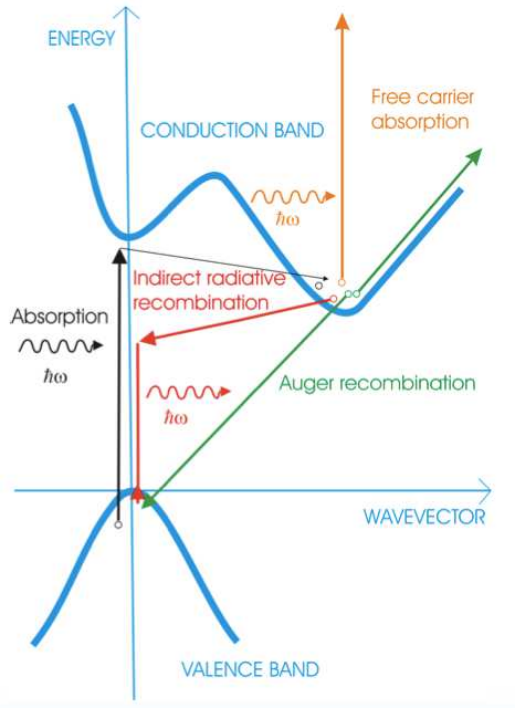


Figure 1.3. Energy band structure of silicon (indirect band gap material). The value of the energy gap is 1.12 eV, but there is a momentum offset between the lowest energy states in the conduction band and the highest energy valence band states. A sketch of the possible ways for radiative and non-radiative recombinations in silicon is shown by the arrows [14].

In silicon, the radiative recombination has an average lifetime (τ_{rad} ~ ms) bigger than that of other non radiative processes ($\tau_{non\text{-}rad}$ ~ ns) for which the internal quantum efficiency, which is the ratio between the probability that a radiative recombination occurs and the probability that a recombination occurs in general, takes value in the order of $10^{-6} \div 10^{-7}$. So, up to now, silicon cannot be used for light generation and for light amplification, but, due to the great and huge interest of the scientific community in this material, several strategies have been adopted with the aim to increase its radiative emission and its power efficiency. The recently reported first silicon laser [15] did not rely on the emission of photons by excited conduction band electrons. This laser instead operated by Raman scattering in which sub-bandgap photons interact only with phonons. The crystalline structure of silicon makes Raman scattering relatively strong in relation to amorphous glasses, but intense optical pumping is still required to create a population inversion of the excited virtual phonon state. While these results are impressive, it is clear that Raman lasers do not have a practical future because they require optical excitation by a pump laser and have a relatively small spectral range in which gain can be achieved. So, the major drawback of the silicon Raman laser is the need of an external optical pumping [16]. Materials which have superior optical properties, such as compounds of Group III and V elements, are used to make the lasers used in long-haul telecommunication networks. These materials are not CMOS compatible, primarily because of mismatched crystal lattice constants with respect to silicon. However, the list of materials that are CMOS compatible is always expanding as new methods of integration are introduced. This heterogeneous approach is currently being pursued by start-up photonics companies such as Luxtera, as well as Intel's silicon photonics research group. Both companies have recently demonstrated electrically pumped lasers on silicon substrates that use integrated III–V materials to achieve gain [17] [18].

Lastly, there is another possibility to use silicon as light emitting material, without the bonding of the silicon substrate wafer and the III-V materials group. This approach has the role to exploit the quantum mechanical effects of silicon, in order to improve the optical properties of the silicon itself or of other currently CMOS compatible materials. Following this approach, silicon quantum dots, also called silicon nanocrystals or silicon nanoclusters (Si-NCs in the following of my thesis), have been identified for many years as promising candidate material for the silicon photonics.

In all my thesis activities, I have worked on electrically pumped silicon nanocrystals based devices.

1.4 The Silicon Nanocrystals

Optical emission in silicon nanocrystals was shown already 25 years ago with the first report of photoluminescence from porous silicon [19] [20]. Porous silicon is formed by the electrochemical dissolution of a silicon wafer (the anode) in a solution containing HF [21]. When F^- and a hole injected from the wafer are both present at the interface, the silicon dissolution takes place. Porous silicon is obtained by decreasing the current density or increasing the HF concentration, so that the holes are the limiting species at the interface. The sizes of the pores and the silicon remnants can be tuned from the nanometer regime to beyond 1 µm. Light emission is especially strong in "spongy" porous silicon, which contains typical feature sizes in the nanometer range. Figure 1.4 shows an example of photoluminescence of Si-NCs, realized here in Trento, in a PMMA solution. The responsible for the enhanced photonic properties of the silicon itself is the quantum mechanical effects.

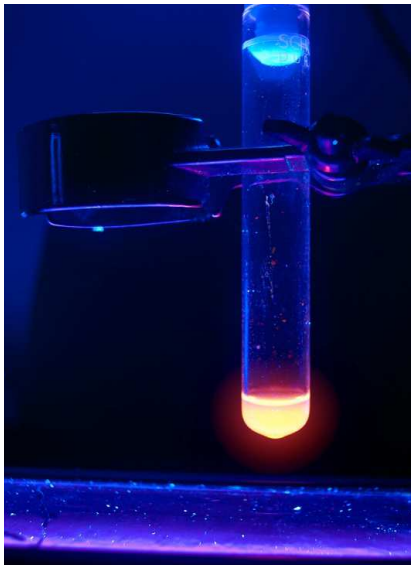


Figure 1.4. Photoluminescence of Si-NCs in a PMMA solution. We can notice the typical red emission of the silicon nanocrystals.

Qualitatively, the effect of quantum confinement in silicon nanocrystals can be understood by considering the simple particle in a box problem. In order to satisfy the boundary conditions, we find that the characteristic ground state energy scales inversely with the square of the width of the confining potential well. Confinement raises the energy of the ground state, tends to create a discrete density of states at low energies, and introduces uncertainty into the momentum of the particle. Figure 1.5 shows the density of states for systems of three, two, one and zero dimensions. One can notice the discrete

density of states in the case of silicon quantum dots. We can improve our approximation of a quantum dot by considering the particles of interest, excitons, in a three-dimensional spherical confinement potential representing the insulating matrix around the semiconductor nanocrystal. Excitons are electron-hole composite states that are coupled together by Coulomb attraction. The mathematics used to describe an exciton is identical to the model that we use to study the hydrogen atom. In terms of the electron and the hole that comprise the exciton, the Bohr radius can be thought of as the typical separation distance. In silicon, the exciton Bohr radius is about 5 nm. This tells us that we can expect to observe quantum confinement effects in silicon nanocrystals that are smaller than approximately 5 nm in diameter. In the devices characterized and examined in my thesis work, the silicon quantum dots are grown in matrix of insulating silicon dioxide, and they have the dimensions of 2 or 3 nm.

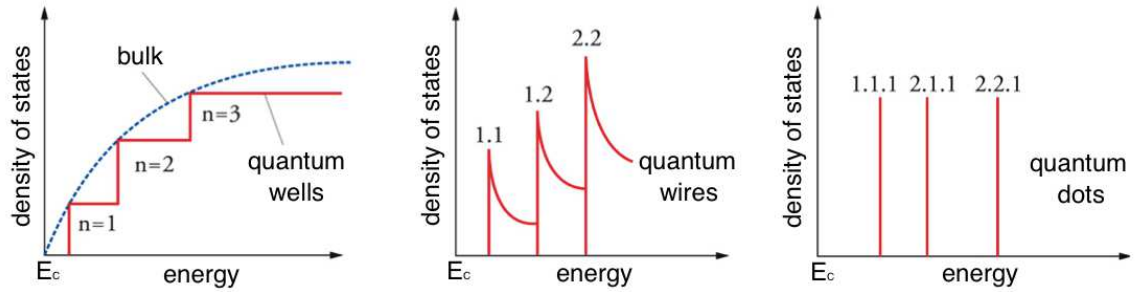


Figure 1.5. Density of states for systems of two (quantum wells), one (quantum wires), zero (quantum dots) dimensions. Quantum numbers for the different states are also shown in the picture: a single number identifies a quantum well, two numbers a quantum wire and three a quantum dot.

In addition to causing the blue shift of the silicon band edge emission into the near infrared or red spectral range, the quantum confinement in the silicon nanocrystals gives brighter emission than the one observed from bulk silicon. The brighter emission must be explained by some combination of enhancement in the absorption cross section and radiative recombination rate and decrease in the rate of non-radiative recombination. Experiments suggest that the absorption cross section in silicon nanocrystals shows little or no enhancement over bulk silicon on a per-atom basis. Of the remaining two factors, most of the improvement in radiative recombination efficiency comes from a dramatic decrease in the nonradiative recombination rate. Nonradiative exciton recombination in bulk silicon is typically dominated by Shockley-Hall-Read recombination at mid gap defect states corresponding to defects and impurities in the crystal. In nanocrystals that are small enough to show quantum confinement effects, such defects are

thermodynamically unfavorable and tend to grow out of the quantum dot. Two other recombination mechanisms that contribute to the inefficiency of light emission in bulk silicon are recombination at surface defects and Auger recombination, in which the energy of the exciton is transferred to a third charge carrier. Both of these mechanisms can be worse in silicon nanocrystals than in bulk silicon. The enhanced sensitivity to surface recombination can be understood by noting the high surface-to-volume ratio, while the rapid Auger recombination rate in charged nanocrystals results from the large effective carrier concentration that a single carrier represents in the small nanocrystal volume. There are two factors that contribute to improvement in the radiative recombination rate in silicon nanocrystals. The first can be understood in the context of Fermi's Golden Rule for quantum mechanical transitions, which can be derived using time dependent perturbation theory. In the formalism of Fermi's Golden Rule, the rate of an optical dipole transition is proportional to the magnitude of an off-diagonal matrix element calculated by evaluating an overlap integral that connects the electron and hole wavefunctions together through the dipole operator. Because the nanocrystal forms a potential well that confines the electron and the hole spatially, these wavefunctions overlap more in position space and the matrix element for the transition increases [22]. At the same time, the uncertainty in momentum space that confinement introduces relaxes the momentum conservation rule and allows a greater proportion of the phonon density of states to assist in the indirect band-to-band transition [23].

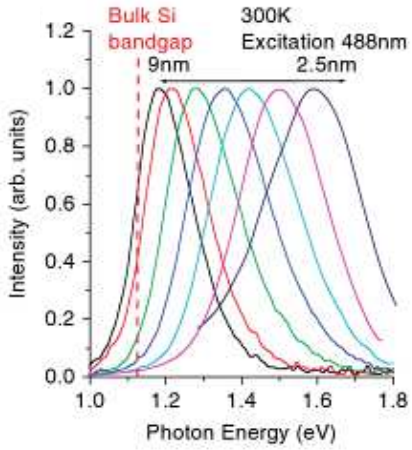


Figure 1.6. Room temperature PL spectra of Si nanocrystals embedded in SiO_2 thin films. The average diameters are changed from about 9 to 2.5 nm. Excitation wavelength is 488 nm.

Figure 1.6 shows the photoluminescence (PL) spectra of Si-NCs embedded in silica films at room temperature with an excitation wavelength of 488 nm [24] . In my work, I will study the luminescence of Si-NCs under electrical pumping.

1.4.1 Silicon nanocrystals formation techniques

The most widely used approach to create the Si-NCs is based on the deposition of sub-stoichiometric silicon dioxide (SiO_2) films, with a large excess of silicon, followed by a high temperature annealing. The annealing causes a phase separation between the two constituent phases, i.e. Si and SiO_2 with the formation of small silicon nanocrystals. The size and the density of the Si-NCs can be controlled by the deposition and the annealing parameters. The chemical vapor deposition (CVD) is a key process in semiconductor fabrication to deposit thin films on semiconductors. In this section, I will describe both the Low-Pressure CVD (LPCVD) and the Plasma-Enhanced CVD (PECVD), which are the two different deposition techniques used in the fabrication of the samples studied in this thesis.

LPCVD is a process used in the manufacturing of thin films with a thickness ranging from a few nanometers to many micrometers. LPCVD is used to deposit a wide range of film compositions with good conformal step coverage. These films include a variety of materials including polysilicon for gate contacts, thick oxides for isolation, doped oxides for global planarization, nitrides and other dielectrics. LPCVD is similar to other types of CVD in that it is a process where gaseous specie reacts on a solid surface or wafer to produce a solid phase material. The LPCVD process can be summarized as a consequence of four different steps. First, the reacting gaseous species are transported to the surface. Second, the gaseous species absorb into the surface of the wafer. Third, the heterogeneous surface reaction produces reaction products. Finally, the gaseous reactants are removed from the surface. The low pressure used in the reactor distinguishes LPCVD from other CVD processes. The main reason for using LPCVD is the ratio of the mass transport velocity and the velocity of reaction on the surface. When the ratio is close to one, the two velocities are of the same order of magnitude. The velocity of the mass transport depends mainly on the reactant concentration, diffusion, and thickness of the border layer. When the pressure is lowered during LPCVD, the diffusion of the gas decreases proportionally to the reciprocal of the pressure. The pressure for LPCVD is usually around 10-10^3 Pa. The LPCVD process has a quartz tube placed in a spiral heater that starts with tube pressure at very low pressure, around 0.1 Pa. The tube is then heated to the desired temperature and the gaseous species (“working gas”) is inserted into the tube at the pressure predetermined between 10 and 1000 Pa. Figure 1.7 shows the system used for the LPCVD technique deposition. The working gas consists of a dilution gas and

the reactive gas that will react with the substrate and create a solid phase material on the substrate. After the working gas enters the tube, it spreads out around the hot substrates that are already in the tube at the same temperature. The substrate temperature is extremely important and influences what reactions take place. This working gas reacts with the substrates and forms the solid phase material and the excess material is pumped out of the tube. One of the most interesting peculiarities of the LPCVD technique is that it is suitable for the deposition of silicon dioxide and polysilicon. The samples produced with LPCVD studied in my thesis work have been fabricated at the CEA-LETI laboratory in Grenoble.

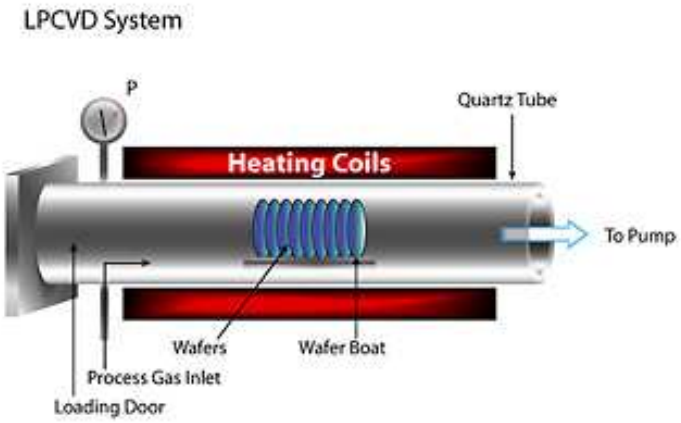


Figure 1.7. LPCVD system.

PECVD is used to deposit SiO_2, Si_3N_4 (Si_xN_y), $Si_xO_yN_z$ and amorphous Si films. In this method of CVD, plasma is added in the deposition chamber with reactive gases to create the desired solid surface on the substrate. Plasma is a partially ionized gas with high free electron content (about 50%). Plasmas are divided into two groups: cold (also called non-thermal) and thermal. In thermal plasmas, electrons and particles in the gas are at the same temperature; however, in cold plasmas the electrons have a much higher temperature than the neutral particles and ions. Therefore, cold plasmas can utilize the energy of the electrons by changing just the pressure. This allows a PECVD system to operate even at low temperatures (between 100 and 400 °C). The energy from the electrons in cold thermal plasmas is useful in PECVD. When the mean free path is large and the system size is small, the free electrons do not exchange energy with ions before they collide with other gasses. The energy from the electrons is then used to dissociate the reactive gas in order to form the solid film on the substrate. In order to excite and sustain

the plasma, a voltage must be applied to the plasma. The voltage is usually applied using an RF signal between two electrodes. The PECVD systems must contain two electrodes (in a parallel plate configuration), plasma gas, and reactive gas in a chamber. To begin the PECVD process, a wafer is placed on the bottom electrode and a reactive gas with the deposition elements is introduced into the chamber. Plasma is then introduced into the chamber between the two electrodes, and voltage is applied to excite the plasma. The excited state plasma then bombards the reactive gas causing dissociation. This dissociation deposits the desired element onto the wafer. Advantages of PECVD include the low temperature, high film density for dielectric, and ease of cleaning the chamber. Disadvantages include the expense of the equipment and the stress of plasma bombardment. Figure 1.8 shows the system used for the PECVD deposition, with in evidence the precursor gases and the RF power used to excite the plasma.

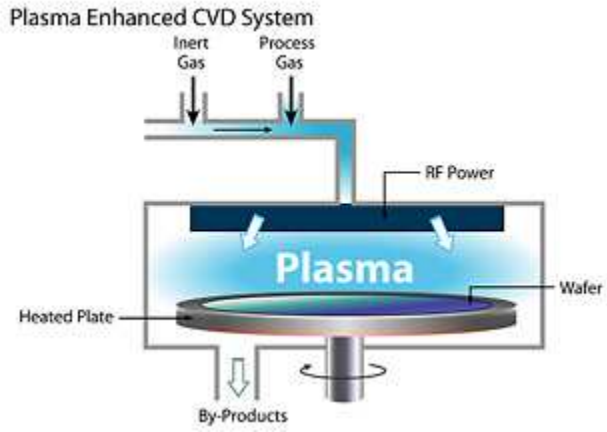


Figure 1.8. PECVD system.

The samples produced with PECVD studied in my thesis work have been fabricated at the “Advanced Photonics and Photovoltaics” (APP) Group of the Bruno Kessler Foundation, in Trento.

In my thesis work, I have studied samples fabricated both with LPCVD and PECVD deposition processes. For every section of my work, I will specify the deposition technique, and the used main parameters, such as the silicon content excess, the annealing time and the annealing temperature.

1.4.2 Metal Oxide Semiconductor Structure

Silicon nanocrystals (Si-NCs) based light emitting devices (LEDs) typically present a metal oxide semiconductor (MOS) capacitor structure. A typical MOS structure is shown in Figure 1.9. The metal plate is usually a heavily n-doped polysilicon layer, which behaves like a metal, and it is called the gate. The insulating layer is composed by silicon dioxide and the other plate of the capacitor is a semiconductor layer, which in this case is p-type silicon, and it is called body. The band diagrams for the three materials taken separately are shown in Figure 1.10.

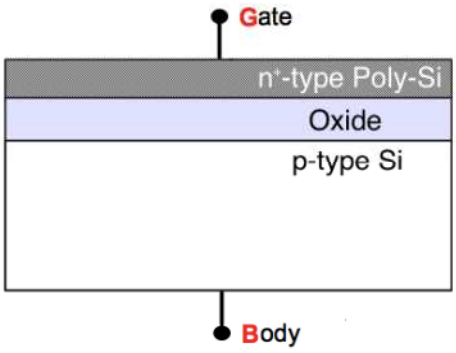


Figure 1.9. Simplified scheme of a metal oxide semiconductor (MOS) capacitor.

A relevant quantity is the work function, qΦ, which is defined as the energy required to extract an electron from the Fermi level and to bring it to the vacuum level. Depending on the metal, one may have different Φ_m values, as well as, depending on the concentration of the impurities within the semiconductor, there are also different values for Φ_s.

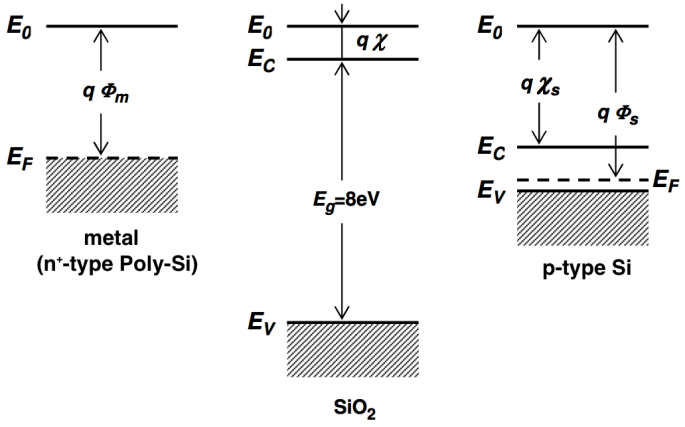


Figure 1.10. Band diagram for metal, silicon dioxide and p-type silicon, respectively. qχ is the semiconductor electron affinity, while qΦ is the work function.

Typically the work function $q\Phi_m$ for an n^+-type polysilicon is 4.05 eV. For a p-type silicon $q\Phi_s$ is around 5 eV. The electron affinity, $q\chi$, depends on the material and it is defined as the minimum energy required moving an electron from the bottom of the conduction band to the vacuum level. The electron affinity for silicon is 4.15 eV, while for SiO_2 is 0.95 eV. Now the problem is what happens when we combine the three layers together in order to form the MOS capacitor.

In this case, there are several assumptions, which have to be taken into account to reach a simple model. We assume that the insulator layer has infinite resistance; hence no charge carrier can pass through the dielectric layer when a bias voltage is applied between the metal and the semiconductor. The thickness of the semiconductor layer, supposed to be uniformly doped, has to be chosen large enough to allow the formation of a wide depletion region. The metallic gate is thought as an equipotential region and an ohmic contact has been established between the semiconductor and the metal contact on the backside of the device. Moreover no lattice mismatches are present at the interfaces and, despite the fact that silicon dioxide is in amorphous phase, the band diagram is assumed to be that of crystalline SiO_2. These last simplifications allow for neglecting interface trapped charges and oxide charges which surely are present in a real MOS structure. Therefore, neglecting boundary effects, the problem can be considered as a one-dimensional one (only the x-coordinate). Figure 1.11 shows the band diagram in a MOS structure for different applied voltages at the metal contact.

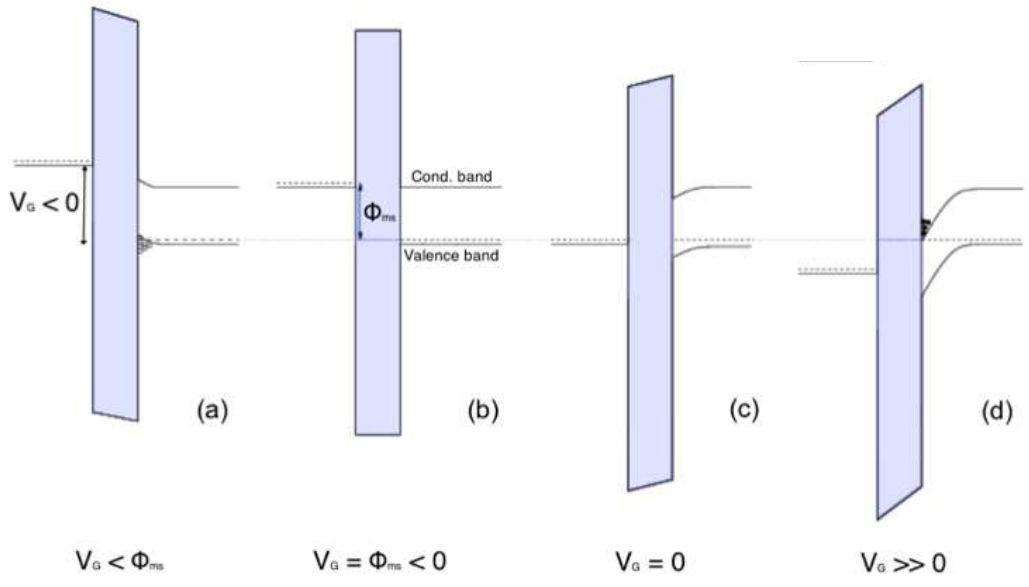


Figure 1.11. Band diagram in a p-MOS structure in accumulation **(a)**, under flat band condition **(b)**, without bias **(c)**, and under inversion condition **(d)**.

The differences between the work function in the metal and the work function in the semiconductor is

$$q\Phi_{ms} = q\Phi_m - q\Phi_s < 0$$

and the voltage which has to be applied to achieve flat bands is the flatband voltage

$$V_{FB} = \Phi_{ms}$$

Now, I will explain the three different working MOS regimes: accumulation, depletion, inversion, respectively.

With large negative bias applied to the gate as shown in Figure 1.11.a, holes are attracted by the negative potential to form an accumulation layer at the silicon surface with higher concentration than in the bulk silicon. The valence band edge E_V bends upward near the silicon surface approaching to the Fermi level. Since the carrier density depends exponentially on the energy difference (E_F-E_V) this band bending causes an accumulation of majority carriers (holes) near the semiconductor surface. The high concentration of these holes forms the second electrode of a parallel plate capacitor with first electrode at the gate.

When the bias is reduced, negative charges are removed from the gate, holes leave the accumulation layer until the silicon will be neutral everywhere. This happens when the applied gate bias is the flat band voltage (Figure 1.11.b). As the bias on the gate is made more positive with respect to V_{FB}, holes are repelled and a region depleted of carriers is formed at the surface. Under depletion conditions, the bands bend downwards. A special case of this regime occurs when no bias is applied to the capacitor, as illustrated in Figure 1.11.c. Increasing V_G at positive voltages; the width of the surface depletion region tends to obtain larger values.

With increasingly applied positive voltage, the surface depletion region will continue to widen until the onset of surface inversion is observed. An inversion layer is formed; the bands bend further downgrade till the Fermi level near the silicon surface will lay close to the bottom of conduction band (Figure 1.11.d). This inversion layer is very thin and separated from the bulk of silicon by the depletion layer. The build-up of inversion layer is a threshold phenomenon. The threshold voltage V_T marks the equality of the concentration of minority carriers (electrons) to the doping concentration. At the onset of inversion, the depletion layer width reaches a limit.

Summarizing there are three regions of interest: accumulation, depletion and inversion corresponding to three different bias voltages. The charge distribution corresponding to these conditions is shown in Figure 1.12.

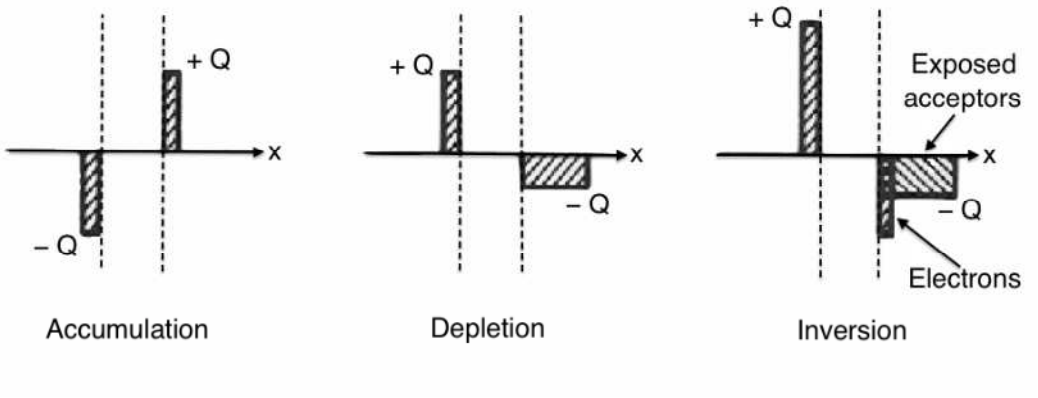


Figure 1.12. Charge distribution in a MOS capacitor under accumulation, depletion and inversion condition [25].

The capacitance of the MOS structure depends, in turn, on voltage that is applied to the body. The dependence is shown in Figure 1.13, where the three regimes of operation are separated by two voltage values: V_{FB} which separates the accumulation regime from the depletion regime and V_T which demarcates the depletion regime from the inversion regime [26].

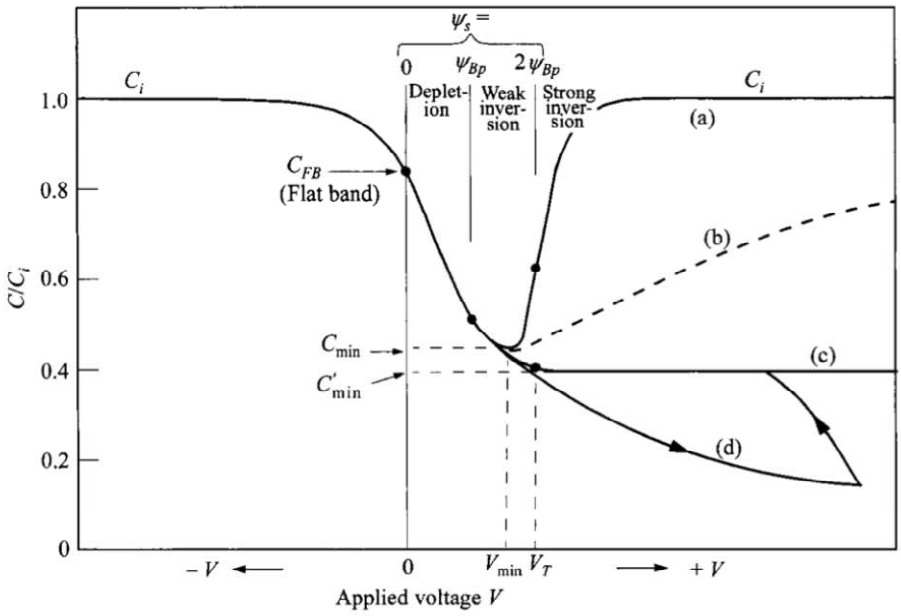


Figure 1.13. Typical Capacitance-Voltage (C-V) curves showing the three different regimes: accumulation, depletion (the flat-band condition is assumed occurring with no bias applied), inversion for low frequency (a), intermediate frequency (b) and high frequency (c) in a p-MOS structure. Curve (d) represents the deep depletion condition, i.e. high frequency with fast sweep (After Sze [27]).

In the depletion condition ($V_{FB} < V_G < V_T$), the capacitance from the gate to the substrate associated with the MOS structure decreases, because a capacitance associated with the surface depletion region adds in series to the capacitance across the oxide.

At the onset of the inversion condition ($V_G > V_T$), the depletion layer width reaches its limit. Since the charge density in the inversion layer may or may not be able to follow the alternating current variation of the applied gate voltage, it follows that the capacitance under inversion conditions will be a function of frequency. At low frequency the increment in the gate charge is balanced by the substrate charge. Therefore, the low frequency capacitance of the structure is equivalent to that of the oxide layer, just as in accumulation mode. Differently, at higher frequencies, the increase of charge in the metal side is not balanced by the substrate charge, since the minority carriers can no longer adjust their concentration. The number of minority carriers in the inversion layer therefore remains fixed at its dc value and the depletion width simply fluctuates about this value. This situation is equivalent to two parallel-plate capacitors in series.

Summarizing, an overall theory can now be constructed by combining the results of the accumulation, depletion and inversion considerations. Specifically, we expect the MOS capacitance to be approximately constant at C_i under accumulation biases, to decreases as the dc bias progresses through the depletion, and to be approximately constant again under inversion biases at a value equal to ~ C_i if the frequency is low or to C'_{min} if we are in the high frequency regime.

On the other side, the current-voltage (I-V) of a MOS diode critically depends on the insulator thickness. If the insulator layer is sufficiently thick (greater than 5 nm for the Si/SiO_2 systems), carrier transport through the insulator layer is negligible and the MOS diode represents a standard conventional capacitor. Alternatively, if the insulator layer is very thin (less than 1 nm), little impediment is provided to carrier transport between the metal and the semiconductor, and the structure represents a Schottky-barrier diode. The last type of devices with an intermediate layer thickness (1 nm < d_{ox} < 5 nm) is the MOS tunnel diode. I will take into account two relevant cases: the MOS tunnel diode on degenerate semiconductor substrate and, then, the MOS tunnel diode on non-degenerate semiconductor substrate. Figure 1.14 shows simplified band diagrams, including also the interface traps, for a MOS tunnel diode with degenerate (p^{++}) semiconductor substrate. Applying a positive voltage to the metal (see Figure 1.14.a), causes electron tunneling from the valence band to the metal. This tunneling current is always assumed to be allowable and increases monotonically with the increasing energy range between the Fermi levels. It further increases with the decreasing insulator barrier height. Applying a small negative voltage to the metal, (see Figure 1.14.b), results in electron tunneling from the metal to the unoccupied semiconductor valence band (Arrow 1). According to Figure

1.14.c, an increase of the voltage –V implies an increase in the effective barrier height for electron tunneling from the metal to the unoccupied states of the valence band. However, electrons in the metal with higher energies can tunnel simultaneously into the empty interface traps and momentarily recombine with holes in the valence band, resulting in another current component (Arrow 2 in Figure 1.14.c). Finally, an additional increase of the bias results in a third very fast-growing tunnel current component from the metal into the conduction band of the semiconductor (see the Arrow 3 in Figure 1.14.d). Figure 1.15 shows the measured I-V characteristics at room temperature (solid lines) and at liquid nitrogen temperature (dashed lines) for three p^{++} silicon samples with a thin oxide layer (2 nm) [27].

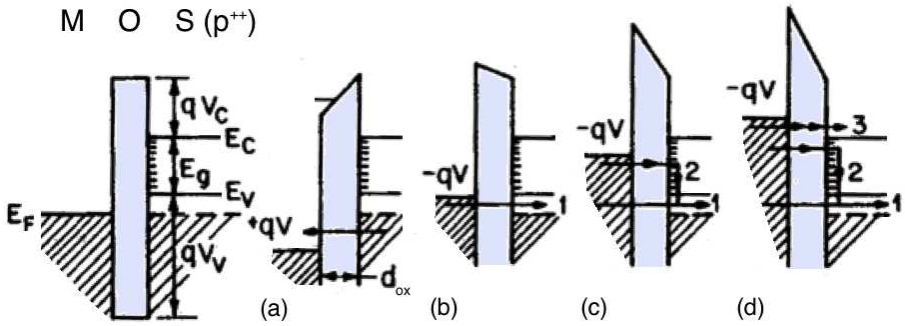


Figure 1.14. Simplified band diagrams, including the interface traps, of a MOS diode on degenerate substrate.

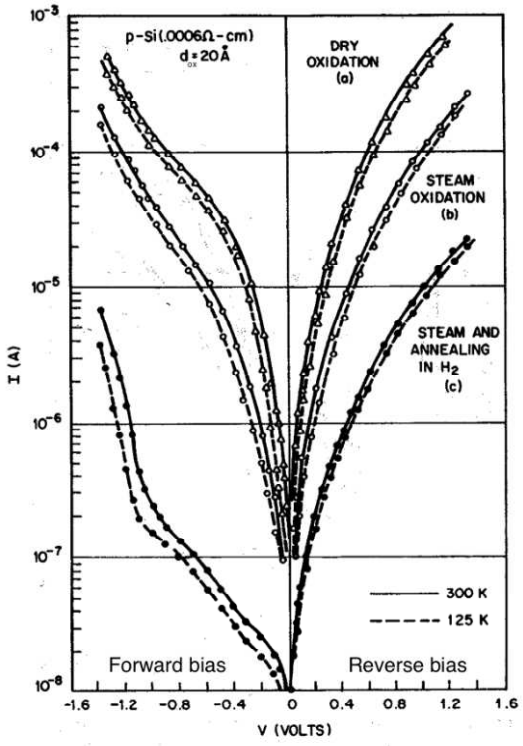


Figure 1.15. Measured I-V characteristics for different p^{++} silicon samples with the oxide layer (2 nm) treated in different ways (After Sze [27]).

Notice the small influence of the temperature on the I-V curve, which is typical for tunneling. The I-V characteristics of curves (a) and (b) show, in principle, the same trend as curve (c), but exhibit considerably increased currents especially in the forbidden energy range (- 1.1 V < V < 0 V). The left branches of the curves for V < - 1.1V represent electron tunneling from the metal into the conduction band. The right branches represent tunneling from valence band into the metal.

For a MOS tunnel diode with non-degenerate semiconductor substrate, the energy-band diagram at thermal equilibrium is shown in Figure 1.16.

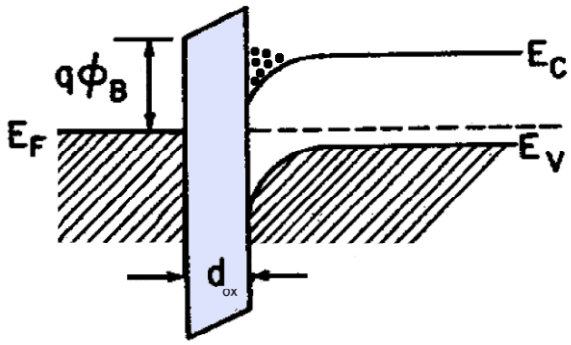


Figure 1.16. Energy band diagram at thermal equilibrium for a MOS diode on non-degenerate substrate with a metal-insulator barrier height of 3.2 eV.

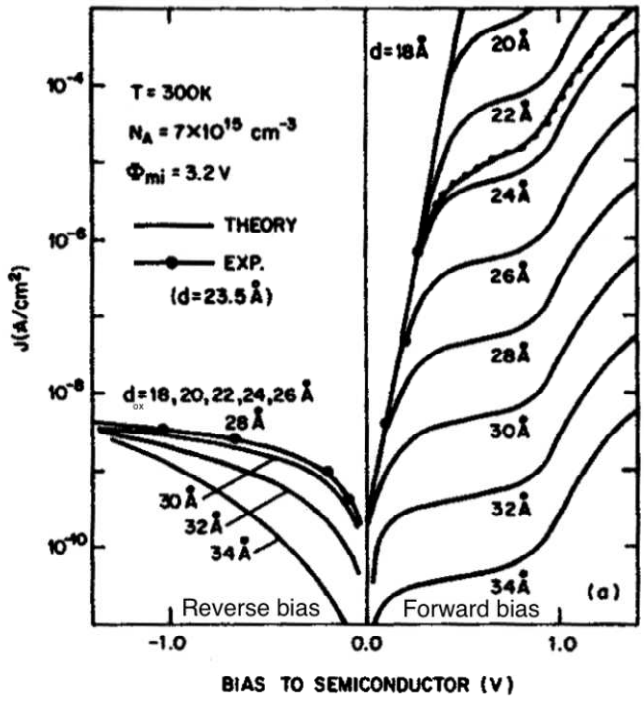


Figure 1.17. Simulated current-voltage characteristics of MOS tunnel diodes with different insulating layer thickness. Experimental results obtained for dox (insulating layer) = 2.35 nm are also shown in the picture (After M. Green [28]).

One of the most important parameters for this diode is the metal insulator barrier height, which has a profound effect on the I-V characteristics. For the shown case ($q\Phi_B$ = 3.2 V), the surface of the p-type silicon is inverted. Two main current components exist: J_{c-m} from the conduction band to the metal and J_{v-m} from the valence band to the metal. Figure 1.17 shows the theoretical I-V curves computed for different oxide layer thicknesses.

Under small forward and reverse biases, the dominant current is the minority (electron) current J_{c-m}, since the Fermi level is close to the conduction band edge. As the forward bias increases the current also increases monotonically. At a given bias, the current increases rapidly with decreasing insulator thickness. At reverse bias the current is virtually independent of the insulator thickness for d_{ox} < 3nm, because now the current is limited by the rate of supply of minority carriers (electrons) through the semiconductor, and is similar to the saturation current in a reverse biased p-n junction. Figure 1.16 also shows the experimental results for d_{ox} = 2.35 nm. Note that there is a good agreement between theory and experiment, and the current voltage characteristics are very similar to those of a p-n junction.

1.4.3 Charge injection and light emission in silicon nanocrystals

In this section, a summary of the basic transport mechanisms and the main excitation processes that can occur in an insulator layer structure is reported. In particular, I will summarize some concepts, which I will use in the following of my thesis. Due to the constant downscaling of the gate-dieletric thicknesses in the MOS devices, the tunneling effects have drastically gained relevance. The quantum mechanical tunneling describes the transition of carriers through a classically forbidden energy state. This can be an electron tunneling through a dielectric, which represents an energy barrier, from one side to the other of the MOS structure. Even if the energy barrier is higher than the electron energy, there is, quantum mechanically, a finite probability of this transition. As the wavefunction of the particle penetrates the barrier and can even extend to the other side, quantum mechanics predict a non-zero probability for an electron to be on the other side. The different types of electronic conduction for p-MOS device under forward bias are summarized in Figure 1.18.

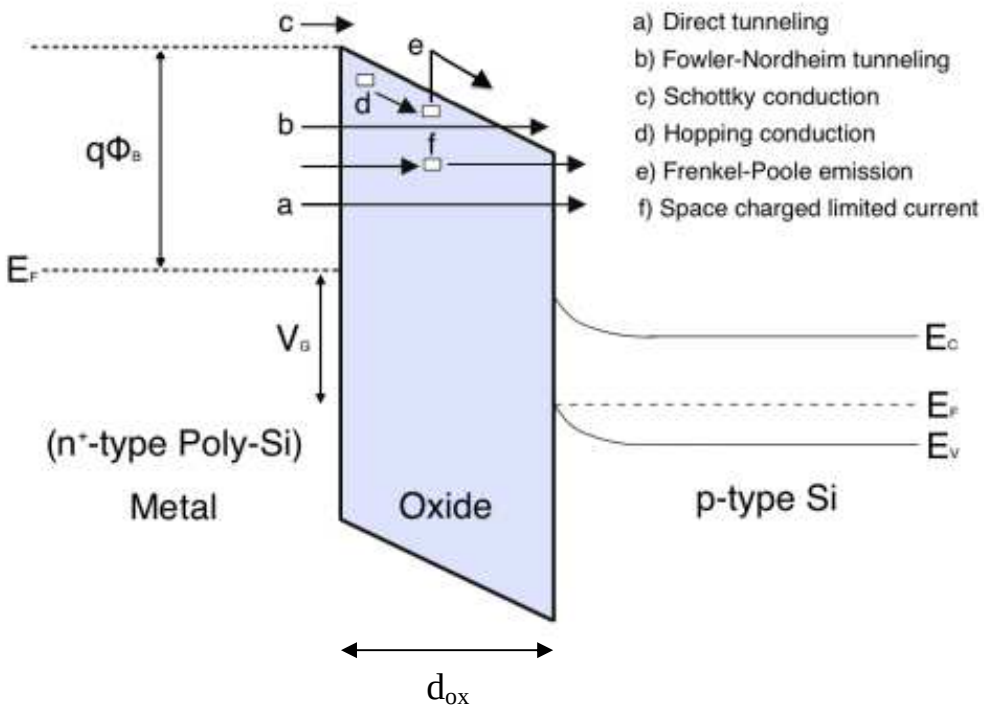


Figure 1.18. The gate current in the thin oxides layer under forward bias may be due to the different mechanisms of electronic conduction. The electron may freely travel inside the oxide layer (thermionic effect, direct tunnel and Fowler-Nordheim tunneling), or their transport may be associated with traps (Poole-Frenkel effect, hopping conduction, and space charge limited current).

The tunneling mechanisms are the most common conduction mechanisms through the insulators. The tunneling itself has a strongest dependence on the applied voltage, but it is essentially independent from the temperature. Considering the shape of the energy barrier, direct tunneling (see Figure 1.18 (a)) or Fowler-Nordheim tunneling (see Figure 1.18 (b)) can be distinguished, depending on whether carriers tunnel through the whole or only partial width of the barrier respectively. In the case of the direct tunneling, the barrier shape is trapezoidal, while in the case of the Fowler-Nordheim tunneling is triangular. The most common approach used to express the tunneling current in such devices is the Tsu-Esaki formula. All the details about this expression can be found in the reference [29].

The model most frequently used to describe tunneling for thick dielectrics and high electric fields, where gate electrons cross a triangular energy barrier shape, is the Fowler-Nordheim formula [30]. The mathematical expression is here reported.

$$J = A \cdot E_{ox}^2 \cdot exp^{\left(-\frac{B}{E_{ox}}\right)}$$

which was originally used to describe the current density due to the tunneling between metals under intense electric field, E_{ox}, defined as the ratio V_{ox}/d_{ox} (voltage applied over the thickness of the oxide barrier – see Figure 1.18). The parameters A and B have been refined by Lezlinger and Snow [31]. The resulting tunneling expression is the following:

$$J = \frac{q^3 m_e^*}{8\pi m_{ox} h q \Phi_B} \cdot E_{ox}^2 \cdot exp^{\left(-\frac{8\pi\sqrt{2m_{ox}(q\Phi_B)^3}}{3hq \cdot E_{ox}}\right)}$$

where q is the elementary charge value, m* is the effective electron mass, m_{ox} is the effective electron mass in the dielectric, h is the Planck constant and $(q\Phi_B)$ is the difference between the Fermi level in the electrode and the conduction band edge in the dielectric. In this case, the electrons do not tunnel directly to the other side of the barrier. Instead they tunnel from the gate contact to the conduction band of the dielectric layer from where they are injected into the semiconductor.

There are also other possible injection processes, which I have shown in Figure 1.18, and which I will briefly describe here, without entering in too much detail. In the Schottky conduction, the thermionic emission over the metal-insulator barrier is the responsible for the carrier transport. Besides the tunneling and the thermionic conduction, which are defined and found in the literature as one-step tunneling processes, defects in the dielectric layer give rise to tunneling processes based on two or more steps. It is assumed that traps arise in the dielectric layer due to the repeated high voltage stress. For thicker dielectrics with a high defect density it is reasonable to assume that also the interaction of two or more traps in the tunneling process takes place. This is the case of the hopping conduction, in which the energy of the electrons is less than the maximum energy of the height trap potential well. The Poole-Frenkel emission (see Figure 1.18 (e)) is instead due to the field-enhanced thermal excitations of the trapped electrons into the conduction band. The model which describes this emission of trapped electrons could be found in the reference [32]. The main motivation to use this expression is that the trap-assisted current density has been found to be a linear function of the square root of the electric field in the dielectric, E_{ox}. It has to be noticed that this is in contrast to the Fowler-Nordheim tunneling current, which is instead a linear function of the electric field E_{ox}. In the case of the hopping conduction and of the Poole-Frenkel emission, the electric field is assumed constant. When the electron injection is strong, this hypothesis is no more valid

and the potential distribution should be calculated using the Poisson's equation. The space charge limited current results from a carrier injected into the oxide, where no compensating charge is present (see Figure 1.18 (f)).

Therefore, the main problem of having light from devices based on silicon nanocrystals is the difficult carrier injection since the host matrix for the Si-NCs is an insulator.

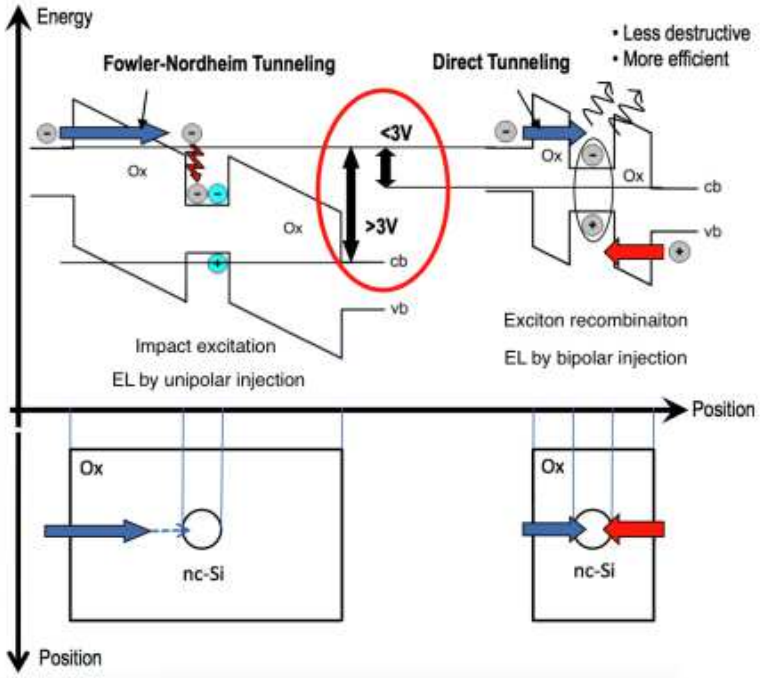


Figure 1.19. Electron-hole pairs are usually generated in silicon nanocrystals either by bipolar injection from both electrodes of the diode or by impact excitation (unipolar injection).

In theory, the charge injection mechanism should be possible when the thickness of the silicon oxide between the silicon nanocrystals is reduced at a value that tunneling currents become important. Figure 1.19 shows how the electron-holes pairs can be generated in silicon nanocrystals. The electrical injection into the silicon quantum dots is a complex and a delicate task. Electroluminescence can be produced either by blackbody radiation or by impact excitation of electron-hole pairs in the Si-NCs by energetic electrons which tunnel through the dielectric by a Fowler-Nordheim process (see Figure 1.19 on the left). In this particular case, the electron has to flow through a barrier with a triangular shape. Electron-hole pairs excited in this way recombine radiatively with an emission spectrum which is very similar to the one obtained by photoluminescence. The problem with impact excitation is its inefficiency and the damages it induces in the oxide

due to the energetic electron flow. To get a strong electroluminescence one should try to get bipolar injection, with the simultaneous injection of electron and holes within the Si-NCs (see Figure 1.19 on the right). In this particular case, the carrier has to flow through a barrier with a trapezoidal shape. The direct tunneling is a conduction mechanism which leads to large injected electrical currents at low applied voltages (less than 3.1 V, which corresponds to the barrier height at the interface of the SiO_2), without leading to the oxide degradation. A right silicon oxide thickness to permit transport is as low as a few nm.

The barrier height and the oxide thickness determine which one is the prevailing mechanism between bipolar (direct tunneling) and unipolar (Fowler-Nordheim tunneling) injection, as shown in Figure 1.20. This Figure shows the main injection mechanisms for different working conditions, depending on the silicon dioxide thickness and the applied electric field. It is interesting to notice that the difference between the direct tunneling and the Fowler-Nordheim one occurs for values of the applied electric field between 6 MV/cm and 8 MV/cm: for the standard thickness of a MOS capacitor active material, this electric field corresponds to an applied bias voltage of 3 V.

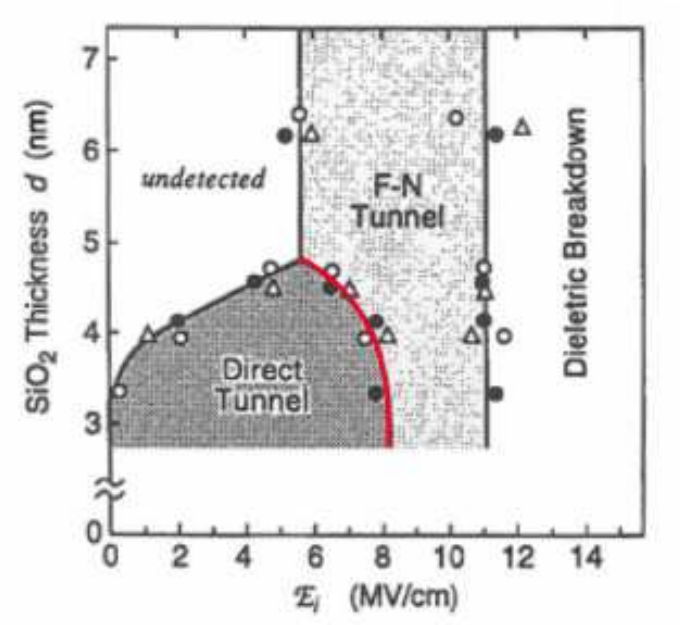


Figure 1.20. Relationship among oxide electric field, oxide thickness and current mechanism through thin silicon dioxide layer [33].

1.5 Silicon Nanocrystals Based Light Emitting Devices

Despite the advantages that the nanostructured silicon offers in comparison to bulk silicon, it is still a relatively poor optical material compared to the direct gap III-V semiconductor materials. The radiative rate, which ultimately limits the optical power that can be radiated by a volume of material, is perhaps one or two orders of magnitude faster for the Si-NCs than for the bulk silicon at 10 kHz. However it is four orders of magnitude slower than the 1 GHz emission rates found in materials such as GaAs. While the radiative recombination efficiency is high, the insulating matrix that surrounds and defines the quantum dot complicates the electrical injection of carriers. Table 1.1 shows a classification of the various efficiencies, used in the following of this work. Silicon nanocrystals based light emitting devices have been fabricated and such devices can reach efficiency up to 0.17 % at low injected current and a turn-on voltage of 1.7 V [34], fully compatible with the CMOS technology itself. Table 1.2 shows in a very simplified timeline frame the network of historical events which led to the present state of the development of the Si-based sources. I have decided to put the developments in the last 20 years, because they are the most significant for my thesis work. The complete table can be found at the reference [35] . In Table 1.2 there are both visible and infrared (IR) devices, because the work done in this thesis will be focalized on both of these two topics. In fact, even if the silicon nanocrystals emission is far from the 1.3 μm and 1.5 μm telecommunications spectral windows, they can be coupled to the emission of erbium ions to create a hybrid optical material [36]. This fact and the possibility to reach energy transfer between the silicon quantum dots and the erbium ions has made the Si-NCs more attractive for the data transfer application and the optical interconnections.

Internal Quantum Efficiency	Number of photons emitted versus the number of electron-hole pairs generated
External Quantum Efficiency	Number of photons externally detected versus the number of charge injected
Power Efficiency	Watts of light detected versus the watts of electricity used to drive the device

Table 1.1. Classification of the various efficiencies in Si based LEDs.

Year	Infrared Devices	Visible Devices
1990		Porous Si Photoluminescence (Canham)
1994	RT Er-doped SiOx LEDs (Franzo et al.)	
1996		Integrated porous Si LED (Hirschman et al.)
2000	Si/SiGe cascade laser (Dehlinger et al.)	Optical gain in Si quantum dots (Pavesi et al.)
2001	Optical gain in Er doped Si QDs (Han et al.)	
2002		Si quantum dots LED (Franzo et al.)
2003	Er doped Si QDs LEDs (Castagna et al.)	
2006	Er doped microdisk laser (Kippenberg et al.)	
2008	Cascaded Si Raman laser (Rong et al.)	
2010	Room temperature Ge laser (Liu et al.)	
2012	Electrically pumped Ge laser (Camacho-Aguilera et al.)	

Table 1.2. Development of Si-based light sources [35].

Indeed, when incorporated in silicon dioxide, the Er^{3+} ions exhibit a weakly allowed atomic transmission at 1.54 μm that is well aligned with the transmission maximum in the optical fibers. For this reason erbium doped fiber amplifiers are commonly used in long distance telecommunications to restore the intensity of optical signals. Because the radiative rate of silicon nanocrystals is fairly low, nonradiative near field energy transfer to erbium ions placed in close proximity to the nanocrystal can be the dominant recombination pathway for excitons. In this way, silicon nanocrystals have been shown to be effective sensitizers for erbium ions in optically pumped waveguide amplifiers. Figure 1.21 shows the energy band diagram for silicon nanocrystals and erbium ions and how energy transfer can occur in such systems. Figure 1.22 shows instead a photoluminescence experiment (PL) performed on two different samples: one with only Si-NCs, and one with Si-NCs and Er^{3+} ions. The PL spectrum is respectively the red one for the first sample and the black one for the second one. The excitation wavelength is 476 nm, which is non resonant with any of the Er^{3+} internal transitions. This experiment has been performed in our photoluminescence laboratory by Nikola

Prtljaga. In the PL spectra, we can clearly observe the erbium emission at 980 nm and at 1535 nm. Moreover, the most important aspect which has to be noticed is that the Si-NCs related PL band around 800 nm is reduced by energy transfer to the Er^{3+} ions.

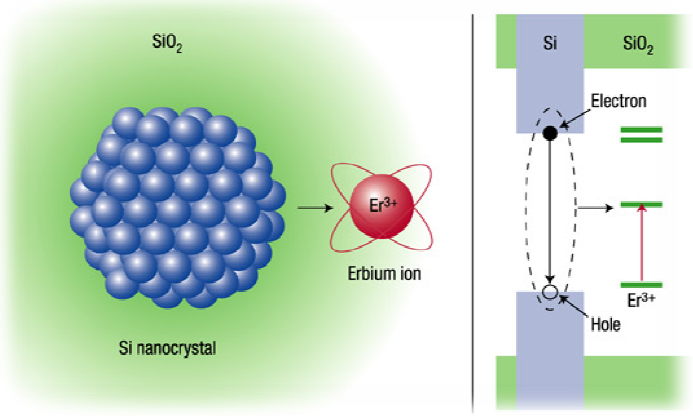


Figure 1.21. **(left)** The wavefunction of an electron–hole pair ('exciton') in a silicon nanocrystal can couple to a nearby Er ion in the silica matrix. **(right)** Energy bands are shown for silicon nanocrystals and erbium ions embedded in a SiO_2 matrix. An excited electron–hole pair in the nanocrystal can recombine by transferring energy to an Er^{3+} ion. The latter is then excited from the ground state to the first excited state as indicated by the red arrow. Here atomic-scale engineering in combination with nanoscale energy transfer can lead to the development of a new class of miniature optical amplifiers (After Polman [37]).

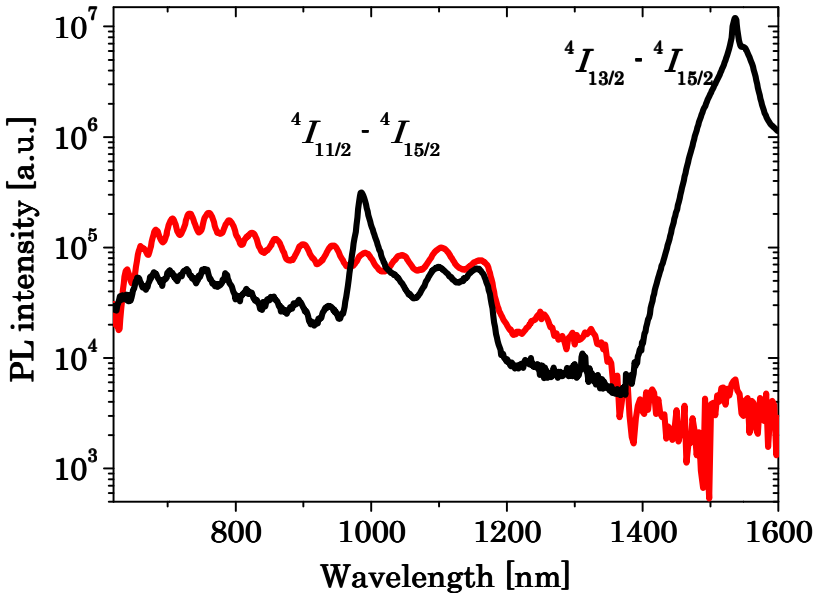


Figure 1.22. Room temperature photoluminescence spectra of two different samples (red line Si-NCs embedded in a silicon oxide matrix, black line Si-NCs and Er^{3+} ions in SiO_2). Symbols on the spectra refer to the internal transition between the indicated states of the Er^{3+} ions. The excitation laser wavelength is 476 nm. These plots are a courtesy of Nikola Prtljaga.

The photoluminescence measurements here reported have proved the energy transfer between the silicon nanoclusters and the erbium ions under optical excitation. Moreover, all optical pump-probe experiments have demonstrated that a positive signal enhancement can be achieved in thick slot waveguide, having Si-NCs and Er^{3+} ions as active material [38]. Both the energy transfer and the signal enhancement in such systems will be object of study in my work. What is new of my approach is that the pumping will be electrical.

1.6 Outline of the thesis

In the present work the electroluminescence and the transport properties of silicon nanocrystals based devices have been studied. The thesis is divided into two main topics. The first one is related to the study and the experimental characterization of silicon nanocrystals based light emitting devices. The devices have been fabricated either at the Bruno Kessler Foundation in Trento or at the CEA-LETI laboratory in Grenoble. In the second, I will present my work done on erbium doped silicon nanocrystals based optical cavities, from the design and the simulation, up to the optical and the electrical characterization. In this case the devices have been fabricated by the CEA-LETI laboratory in Grenoble.

This thesis presents an experimental work realized at the Nanoscience Laboratory of the University of Trento. All the experimental setups assembled and used are presented in the appendix A. The chapters are organized as follows:

In chapter 2, I present the fabrication and the characterization of silicon nanocrystals based light emitting devices. This work has been financed by the Intel Corporation and it has been performed in collaboration with the APP Group of the Bruno Kessler Foundation. Devices produced by different batches and different layouts are studied and compared in terms of structural properties, conduction mechanisms and electroluminescence properties. Finally, I discuss current-voltage, capacitance-voltage characteristics and time resolved electroluminescence measurements. Power efficiency is evaluated and studied in order to understand the relation between the exciton recombination mechanisms and the electrical conduction.

Chapter 3 describes the fabrication and the characterization of silicon nanocrystals based light emitting devices realized at the CEA-LETI laboratory in Grenoble with the financial support of the European Commission, through the project ICT-FP7-224312 HELIOS. Devices produced by single layer or multilayer depositions are studied and the electrical charge transport is discussed as a function of different fabrication parameters. I report also electroluminescence measurements. The external quantum efficiency of optimized light emitting device is evaluated. Light emitting field effect transistors are fabricated and a complete electrical and optical characterization is performed. A comparison between light emitting capacitor and light emitting field effect transistor is reported.

In the fourth and the fifth chapters, I report my study done on the erbium doped silicon nanocrystals based light emitting devices and optical cavities.

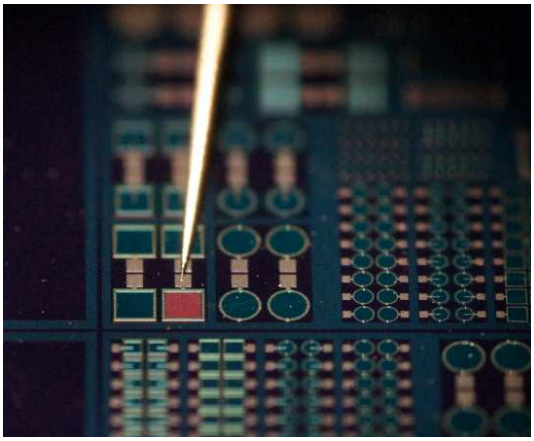
Chapter 4 discusses the initial work done on erbium doped silicon rich silicon dioxide based light emitting devices. The investigation of the opto-electrical properties of LEDs in direct current and alternate current regime are studied in order to understand the different injection mechanisms and the role of the silicon content and of the oxide barrier thickness in multilayered devices. The bipolar pulsed excitation in such devices is also discussed and I estimate the value of the energy transfer between the silicon nanocrystals and the erbium ions. Finally, the best active material is chosen in order to fabricate erbium doped silicon nanocrystals optical cavities.

Therefore, in chapter 5, I report all the study performed on the erbium doped silicon nanocrystals based optical cavities. Slot waveguides are described, from the design and the simulation, up to the fabrication and the electrical and optical characterization. I also discuss the infrared photoconductivity and the photovoltaic effects of the silicon nanoclusters in the waveguides. In the last part of the chapter, there is a description of the study performed on the erbium doped ring resonators. A complete experimental characterization, also with electro-optical pump-probe experiment, is reported. Some ground for the lack of the active functions are presented and discussed in order to delineate a path for the fabrication of an optical amplifier, by means of electrical pumping.

Finally, in chapter 6, I present the conclusions of all the work and I discuss future directions for research in silicon based light emitting devices and I report a brief outlook for silicon nanocrystals based devices in silicon photonics.

Chapter 2

Silicon Nanocrystals Based Light Emitting Devices fabricated by FBK



Visible light emission from a Si-NCs based LED. The devices have been fabricated at the FBK in Trento.

In this chapter, silicon rich silicon oxide based light emitting devices, fabricated at the Bruno Kessler Foundation (FBK) in Trento, within the INTEL project, are presented. After a brief introduction on the project, the sample layout and the active material splitting are here described. In particular, this study is focalized on the latest two runs of the project, Run 2C and Run 3. After that, I will deal with the electrical and the optical characterization. Electroluminescence study, time resolved measurements, with a detailed analysis, and power efficiency estimation are also reported.

2.1 The INTEL project

The project “Novel Scheme for a Silicon nanocrystals based LED” has been carried out by the MicroTechnologies Laboratory of the FBK and the Nanoscience Laboratory of the Department of Physics of UniTN, in collaboration with the INTEL Corporation. The project ended in 2008. The project produced different runs, each one fabricated to improve the electroluminescence (EL) and the power efficiency of the devices with respect to the previous ones. At the end of the project, light emitting diodes with power efficiency of 0.17 % have been realized. My study, carried out from April 2013 – five years after the end of the project – will be focalized on the latest two runs, Run 2C and Run 3 and it has the goal to understand some still open issues, related to the differences on the I-V characteristics and on the time resolved electroluminescence measurements. The study of the power efficiency will be presented here, but the main objective of this study is the understanding of the different performances between the two different runs. These two runs are presented at the beginning of this chapter. The batch of Run 2C consists of 17 wafers, while Run 3 includes 25 wafers with different active layer stacks. For an appropriate comparison, only Wafer 10 of Run 2C and Wafer 13 of Run 3 will be considered because they have the same active layer, but different structure and layout. Moreover, Wafer 16 and Wafer 17 of Run 3 will be discussed in order to figure out the kind of charge injection occurring into the studied devices.

2.2 Sample layout and active material splitting

All the light emitting devices (LEDs) realized within the project have a metal oxide semiconductor (MOS) structure on p-type silicon substrate with a sequence of silicon rich silicon oxide and silicon dioxide layers as gate dielectric. These layers have been grown by plasma enhanced chemical vapour deposition (PECVD).

2.2.1 Run 2C

In Wafer10 of Run2C the active structure has an expected total thickness of 32 nm. The substrate is p-type (boron doped) Si with 12 - 18 Ω·cm resistivity. The gate is formed by 100 nm-thick layer of n-type in-situ phosphorus doped polycrystalline silicon (poly-Si) with resistivity around 10^{-3} Ω·cm. The poly-Si is covered by a 50 nm-thick Si_3N_4 antireflective coating deposited by low-pressure chemical vapor deposition (LPCVD) to improve the light extraction. A 120 nm thick SiO_2 layer (TEOS) protects the

active layer. Local oxidation of silicon (LOCOS) was performed at 1150 °C for 30 min to both grow a 500-nm thick field oxide (for active area isolation) and decompose the SRO into the Si-NCs and the SiO_2 in the gate dielectric. By sputtering at 200 °C, a 500 nm-thick layer of Aluminum (Si 1%) was deposited on back of the wafer and Al (1% Si) was also used to connect the gate area with the bonding pad. The devices were additionally electrically isolated by a channel stop obtained by boron implantation in p-type substrate. For a detailed description of fabrication process of Run2C see the reference [39]. All the layer thicknesses are nominal values (based on previous careful characterization of the deposition rates), which were controlled by both profilometry and variable angle spectroscopic ellipsometry performed on previous batches of monitor wafers. A schematic cross section of a light emitting device (LED) structure of Wafer10 of Run2C is shown in Figure 2.1. According with the results obtained for the former runs an increment of the poly-Si gate thickness from 15 nm to 100 nm was involved in realizing Run2. In fact, a very thin poly-Si layer might cause spiking of Al, which might contact directly the silicon rich oxide (SRO) layers or/and result in a large increase of the resistivity of the poly-layer hindering the uniform distribution of the carriers in the poly-Si gate. Three levels of photolithographic mask were used within the process for realizing Run2C wafers. In Figure 2.2 right-hand side, the masks are shown in three different colors: violet, light green and dark green. Three blocks of photolithography checker, shown in LED block right hand side, has been also provided. Left-hand side, a whole wafer with the 13 dies (depicted in bluish green) containing the devices of interest is represented. In addition, the figure indicates also the labeling system applied for identifying every single structure on a wafer.

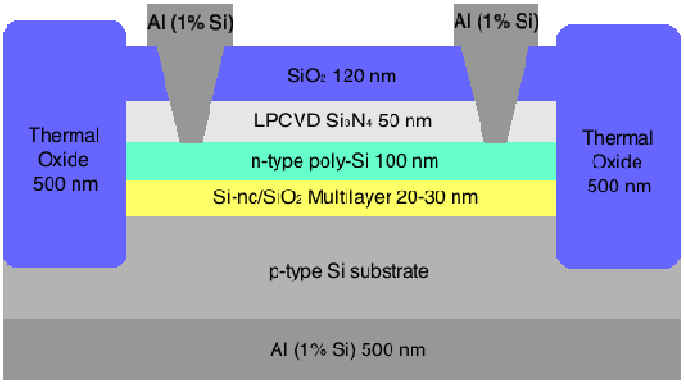


Figure 2.1. Simplified and not to scale drawing of the cross-section of the structures realized in Run2C.

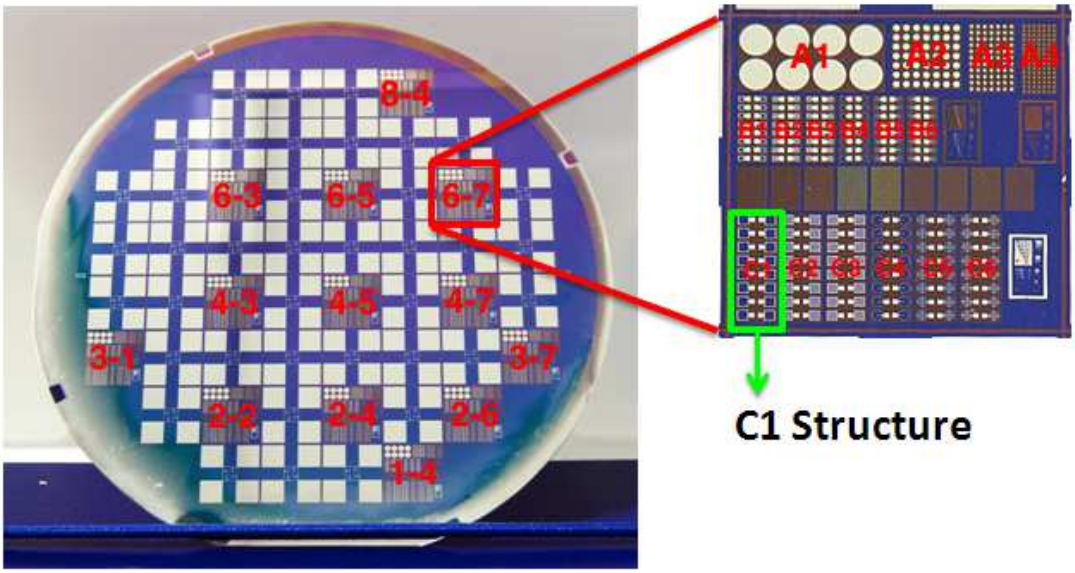


Figure 2.2. Scheme of the wafer layout used for Run2C. The devices of interest for this work are situated in the 13 red labeled areas. The labeling system applied to identify every type of structures on the wafer is shown in the right top.

2.2.2 Run 3

The aims of Run3 are to remove metal contact from light emitting region to avoid spiking and to reduce the thermal treatment of the Si-NCs formation simplifying the structure and the fabrication process. In the previous runs, silicon nitride and SiO_2 layers have been deposited after SRO and poly-Si in sequence, in order to increase the light extraction and to protect the active layer during the process. However, those depositions introduced extra heat treatment and consequently influenced the formation of the silicon quantum dots, which has been noticed by the weakening of Si-NCs photoluminescence signal after the device processing. On the other hand, having metal contact on the top of active region can cause spiking through poly-Si into the active material resulting in defect formation and non-uniformed carrier injection. To solve these problems, new structure has been designed (see Figure 2.3). The device structure is a MOS capacitor where alternating stoichiometric SiO_2 and SRO layers with large Si excess, grown by PECVD, is used as the gate oxide. In this work Wafer13, Wafer16 and Wafer17 of Run3 are detailed. The nominal thickness of SRO/SiO_2 multilayer (ML) is 32 nm for Wafer 13 and 29 nm for Wafer 16 and Wafer 17. The substrate is a p-type Si layer. A 500 nm-thick oxide layer, grown by thermal oxidation at 1050 °C for 60 min, was etched to confine the device active area. The 120 nm-thick poly-Si gate layer was in-situ phosphorus doped during LPCVD deposition (resistivity of around 10^{-3} Ω·cm). Silicon nanocrystals in

Wafer 13 were formed by annealing the ML at 1150 °C for 30 min and 1000 °C for 60 min in nitrogen. In Wafer16 and Wafer17 only a single annealing at 1150 °C for 30 min in N_2 was performed. In addition, up to 2 µm of Si were etched away from the backside of all the wafers to remove the doping inversion layer: this inversion layer is a result of dopant diffusion from n-type poly-Si to silicon substrate during the annealing. Aluminum (1% Si) is used to connect the gate area with the bonding pad and is also deposited (500 nm-thick layer) on back of the wafers by sputtering at 200 °C. The actual thicknesses of the individual layers within the ML stack were somewhat smaller than the nominal thickness values. This is due to a delay in plasma injection during the plasma-enhanced chemical vapor deposition (PECVD) growth and interdiffusion at the ML interfaces during the high temperature annealing. The total active layer thickness is found to decrease of about 30% of its nominal value.

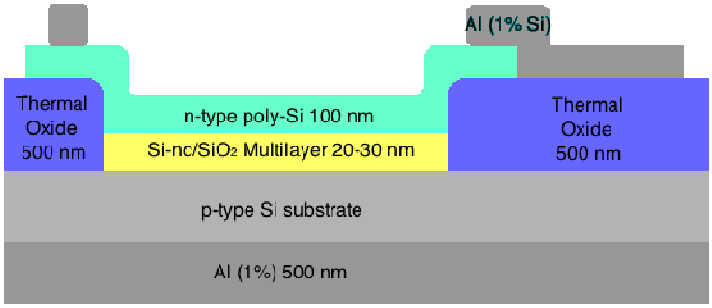


Figure 2.3. Cross-sectional sketch of Run3 layout (not to scale).

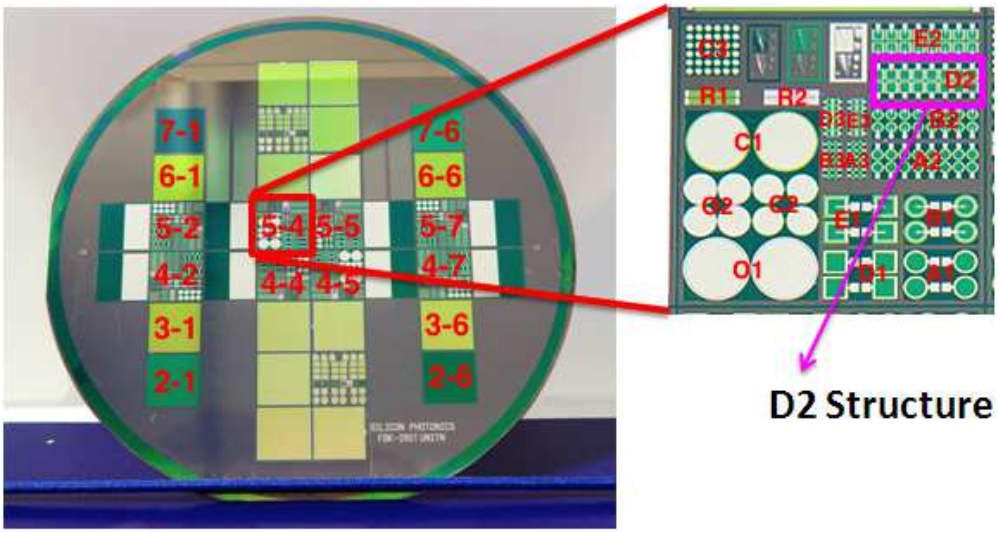


Figure 2.4. Scheme of wafer layout used for Run3. The labeling system applied to identify every single device of the wafer is shown in the right top.

As shown in Figure 2.4 left hand side, three levels of mask have been used in Run3. The first mask was used to define the device area (in blue color), which means field oxide has been patterned and the active region has been opened for SRO deposition. The second photolithography was applied after SRO and Poly-Si deposition. The purpose of the second photolithography was to leave SRO and poly-Si (in pink) only covering active region. Finally, Aluminum was deposited and patterned by the third mask as metal contact (in green). Similar to the previous layout, three blocks of photolithography checker were also provided, shown in LED block right hand side. Different MOS LED structures and test structures, such as capacitors and resistors, were designed for reference and test measurements. As shown in the right of Figure 2.4, the whole wafer is divided into 10 mm by 10 mm dies. Literally, the method of device labeling is illustrated in Figure 2.4 right top. In this new layout, plenty of areas is preserved for materials characterization. Besides these areas for spectroscopy measurement, some capacitors and resistors are designed for electrical characterization inside the LED blocks. LED block O1 and O2 are field oxide capacitors used to characterize the quality of thermal oxide and estimate the substrate doping. C1, C2 and C3 are MOS capacitors with SRO instead of SiO_2 to study the transport in the SRO film. Poly-Si and metal wire resistors are also provided in LED blocks R1 and R2 to determine the resistivity of the electrodes. Figure 2.5 shows pictures of fabricated wafers of both the runs.

Finally, the differences in the fabrication process between Run 2C and Run 3 can be summarized as following:

- ✓ Run 3 has the displacement of the metal contact from the active region and of two layers on top of the active layer material in order to avoid spiking;
- ✓ The annealing treatment of the two different runs are different;
- ✓ In the Run 3 process, up to 2 µm of silicon was etched away from the backside of all the wafers, in order to remove the doping inversion layer. This inversion layer is a result of dopant diffusion from n^+-Poly to silicon substrate during the annealing. The thickness of the inversion layer was obtained from simulation.

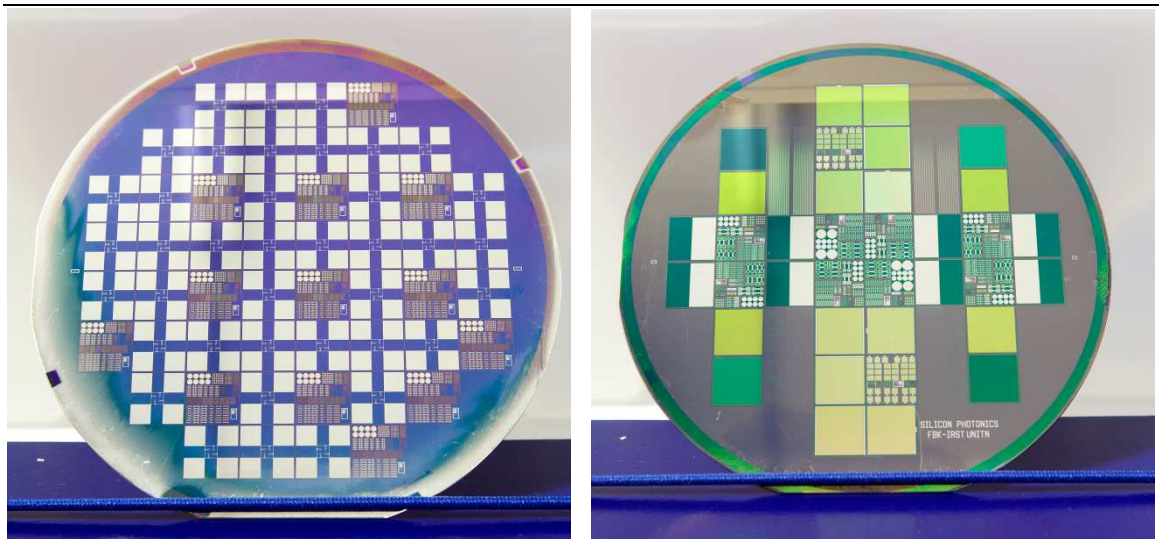


Figure 2.5. Photographs of fabricated wafers of Run 2C **(left)** and Run 3 **(right)**, respectively.

2.2.3 Active material splitting

A multilayer approach in the LEDs active material allows the independent control of Si-NCs size and density. Upon annealing at a high temperature, the thickness of non stoichiometric SRO in the ML structure confines the nanocrystals size, while the excess silicon content of the SRO layer determines the quantum dots density. The pair of SiO_2 and SRO layers forms the ML period.

Label	Nominal thickness*	SRO layers	SiO_2 layer thickness (nm)	SRO layer thickness (nm)	Annealing treatment
Wafer 10 Run 2C	2 nm SiO_2/ 4 nm SRO	5	1.5 ± 0.1	3.1 ± 0.1	1150 °C 30 min
Wafer 13 Run 3	2 nm SiO_2/ 4 nm SRO	5	1.8 ± 0.1	3.1 ± 0.1	1150 °C 30 min; 1000 °C 60 min
Wafer 16 Run 3	2 nm SiO_2/ 3 nm SRO + 4 nm SiO_2 at top	5	1.8 ± 0.1	2.0 ± 0.1	1150 °C 30 min
Wafer 17 Run 3	2 nm SiO_2/ 3 nm SRO + 4 nm SiO_2 at bottom	5	1.8 ± 0.1	2.0 ± 0.1	1150 °C 30 min

Table 2.1. Active layer composition for the samples under study. The color code used to distinguish the four wafers will be repeated in all the plots of this chapter.
(*) The nominal thickness is referring to the nominal thickness of a single layer.

All the studied structures present five periods, resulting in a gate dielectric thickness of around 20-30 nm to achieve measurable currents at rather low voltages. Table 2.1 gives all the details about the samples under study. Figure 2.6 shows a high resolution TEM image of the Wafer 10 of Run 2C. The analysis confirms the presence of the multilayer structure and the formation of the silicon nanocrystals.

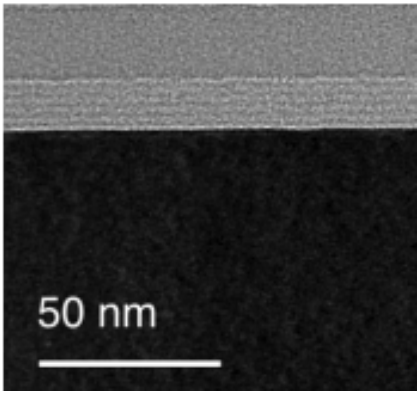


Figure 2.6. TEM image of W10 – Run 2C.

For Run3 devices, instead, three different structures will be analyzed (see Figure 2.7). Wafer 13 has 5 ML periods of nominal 2 nm SiO_2/4 nm SRO with 2 nm-thick oxide facing both the top gate and the bottom substrate. Wafer16 and Wafer 17 have five ML periods of 2 nm SiO_2/3 nm SRO, the first with 2 nm-thick oxide at the top and 4 nm-thick at the bottom of the ML, which serves as a tunneling barrier for holes, and the second with 2 nm-thick oxide at the bottom, and 4 nm-thick oxide at the top of the ML, serving as tunneling barrier for injected electrons. The use of electron or hole barriers makes it possible to distinguish the case of electrons or holes injection.

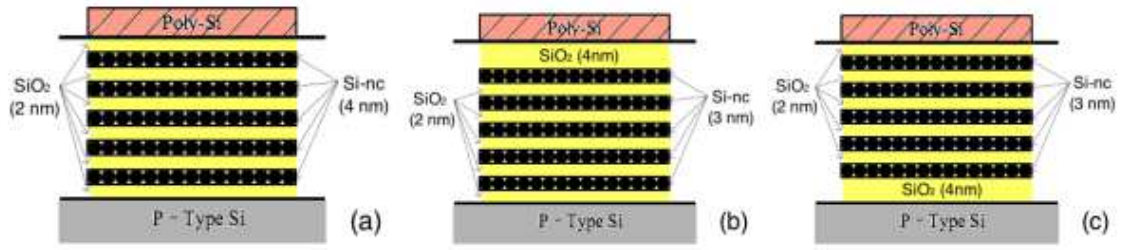


Figure 2.7. Drawing of the active layer stacksfor Wafer13 **(a)**, Wafer16 **(b)** and Wafer17 **(c)** of Run3 devices. Silicon nanocrystals are represented by black dots, while the silicon dioxide matrix is the yellow background.

2.3 Experimental characterization

2.3.1 I-Vs and C-Vs measurements

A first set of reliability tests has been performed on the wafers studied in this work. In fact, several environmental factors can affect the LEDs during the five years that passed after the production. These measurements gave an exhaustive proof that both the Wafer10 of Run2C and the Wafer13, 16 and 17 of Run3 could be used for further tests and for the understanding of the different performances of these two runs.

The I-V characteristics of Wafer10 - Run2C and Wafer13 – Run3 are shown in Figure 2.8. Note that the current is here reported as absolute value, in order to be able to use the logarithmic units. Actually, when we apply a forward bias the current is negative (i.e. from the top contact to the chuck); while in reverse bias the current is positive (i.e. from the chuck to the top contact). This behavior is verified for all the analyzed devices. These plots are obtained by averaging ten single sweeps. The error bars are computed by standard deviation. For every measurement, the devices are chosen among the never tested one, with the same design and active area, in order to compare directly the current values. In all the measurements, the chuck is grounded, while the voltage bias is applied on the metallic contact on top of the wafer. Therefore a negative bias to the LED means forward bias condition. Vice versa, with a positive bias applied to the gate, we are in the reverse bias condition. To study the LED reliability, the I-V curves recorded in 2008 are also reported in the figure [40].

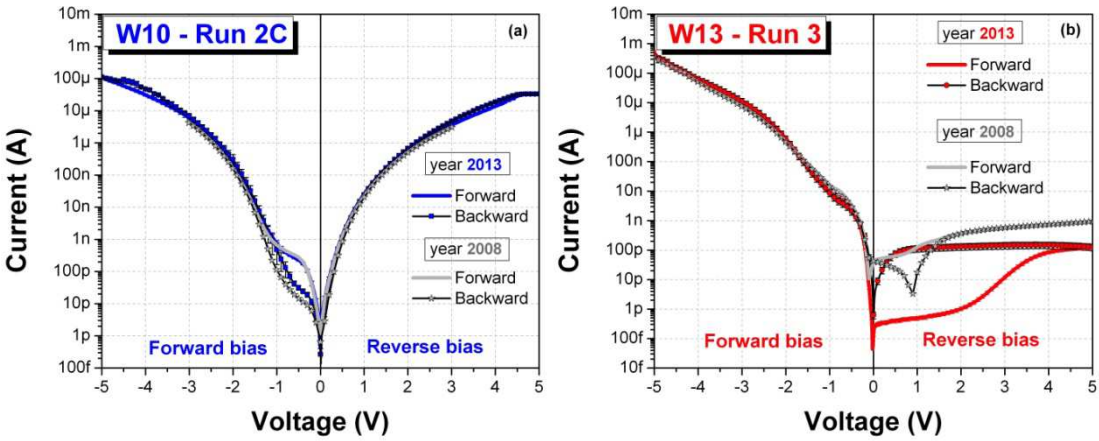


Figure 2.8. I-V characteristics of the multilayered LEDs of Wafer10 - Run2C **(a)**, Wafer13 – Run3 **(b)**. Error bars represent the standard deviation of the plotted data but are covered by symbols because of the high reproducibility.

Figure 2.8 (a) shows that Wafer10 devices behave like in 2008. This means that the fabrication process used for realizing Run2C allows making very reliable structures. The I-V characteristic presents almost the same current in forward and reverse bias. According to what has been discussed in Chapter 1 this is typical of a MOS device with heavily doped p-side (see Figure 1.15) or of a device where the oxide barrier is thick (see Figure 1.17).

For negative gate voltages (forward bias), three different current trends can be clearly distinguished in Figure 2.8 (a). From 0 V up to -1.1 V, the current increases weakly (up to electric fields of around 0.5 MV/cm). Then, a fast increment follows up to -3 V (1.2 MV/cm). For negative voltage bias larger than -3 V, the current increment slows down. In reverse bias the current increases with increasing the gate voltage, and at + 3V it takes the same values as the one observed in forward bias. Therefore, the I-V characteristic is not rectifying. The symmetry of the I-V characteristic is a consequence of the injection mechanism, for which we have bipolar injection in forward bias, while we have unipolar injection in the reverse bias. The oxide quality is such that, in reverse condition, an inversion layer is formed in the junction between the active layer and the p-type doped substrate. A simplified mechanism of what is occurring is given in Figure 2.9.

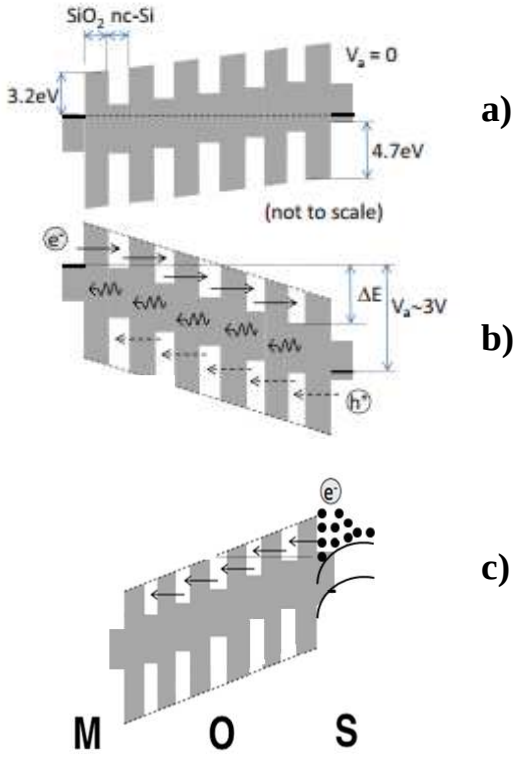


Figure 2.9. Schematic band diagram of an ideal multilayer structure under **(a)** no bias, **(b)** forward bias and **(c)** reverse bias.

In forward bias, both electron and hole tunnel into the active layer (see Figure 2.9.b). In reverse bias condition, an inversion layer is formed in the junction between the active layer and the p-type doped substrate (see Figure 2.9.c). In this case, there is only unipolar injection of electrons from the backside of the gate dielectric. The straight arrows indicate the tunneling in the multilayer structure. The electroluminescence – indicates as emission of photons in Figure 2.9.b – is expected only in the forward bias condition, because of the bipolar injection of electron and holes inside the active layer.

For low current injected or at low forward bias applied, a hysteresis loop is found in Wafer 10 devices, which extends to about -1.1 V under forward bias. The hysteresis originates from the charge accumulation within the SRO layer. Positive charges – injected from the substrate - are accumulated under negative forward bias. This causes a built-in potential that adds to the external bias. This explains the weak increment of current in the hysteresis region. The hysteresis width is associated with the density of trapped charges [41].

Figure 2.8 (b) shows the I-V characteristic for devices of Wafer13 Run3. On the plot also the sweeps performed in 2008 are shown. There is a good agreement between measurements in forward bias regime. The large forward bias current is due to tunneling mechanisms within the ML structure. On the contrary, in reverse bias there is a marked difference between the curves. The behavior of Wafer13 devices is very different from the one of Wafer 10 – Run 2C. The I-V characteristic of Wafer 13, in fact, is strongly rectifying. The reverse current is of the order of 10 pA, while in forward bias the current rises over 100 μA. This I-V characteristic resembles the one of a p-n junction diode, demonstrating an exponential dependence at low forward voltages and the effect of a series resistance at high forward voltages. The behavior for this new type of Si-NCs MOS LED resembles the behavior a MOS tunnel diode with leaky oxide or thin oxide layer. In fact, when the oxide is leaky, no inversion layer is formed at the oxide-p-type doped substrate and the I-V characteristics yield rectification (see Figure 1.17). Therefore, it is not possible the injection of electrons from the backside of the gate dielectric.

We believe that the differences between the two I-V characteristics have to be researched in a different quality of the oxide, where in one case it is well insulating and in the second it leaks through. The critical interface for the injection mechanism in reverse bias condition is the one between the multilayer and the device substrate. In order to better understand the injection mechanism into our devices, we have studied also W16 and W17, which have a thicker electron or hole barriers, respectively.

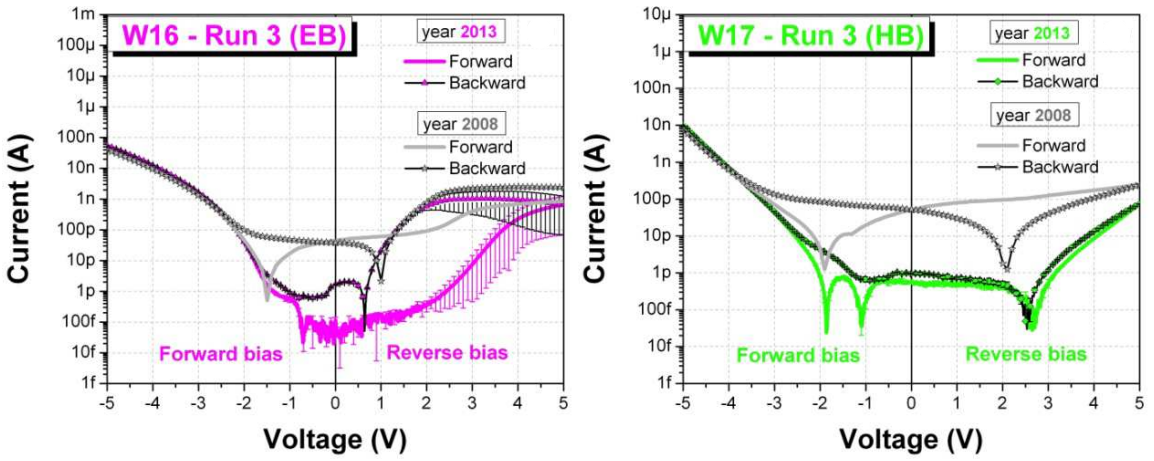


Figure 2.10. I-V characteristics of the multilayered LEDs of Wafer16 **(left)** and Wafer17 **(right)** - Run3. Error bars represent the standard deviation of the plotted data but, a part for Wafer 16, are covered by symbols because of the high reproducibility.

Figure 2.10 show the I-V characteristics for Wafer 16 and Wafer 17 devices respectively. These LEDs share the same ML structure but the former has a 4 nm thick SiO_2 layer at the top of the active region and the last has a 4 nm thick SiO_2 layer at the bottom of the active region. These additional oxide layers result in a current reduction of about four orders of magnitude when the LEDs are forward biased. In fact, a 4 nm thick SiO_2 layer constitute a large barrier for electron or hole tunneling.

The new measurements performed on Wafer 16 show a large hysteresis region in reverse bias (negative charges are accumulated), as happens for Wafer13 devices with positive gate voltage applied. Both Wafer16 and Wafer17 present a behavior in agreement with the one obtained five years ago in forward bias, but they present a bigger hysteresis in reserve bias condition, which shows a degradation of the oxide with the formation of more trap states. It is interesting to notice that, in forward bias, the currents start to flow at different applied voltage. For negative voltages larger than -2.5 V (for W16) and larger than – 3.8 V (for W17), the current flows into the devices. These voltage values give a hint on the barrier height for electrons (W16) or holes (W17) tunneling in an F-N mechanism. Note also that, a part the region between – 3V to + 3V, the I-V characteristics of W17 starts to get symmetric. This is an hint on the role of the thick oxide barrier in permitting the formation of the inversion layer and, therefore, of the injection of hot electrons through the active layer. In a way, W17 resembles the situation found for W10 – Run 2C and schematically shown in Figure 2.9.

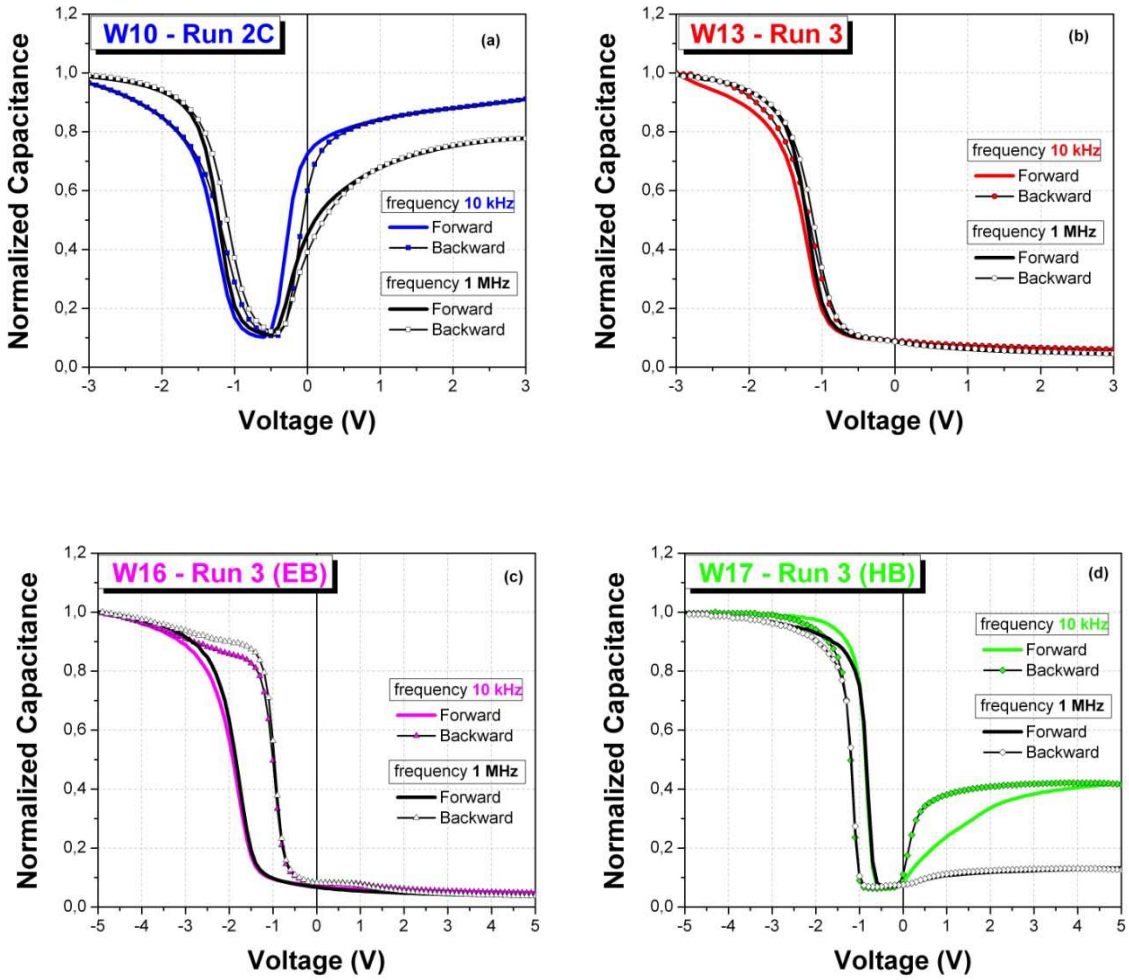


Figure 2.11. C-V characteristics of the multilayered LEDs of Wafer10 - Run2C **(a)**, Wafer13 **(b)**, Wafer16 **(c)** and Wafer17 **(d)** – Run3. The small signal frequency is chosen to be 10 kHz and 1 MHz.

Figure 2.11 shows the high frequency C-V characteristics recorded for Wafer10 - Run2C and Wafer13, Wafer16 and Wafer17 - Run3 devices. These measurements are performed in order to clarify the presence of charge trapping at interfaces. The difference between the C-V sweeps obtained for Wafer10 and Wafer13 devices (Figure 2.9 (a) and (b)) is due to the different capability of the charge density in the inversion layer to follow the ac variation of the applied gate voltage. Wafer13 is not able to follow the ac variation of the applied gate voltage. This difference between the two wafers is the same observed also for the I-V characteristics. In the reverse bias condition, there is no current flowing in W13 and there are no charges accumulated. This observation agrees with the previous considerations done observing the I-V characteristics.

In the case of Wafer16 and Wafer17 devices (see Figures 2.9 (c) and (d)) the C-V curves at the highest frequency have a step-like shape. This behaviour might be attributed to the mechanism of charge trapping at the Si NCs/SiO_2 interface or near the interface region. The hysteresis is counterclockwise, with respect to the voltage scanning direction, in Wafer 16 and this is the indication of a net positive charge accumulated close to the ML/barrier interface [41]. In contrast, the C-V hysteresis is clockwise for Wafer 17, meaning the trapping of net negative charge at the ML/barrier interface. Summarizing, in the case of W16 the trapped charge is positive, while in the case of W17 the trapped charge is negative. The amount of the net trapped charge in Wafer16 is larger than in Wafer17, as shown by the difference in the C-V hysteresis width. This is supported by the tunneling mobility and the barrier height that are larger for holes than for electrons. In fact, we do not have to forget that the potential barrier height in Si/SiO_2 system is 3.2 V for conduction electrons and 4.7 V for holes in valence band.

Summarizing, the C-V characteristics confirm the presence of the inversion layer both in Wafer 10 – Run2C and in Wafer 17 – Run3. We can conclude that the main differences between W10 – Run 2C and W13 – Run 3 is the different quality of the oxide, where in the first sample it is well insulating, while in the second one it leaks through. Wafer 17 supports our guess of the presence of the inversion layer in W10 – Run 2C, because they behave in a similar way and it has a thick oxide on the bottom of the active layer.

2.3.2 Electroluminescence spectra

In this section, spectral analysis of electroluminescence (EL) will be presented. It has to be underlined that the electroluminescence signal can be detected only in the forward bias regime, i.e. a negative voltage applied to the gate and the chuck grounded. In the Run 2C we do see EL only in forward bias, even if the I-V curve presents a not-rectifying behavior. This observation is explained by the fact that we cannot efficiently inject holes from the metal, and so the electrons injected from the back cannot recombine. In the Run 3 devices we do not have any current flowing in reverse condition (see Figure 2.8) and, thus, no electroluminescence signal.

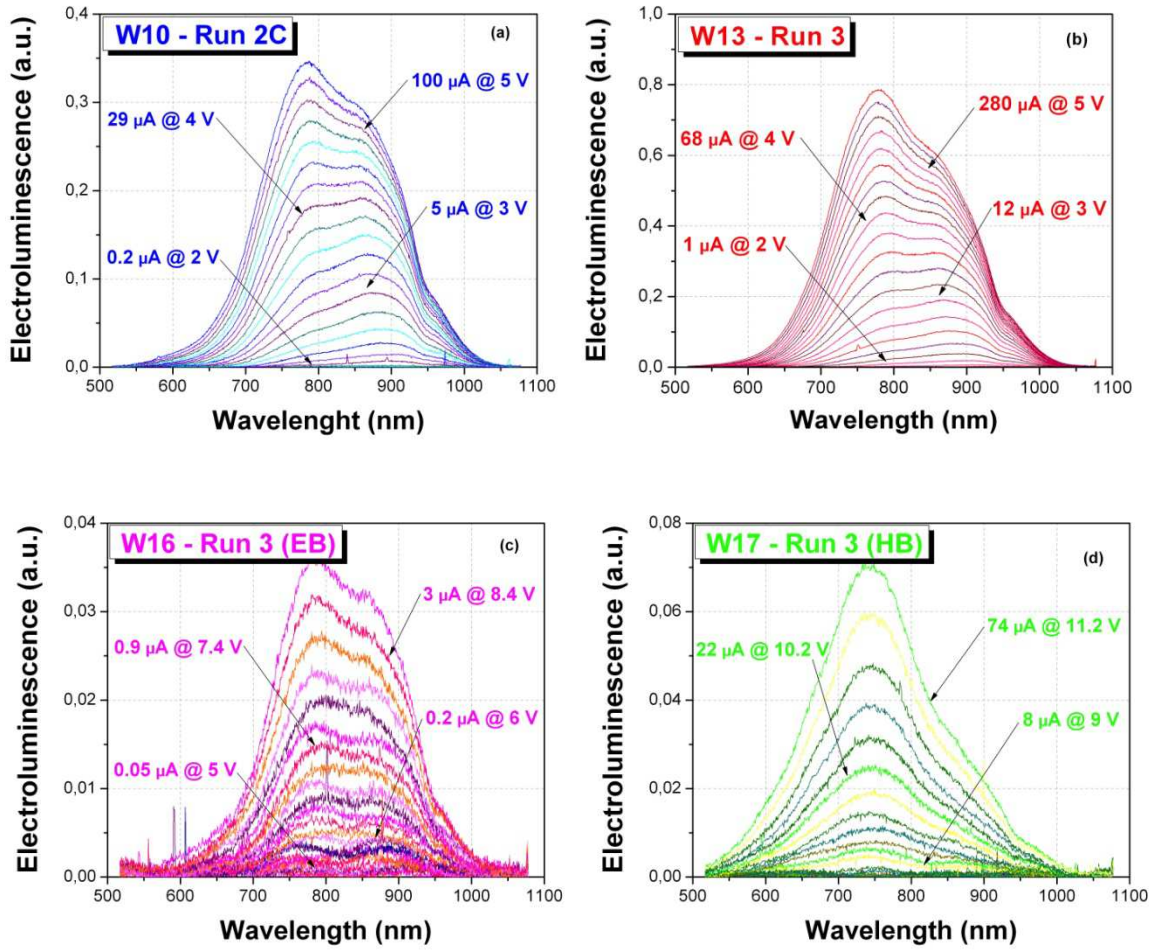


Figure 2.12. EL spectra of Wafer 10 **(a)**, Wafer 13 **(b)**, Wafer 16 **(c)** and Wafer 17 **(d)** for different applied voltages. The values of electroluminescence are reported in arbitrary units and are useful for a comparison between different devices.

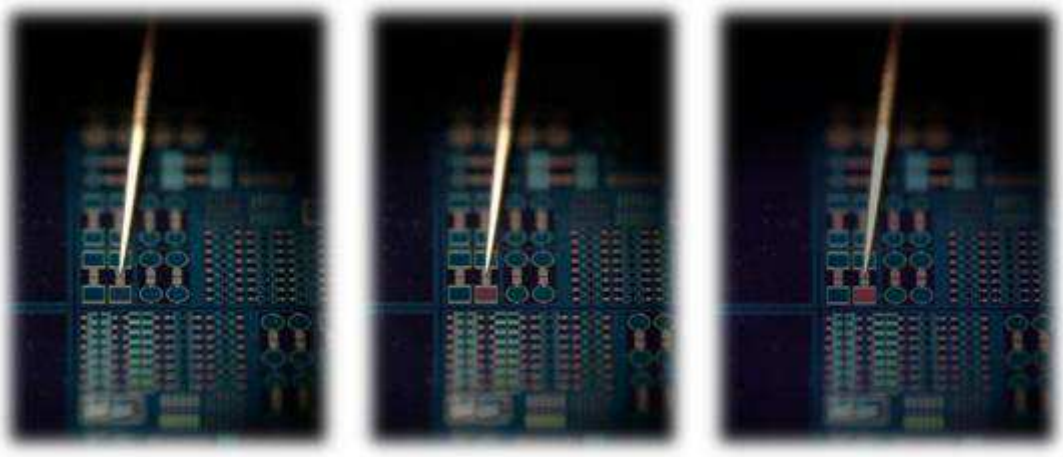


Figure 2.13. Pictures of the EL from Si-NCs based LED on Wafer 13 – Run3. The voltages applied to the device are 3V, 4V and 5V, *from left to right*.

Since only the forward bias region is significant for the EL measurements, the negative voltages (with respect to the grounded substrate) applied to the gate are simply reported in absolute value. The EL spectra of Wafer 10 – Run 2C and Wafer 13, Wafer16 and Wafer17 - Run3, collected at different applied voltages, are shown in Figure 2.12. EL intensity almost doubles in Wafer 13 (Figure 2.12 (a)) with respect to Wafer 10 (Figure 2.12 (b)) at the same applied voltage. The EL spectra are broadened and extend to short wavelengths. The spectra from SRO 4 nm/SiO_2 2 nm devices peak at different wavelengths depending on the gate voltage. The position of the EL peak is slightly shifting towards shorter wavelengths with increasing bias. In particular, a peak around 900 nm is evident below 3 V, while a peak at about 800 nm rises at higher voltages. The origin of this behavior lays in the different mechanisms that generate luminescence into the Si-NCs. The most probable path for electroluminescence involves both exciton recombination in the Si-NCs and defect-assisted recombination, where luminescence is the result of the recombination of carriers trapped at radiative recombination centers that form at the interface between Si-NCs and the dielectric or even in the dielectric itself [43]. One possible candidate for these centers is the silanone bond that is formed by double Si-O bonds [44]. The light emission at low voltages (emission peaked at ~ 900 nm) is mainly due to the bipolar (electrons and holes) injection via the direct tunneling mechanism. In fact, EL emission occurs at voltages lower than 3.1 or 4.7 V, which are the values corresponding to the height of the energy barriers at the silicon oxide interface for electrons or holes, respectively. The large bandwidth of the emission is a consequence of an inhomogeneous broadening due to the size dispersion of Si-NCs. At higher voltages, Fowler–Nordheim tunneling of hot electrons into the oxide conduction band occurs: EL is then produced by recombination of electron-hole pairs in the Si-NCs which have been excited by the current of hot electrons via an impact excitation mechanism. The impact excitation mechanism is inefficient, and the hot electron injection damages the oxide. At high voltages applied the recombination occurs mainly through trapped carriers on radiative interface states (emission peaked at ~ 800 nm) [45].

In Wafer16 and Wafer17 devices (Figures 2.12 (c) and (d)) the oxide barriers block the injection of electrons and holes into the Si-NCs, respectively. Very weak electroluminescence emission is observed under high applied electric fields. The light emission is undetectable below 5 V for Wafer16 and below 9 V for Wafer17. EL spectra of Wafer16 and Wafer17 confirm the previous claims. Indeed, in the devices with the

electron barrier (EB), direct tunneling is prevented and the onset of Fowler-Nordheim tunneling is responsible for emission around 900 nm. On the other side, in the devices with hole barrier (HB), emission due to defect-assisted recombination (at shorter wavelengths) prevails.

Figure 2.13 shows the visible EL from a device of Wafer 13 - Run 3. The three pictures are showing the red color, typical of the Si-NCs emission, as a function of the applied voltage. The photographs have been done on the device with large emitting area.

Figure 2.14 shows the integrated EL as a function of the applied voltage, in order to see the different injection mechanisms. The values are obtained by integrating the whole areas of the EL spectra at different applied voltages/injected currents. In Figure 2.14 (a) and (b) the integrated EL dependence on the applied voltage shows two clearly distinct regions: a region of low voltages, when the EL increases rapidly, and a region of high voltage, when it increases more slowly. The first region is attributed to the bipolar (electrons and holes) injection into silicon nanocrystals under the direct tunneling regime [46]. The direct tunneling is the dominant charge transport mechanism in structures with thin (2 nm) oxide layers. The second region is instead due to the dominant unipolar (electron) injection into silicon oxide conduction band by the Fowler-Nordheim tunneling. The transition between these two regions occurs at the applied voltage of about 3 V, which corresponds to the energy barrier height for electrons at the Si/SiO_2 interface.

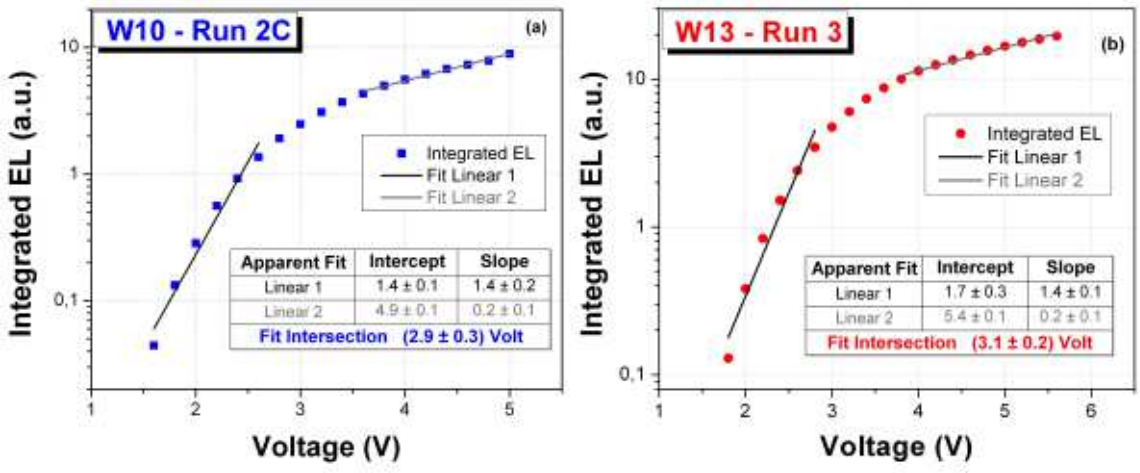


Figure 2.14. Integrated EL as a function of the applied voltage for the ML device of Wafer 10 – Run 2C **(a)** and Wafer 13 – Run 3 **(b)**. The intersection between the two linear fits gives values around the 3 V. The first region is attributed to the bipolar injection into the Si-NCs, while in the second region the unipolar injection is the main excitation mechanism.

The Integrated EL as a function of the bias gate voltage has been also evaluated for Wafer16 and Wafer17, but it is not reported here. Because of the 4 nm barrier of silicon dioxide in the active layer, no EL is present below 5 V and 9 V respectively. Indeed, the direct tunneling mechanism is prevented in these devices because of the oxide barriers. In Wafer16 devices, when voltages higher than 5 V are applied (i. e. under the Fowler-Nordheim tunneling regime), the light emission is attributed to impact ionization of electrons injected from the top electrode into the Si-NCs. Instead, in Wafer17 devices the holes are more difficult to inject than the electrons and the electroluminescence is principally due to recombination of carriers trapped at radiative recombination centers [47]. Figure 2.15 shows, in the same plot, the integrated EL obtained in Wafer 10 and in Wafer 13 devices as a function of the current density. The slope of the integrated EL vs. the current density characteristic is related to the internal quantum efficiency. The results are reported in the plot. It has to be underlined that it is a log-log plot, and so the slope of the apparent fit tell us if the relationship between these two parameters is linear, sublinear or superlinear. In our case, both the devices share the same slope of (0.9 ± 0.1), for applied voltages below 3 V. This means that, in this region – which is the region in which the bipolar tunneling occurs – the EL increases linearly with the injected current. When the applied voltage rises over 3 V, a smaller slope is evident. The difference in the slope value might be attributed to the hot carrier injection that takes place under the Fowler-Nordheim tunneling regime, leading to lower efficiency than in direct tunneling regime.

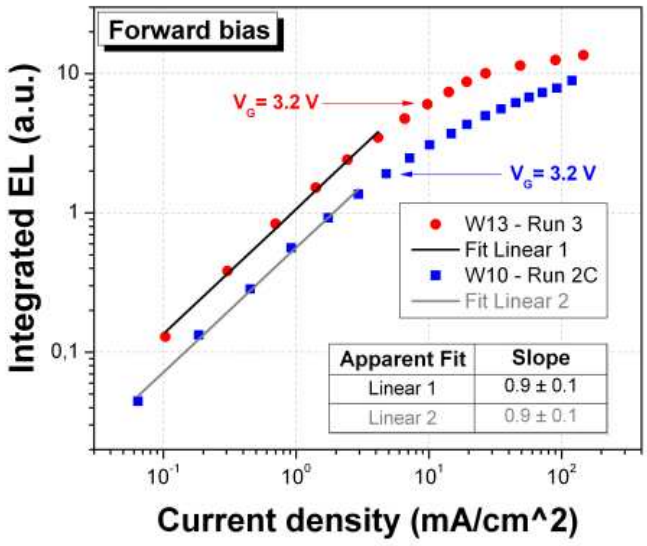


Figure 2.15. Integrated EL as a function of the current density. The apparent linear fit is calculated for both the wafers in the region below the onset of the Fowler-Nordheim tunneling.

2.3.3 Time resolved electroluminescence

It was theoretically predicted [48] and experimentally demonstrated [49] that the EL of the silicon nanocrystals LEDs shows a peak when the supply voltage is swept abruptly from positive-to-negative values and vice versa. Walters et al. demonstrated the possibility to have sequential injection in LEDs, with electroluminescence overshoot peaks at the bias transition and, then, a lack of the emission under the DC electrical bias. After the gate bias is switched from a negative to a positive level, the emission pulse rises to a peak value and then begins to decay as the previously injected holes are consumed by electrons in exciton formation and recombination. Some fraction of the exciton population may be formed by charge carriers that migrate between nanocrystals in the ensemble rather than by the direct carrier injection. When the EL signal is no longer observed, there are no holes left in the nanocrystal ensemble to form excitons. However, electrons continue to be injected into the nanocrystal array due to the positive bias gate, resulting in each nanocrystal becoming recharged with an electron. When the gate voltage is switched back to a negative potential, holes enter the electron-charged nanocrystals, forming excitons, and there is another electroluminescence overshoot. Therefore, an alternating current pumping scheme allows to get information on the injection mechanisms in such devices. In this section, I present the measurements performed on all the wafers under study with an alternating current (AC) pumping scheme.

Figure 2.16 shows an example of the behavior of time resolved electroluminescence performed on Wafer 10 – Run2C. The dashed line represents the square waveform voltage applied in AC to the device (in this case the voltage is switched abruptly between - 3V and + 3V), while the blue plot represents the time resolved EL signal (y-axis on the left). The first observation is that we do have electroluminescence signal in forward bias, while there is no EL in the reverse bias regime. This agrees with what we found in the previous sections. In addition, every time we switch abruptly the polarization, we do see an electroluminescence overshoot. The presence or not of these EL overshoots and their explanation is the focus of this section.

Figure 2.17 shows in fact time resolved electroluminescence measurements performed both on Wafer 10 – Run2C and on Wafer 13 – Run3 in different AC regimes (reverse to forward regime, reverse to zero and zero to forward polarizations). As shown in the figure, there are several differences between these plots.

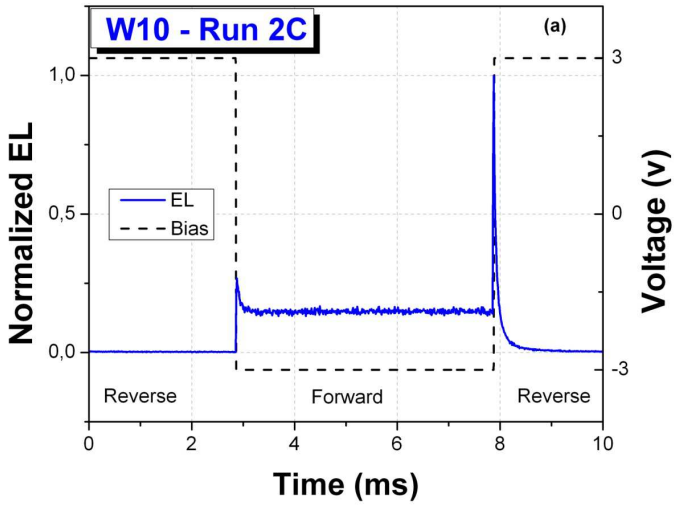


Figure 2.16. Example of time resolved electroluminescence measurement performed on W10 – Run 2C. The dashed line represents the square waveform voltage bias applied, while the blue line is the time resolved EL signal.

Figure 2.17.a shows the time resolved electroluminescence of W10 – Run 2C with a square waveform AC applied from -3 V and +3 V. The devices show EL peaks every time the sign of the gate bias is changed. Under a constant bias, the holes accumulate at the interface between the substrate and the multilayer (ML) gate, while the electrons accumulate at the interface between the top and the active material. When the bias is abruptly changed, electrons are injected into the hole-charged nanocrystals side and holes are injected into the electron-charged nanocrystals side, generating the two overshoots of the EL emission. The amplitude of the peaks is about four times larger for the forward-to-reverse bias transition than for the reverse-to-forward one. This asymmetry might be explained by the difference in electron and hole injection efficiencies from the n-type polycrystalline silicon gate and the p-type Si substrate. Indeed, the accumulation of holes in the multilayer is greater under forward than under reverse bias. The EL decay time is larger for the reverse-to-forward bias transitions (~ 60 µs) than for the forward-to-reverse transitions (~ 40 µs). Moreover, after reverse-to-forward bias transition, the EL peak emission decays to a non-zero EL signal. This constant EL signal under the forward bias is the direct current EL emission.

In Figure 2.17.b the reverse side of the driving square-form voltage signal is reduced to zero. When the bias is switched to -3 V, EL rises till the continuous emission regime. The constant EL signal under the forward bias is due to bipolar injection into the Si-NCs of electrons from the gate and holes from the substrate. When the supply voltage

is turned off, an EL overshoot occurs. Then, EL decays to zero. The created excitons remain inside the Si-NCs even after the voltage switches off. In this condition, the wave function overlap of each confined electron-hole pair is maximized and consequently the probability of radiative recombination is increased. The height of the EL peak is two times larger with respect to the continuous EL signal intensity. The EL overshoot could also be related to the presence of a current peak, probably due to the release of carriers accumulated in the device under steady state conditions, which are released when the external biasing voltage is switched off [50].

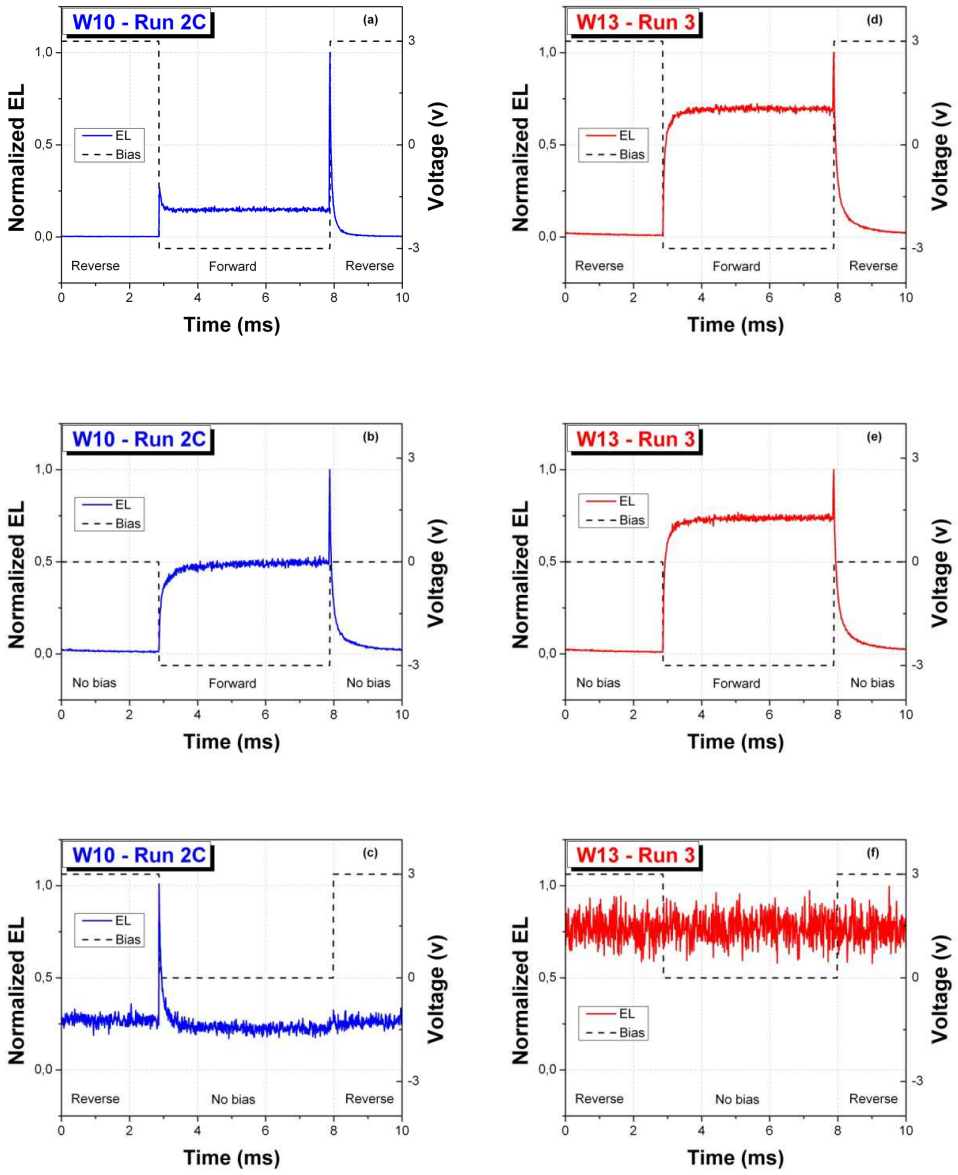


Figure 2.17. Time resolved plot of the AC driving square waveform voltage (dashed line) and resulting EL (colored solid line) of the Si-NCs LEDs of Wafer 10 – Run 2C **((a), (b), (c))**, and Wafer 13 – Run 3 **((d), (e), (f))**. Every single plot is normalized to the highest value recorded during the measurements. The frequency of the square waveforms is 100 Hz.

Figure 2.17.c supports the previous claims. In this case the forward side of the polarization signal is reduced to zero, in a way that we switch the voltage from reverse bias to zero and then to reverse bias again.

The EL peak occurs at the reverse-to-zero transition and its amplitude is very low (only four times larger than the background noise). Also in this case the presence of this overshoot is due to the "relaxation processes" (carrier trapped with Si-NCs tunnel towards nearest opposite-charged Si-NCs, leading to EL causing a reduction of the internal energy) and the low amplitude of the EL peak can be related to the low hole-injection efficiency under the reverse bias condition. Indeed, when the supply voltage is switched off, EL cannot be generated by external injection, because, in reserve bias condition, we can inject electrons from the substrate, but we cannot inject efficiently the holes from the top of the device.

For Wafer 13 – Run3 the time resolved electroluminescence measurements show different shapes.

Wafer 13 - Run3 devices show an EL peak only for forward-to-reverse transitions (see Figure 2.17.d). The absence of the EL peak for the reverse-to-forward transition is expected and it is due to the rectifying behavior shown in the I-V characteristic (see Figure 2.8). In fact, in reverse bias the formation of the electron inversion layer does not occur, as demonstrated by the C-V sweeps. The peak height is less than twice the constant EL signal amplitude and the decay time is about 100 µs. The comparison between this EL emission peak and that one shown in Figure 2.17.e, where negative pulsed bias is applied, suggest that the “relaxation process” is responsible for EL overshoots. When the square-form voltage signal is reverse-no bias (Figure 2.17.f), we show only background noise: this indicates that no EL is emitted by the Wafer13 devices. The results reported in Figure 2.17.f are not surprising because of the rectifyng behaviour of the current-voltage characteristic of the Wafer13 – Run3. In fact, it is impossible to inject current in the devices both in reserve bias and in the no bias conditions.

A simple model of what happens in these structures is reported in Figure 2.18. On the left of Figure 2.18, there are the band diagrams for the Wafer 10 – Run 2C in forward bias (top) and in reverse bias condition (bottom). In the forward bias condition, when both electrons and holes can be injected, they can recombine and emit the photon. In reverse bias condition, there is the possibility to inject only the electrons from the substrate. These electrons are injected in the hole-charged silicon nanocrystals (they are charged because of the previous polarization) and can recombine generating luminescence.

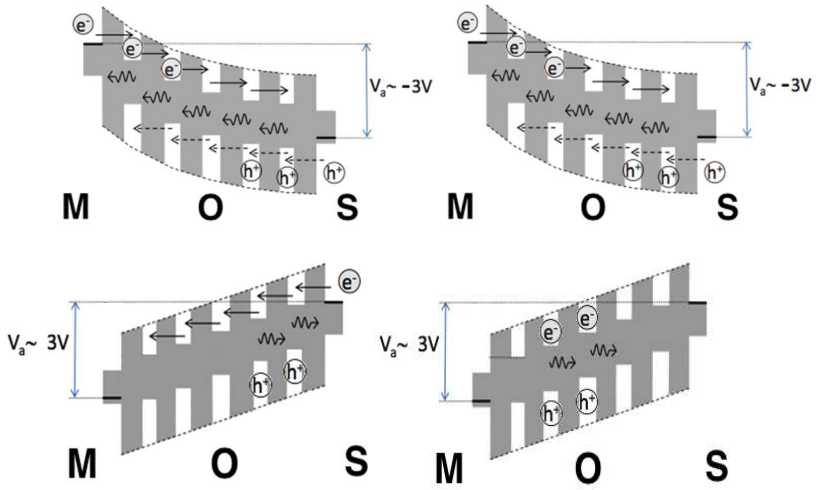


Figure 2.18. Schematic band diagram of an ideal ML structure under forward bias **(top)** and reverse bias **(reverse)** conditions. On the left, the model for W10 – Run 2C, on the right the model for W13 – Run3.

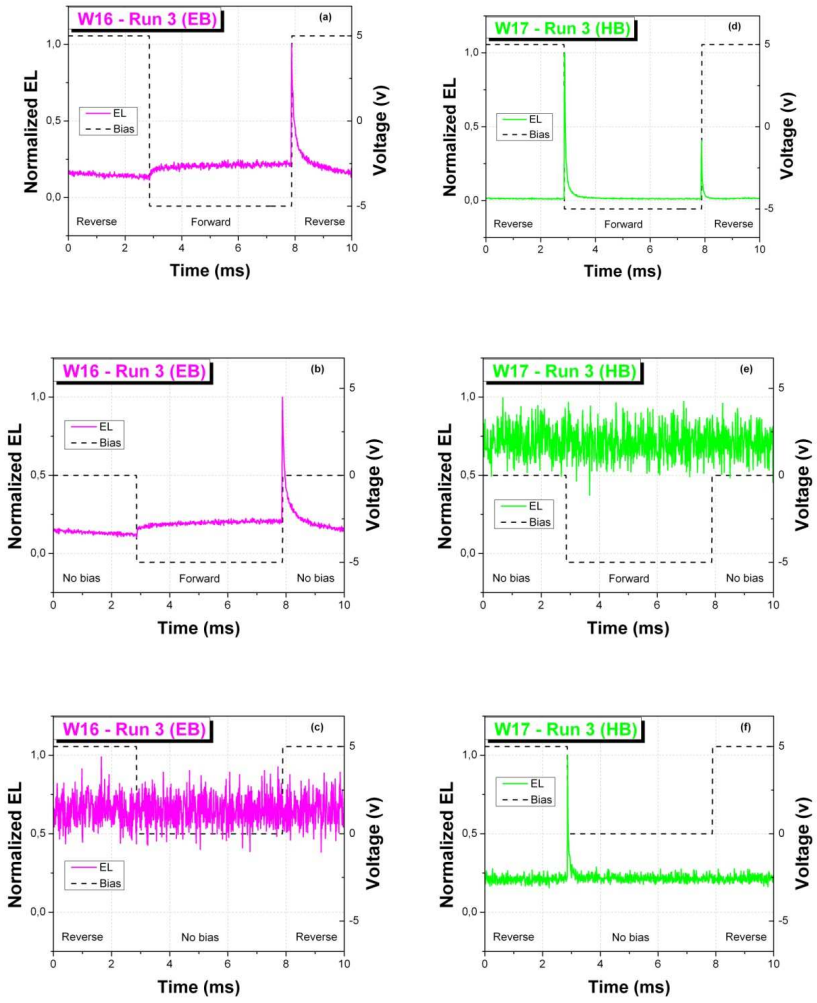


Figure 2.19. Time resolved plot of the alternating driving voltage (dashed line) and resulting electroluminescence (EL) (colored solid line) of the Si-NCs LEDs of Wafer 16 – Run 3 **((a), (b), (c))**, and Wafer 17 – Run 3 **((d), (e), (f))**. Every single plot is normalized to the highest value recorded during the measurements. The frequency of the square waveforms is 100 Hz.

On the right of Figure 2.18, there are the diagrams corresponding to Wafer 13 – Run 3. In this case, the situation in the forward bias configuration is similar to what discussed for Wafer 10 – Run 2C, but it is different in the reverse bias regime. In reverse bias, in fact, there is no injections of electrons from the substrate. This observation can be explained with the different quality of the oxide, as discussed in the previous sections. The time resolved electroluminescence measurements confirm our thesis.

Additional support to the previous reasoning is given by the time-resolved EL measurements performed on Wafer16 and Wafer17 - Run3. In order to obtain detectable EL signals, the bias amplitude is increased with respect to the previous measurements because of the presence of a 4nm-thick oxide layer at the top or at the bottom of the multilayer (ML). Figure 2.19.a shows a similarity of the behaviour of W16 with what obtainde for W13. All the three different plots of these two wafers present the same shapes. In such devices, the electron injection and the hole injection are efficient only in forward bias. The difference between these two samples is only that a large forward bias is needed to tunnel through the 4 nm oxide.

Wafer17 – Run 3 presents instead a 4 nm-thick oxide layer at the bottom of the ML, which block the hole injection under forward bias regime. The time resolved EL measurement of Wafer 17 show similar shapes of Wafer 10 – Run 2C. The only difference is reported in Figure 2.19.e, because of the absence of electroluminescence under forward bias, due to the high voltages required in order to have a detectable luminescence signal. Figure 2.19.d shows two well defined EL emission peaks every bias transition. In forward bias regime electrons are injected from the gate inside the ML but holes are blocked by the thick oxide layer at the bottom of the ML. No EL is detected under this condition. When the bias is abruptly changed, holes are injected into the electron-charged nanocrystals from the gate, bringing the peak of EL emission. At the reverse-to-forward bias transition a large amount of electrons is injected into hole-charged nanocrystals, causing the other large EL overshoot.

Summarizing, from the time resolved measurements we have found a similar behaviour between W16 and W13, and between W10 – Run2C and W17. The main important parameter needed to understand these devices is the injection mechanism in the reverse bias condition. The differences between these samples have to be researched in the different quality of the oxide.

In order to understand the frequency-dependant behaviour, the time resolved EL signal over one period for frequencies among 100 Hz and 10 kHz are evaluated. The decay time for EL pulses corresponding to forward-to-reverse transitions are fitted at each frequency and for different voltage amplitudes using a stretched exponential decay. In fatc, for silicon nanocrystals, a stretched exponential decay is typically reported in the literature [51]. The fitting expression is the following:

$$EL\,(t) = EL\,(t = 0) \cdot \exp^{(-\frac{t}{\tau})^{\beta}}$$

where EL (t) and EL (t = 0) are the electroluminescence intensity during the decay and at t=0, respectively, τ is the decay time and β is called the dispersion factor. This parameter tells us the distribution of the silicon quantum dots size and the diffusion among different Si-NCs. In general, $\beta < 1$ represents a distirbution of indipendent single exponentials (from nanocrystals of a certain size as determines by the observation wavelength) with different lifetimes.

Figure 2.20 (left) shows the decay time as a function of the applied voltage for three different frequency values. The β values lie around 0.8. The decay time of the EL signal also decreases with increasing the frequency, as shown in Figure 2.20 (right). Higher frequencies induce a response from a smaller size distribution of silicon nanocrystals, which have a faster decay time [52]. Starting from the decay time and the rise time, it is possible to estimate the value of the excitation cross section for the Si-NCs under electrical pumping [50]. The results are reported in Figure 2.21 as a function of the voltage at a fixed square waveform frequency of 100 Hz.

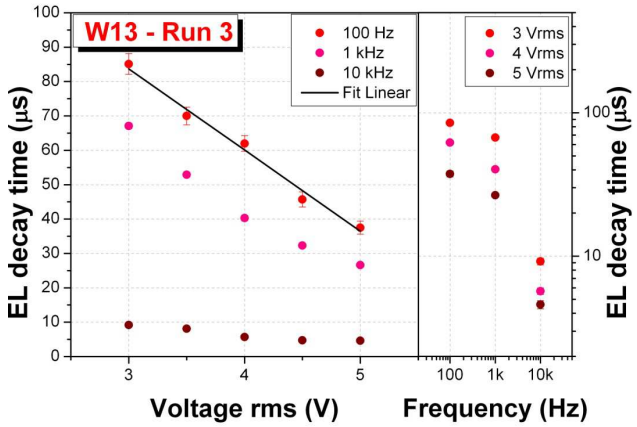


Figure 2.20. Dependence of EL decay time from both RMS voltage value **(left)** and frequency **(right)** for the Wafer 13 – Run 3 devices. The lifetimes are computed performing a stretched exponential fit during the forward-to-reverse transition of the exciting waveform. In some cases, the error bars are covered by the symbols.

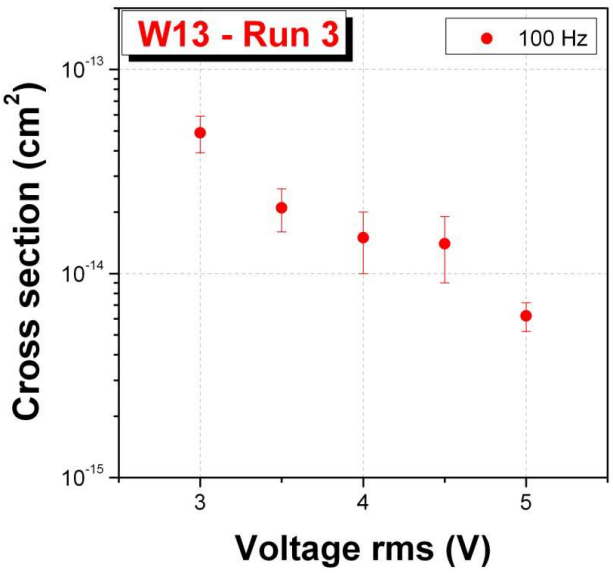


Figure 2.21. Excitation Si-NCs cross section as a function of the voltage, at a fixed square waveform frequency of 100 Hz.

The value of the excitation cross section decreases from few 10^{-14} to few 10^{-15} cm^2 with increasing the amplitude voltage. The values are in a good agreement with theoretical predictions and similar measurements done on Si-NCs light emitting devices by Irrera et al. or by Valenta et al. [50], [53], [54]. As expected, the highest values of the Si-NCs cross section are related to the best working condition for the studied LEDs, which is the direct tunneling regime ($\leq$ 3 V).

2.4 Power Efficiency estimation

The measurements reported so far are useful for the comparison between devices with similar characteristics and similar geometries. In order to compare the performances of the studied LEDs, parameters such as optical power and power efficiency are evaluated. The definitions of all these parameters are reported in Table 1.1.

The optical power has been measured with a large p-i-n photodiode, whose output current signal has been measured by a Keithley 6485 picoamperometer. A simple correction for the collection solid angle has been evaluated, taking into account the acceptance angle of the photodiode. The photodiode has been placed within a few millimeters above the LED. The optical power is estimated as $P = P_m/\sin^2\varphi$, where φ is the acceptance angle of the photodiode and P_m is the measured fraction of the total emitted optical power emitted into the air.

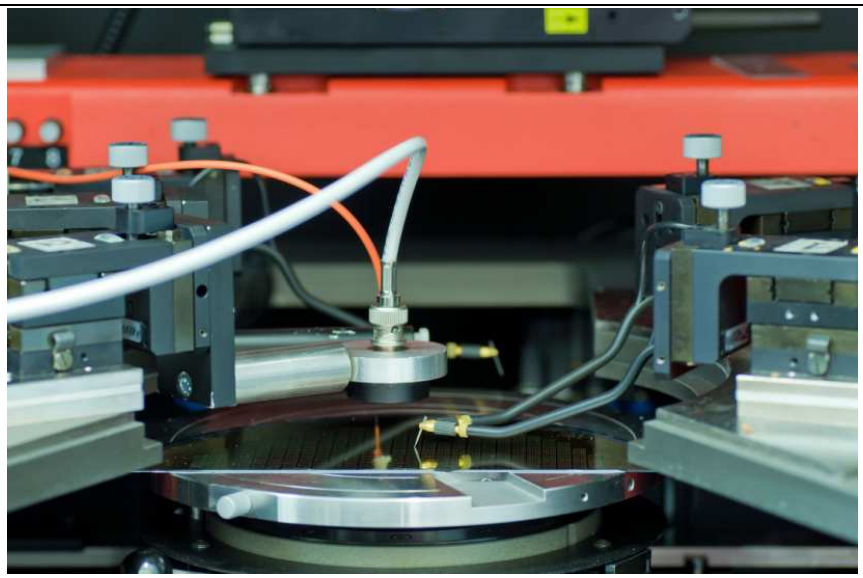


Figure 2.22. Experimental setup used to measure the optical power and the power efficiency.

Label	Optical Power Density (μW/cm^2)	Current Density (mA/cm^2)	Gate Voltage (V)	Power Efficiency (%)
Wafer 10 Run 2C	**0.19 ± 0.01**	**0.86 ± 0.01**	**2.30 ± 0.01**	**0.010 ± 0.001**
Wafer 13 Run 3	**0.51 ± 0.02**	**0.59 ± 0.01**	**2.00 ± 0.01**	**0.043 ± 0.002**

Table 2.2. Power efficiency estimation for different devices measured at low injected current.

Figure 2.22 shows a picture of the experimental setup with the wafer on the chuck, the electrical probes and the detector on the top of it. The highest values of power efficiency for Wafer 10 – Run 2C and Wafer 13 – Run 3 devices are reported in Table 2.2. The recorded values for the two wafers are showing that the fabrication process involved in Run 3 yields to the realization of more efficient LEDs in comparison to those of Run 2C. We can conclude that the different fabrication process has lead to the realization of a more efficient light emitting device.

Despite the power efficiency in Wafer 13 is enhanced by a factor of 4 with respect to the previous run, the value of the optical power density is anyway still too low for practical purposes in lightening. One possible application of such devices will be proposed at the end of the thesis.

2.5 Conclusions

In this chapter, charge injection, transport and recombination in silicon nanocrystals based LEDs have been presented. For the analysis and the electro-optical characterization, four devices have been studied. For the comparison, Wafer 10 – Run 2C and Wafer 13 – Run 3 have been analyzed because they have similar active layer, but different structure and layout. Moreover Wafer 16 and Wafer 17 - Run3 have been considered in order to figure out the character of charge injection occurring in the studied devices. In fact, the first has a 4 nm-thick oxide layer at the top of the ML, which serves as a tunneling barrier for electrons, and the second has a 4nm-thick oxide layer at the bottom of the ML, serving as tunneling barrier for injected holes. The use of electron or hole barriers made it possible to differentiate the electron and the hole injection giving more information about the opto-electrical behaviour of Wafer13.

The I-V sweeps show a non-rectifying behavior for Run2C devices, while a marked rectifying behaviour is shared in Wafer 13 - Run3, suggesting that there was a difference in the substrate for the two runs. Wafer 16 presents a similar behaviour of Wafer 13, while Wafer 17 share the same behavior of Wafer 10 – Run2C. We believe that the differences between the two I-V characteristics have to be researched in a different quality of the oxide, where in one case it is well insulating and in the second it leaks through. The critical interface for the injection mechanism in reverse bias condition is the one between the multilayer and the device substrate. Moreover, the C-V measurements give us an hint on the role of the thick barrier oxide in permitting the formation of the inversion layer, and, therefore, of the injection of hot electrons through the active layer.

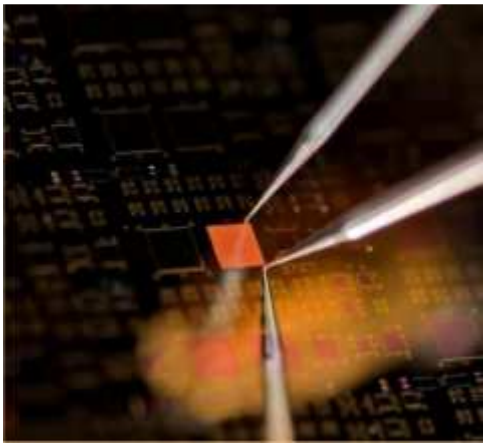
A spectral analysis of EL was performed on the studied samples, and starting from the obtained results the different emission mechanisms that can occur under appropriate gate bias condition have been discussed. The recorded spectra revealed a peak around 900 nm, evident below 3V in forward bias, and the onset of a peak at about 800 nm, at higher voltages. The origin of this behavior lies in the different mechanisms that generate luminescence in the silicon nanocrystals. The most probable path for EL involves both exciton recombination in the Si-NCs, at longer wavelengths, and defect-assisted recombination, where luminescence is the result of the recombination of carriers trapped at radiative recombination centers that form at the interface between Si-NCs and the dielectric or even in the dielectric itself. The light emission at low voltages is due to the bipolar (electrons and holes) injection via direct tunneling mechanism. In fact, EL occurs

at voltages lower than 3.1 or 4.7 V, which are the values corresponding to the height of the energy barriers at the silicon oxide interface for electrons or holes, respectively. At higher voltages, Fowler–Nordheim tunneling of hot electrons into the oxide conduction band occurs: EL is then produced by recombination of electron-hole pairs in the Si-NCs or through trapped carriers on radiative interface states, which have been excited by the current of hot electrons via an impact excitation mechanism. By applying square wave voltages at varying frequencies, integrated EL peaks at a frequency between 10 kHz and 100 kHz, depending on the root mean square value. Beyond these values the pulse duration will be shorter than the radiative lifetime of the Si-NCs and some of the excitons will not recombine due to the statistical nature of spontaneous emission.

Time-resolved EL measurements yield more direct information of the carrier dynamics of the devices operation. Using pulsed pumping scheme there is the possibility of sequentially injecting opposite carriers into the Si-NCs material, which subsequently recombine radiatively. This is pointed out by the presence of EL overshoots when the supply voltage is swept abruptly from positive-to-negative value and vice versa. Wafer10 - Run2C devices share this behaviour. On the contrary, Wafer13 - Run3 devices (rectifying I-V characteristic) present a lower EL emission peak only during forward-to-reverse bias transitions. The presence of these overshoots is associated with the excitons that remain inside the quantum dots even after the voltage is switched off. At this moment, the wavefunction overlap of each confined electron-hole pair is maximized and consequently the probability of radiative recombination is increased. The electron and hole barriers present in Wafer16 and Wafer17, respectively, allow for selection of the charge injection and the time-resolved EL characteristics of these two samples confirm the previous claims. W16 is quite similar to W13, while W17 – Run 3 to W10 – Run 2C. All the measurements confirm the fact that the injection from the substrate is the responsible of the differences between the samples. The key parameter needed to understand these devices is the injection mechanism in the reverse bias condition. The differences between these samples have to be researched in the different quality of the oxide.

Chapter 3

Silicon Nanocrystals Based Light Emitting Devices fabricated by CEA-LETI



Visible light emission from a device with silicon nanocrystals. The devices have been fabricated at the CEA-LETI center in Grenoble.

In this chapter, I will talk about silicon rich silicon oxide based light emitting devices, fabricated at the CEA-LETI laboratory in Grenoble, within the European project HELIOS. The devices have been realized after the work and the experience on the Si-NCs based LEDs obtained in the INTEL project, presented in the previous chapter. In this part of my work, after a brief introduction on the HELIOS project, the new device design and the active material optimization will be presented. After that, I will report the electro-optical characterization and the power efficiency estimation. At the end of the chapter, light emitting field effect transistors are reported, and a comparison between capacitors and transistors. A comparison, in term of devices performances is also done between these devices and the ones presented in the previous chapter.

3.1 The HELIOS project

As described in the introduction of the thesis, silicon photonics (or more precisely CMOS Photonics) is a way to tackle the problem by developing a small number of generic integration technologies with a level of functionality that can address a broad range of applications. In these three years, I have worked on the European HELIOS project. The HELIOS acronym stands for “pHotonics ELectronics functional Integration on CMOS”. The aim of the project is a complete integration between photonics and electronics within a single chip, all CMOS compatible and all silicon based. The objective of the HELIOS project is to combine a photonic layer with a CMOS circuit by different innovative means, using microelectronics fabrication processes. Within this European project, my work was in the Work Package 11, which has the aim to evaluate the potential of silicon related materials for light emission and light amplification. In particular, I was involved in the experimental characterization of silicon nanocrystals light emitting devices, erbium doped silicon nanocrystals light emitting devices and erbium doped silicon nanocrystals optical cavities. These three main topics will be presented in the last three chapters of my thesis.

3.2 Si-NCs based LEDs

In this section the mask and the device design are presented. The active material optimization and the structural analysis of monitor layer are also reported.

3.2.1 Device design

A schematic top view of the mask is presented in Figure 3.1. On every dies, there are two regions: one of n-type devices and one of p-type devices. For every region, there are several devices: capacitor, Van der Pauw structures and transistors. The dimensions of these devices can vary between 100 µm x 100 µm up to 1000 µm x 1000 µm. All the measurements performed in my work have been done on devices with emitted area of 300 µm x 300 µm. Figure 3.1 reports also a zoom on the detail of the capacitor used with the definition of the two metallic contacts used. For all the devices the cross section is the same. A schematic cross-section of a Si-NCs LED and a picture of it are shown in Figure 3.2 and in Figure 3.3, respectively. In Figure 3.2, the active layer is shown in the green color, while the bias polarization is reported with the light blue color. The polarization depicted in the figure is the one used for the forward bias condition, with the

negative bias applied on the n-type polysilicon on top of the active layer and the positive voltage applied on the p^+ silicon. This condition is the only one, which yields electroluminescence from the Si-NCs LEDs.

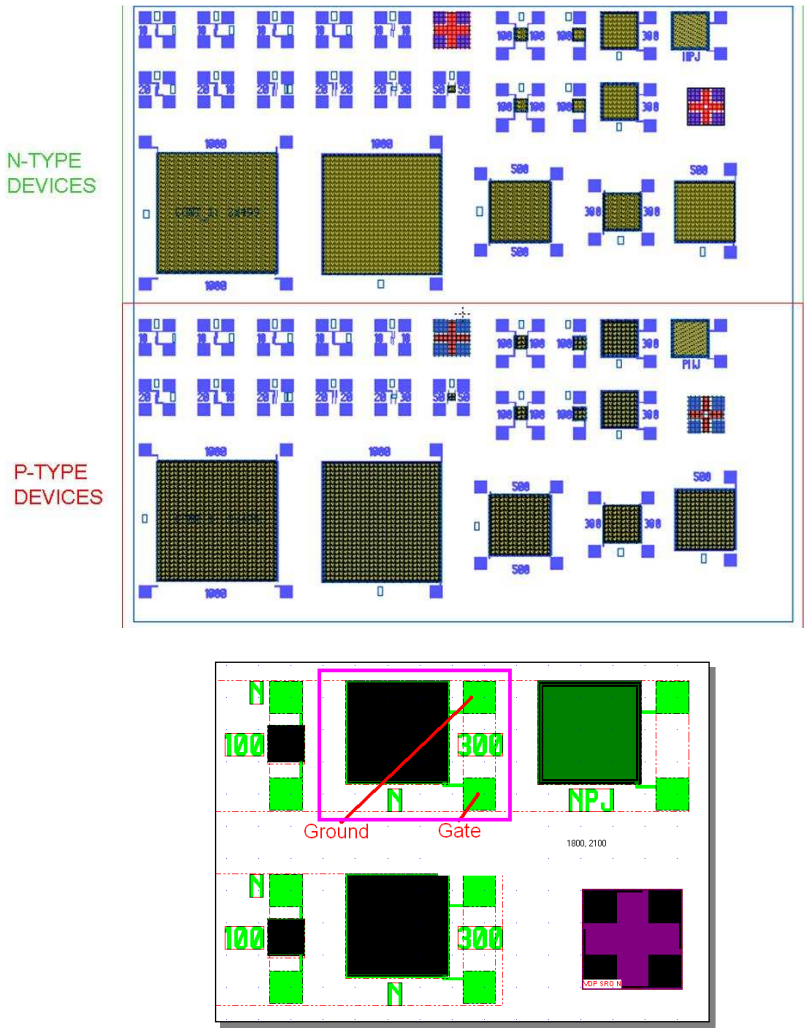


Figure 3.1. **(top)** Die layout of the mask for the silicon nanocrystals based light emitting devices. **(bottom)** Detail of the capacitor used, with specified the two electrical contacts.

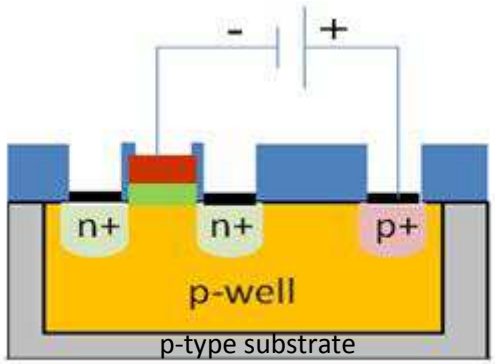


Figure 3.2. Si-NCs LED cross section. The active layer is shown in the green colour. The reported polarization is the one used for the forward bias condition.

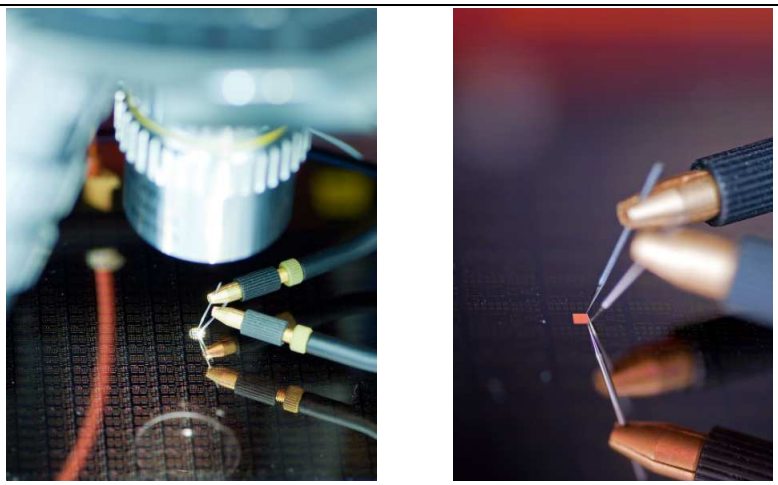


Figure 3.3. **(left)** Photograph of the fabricated Si-NCs LED wafers in a probe station and **(right)** Photograph of an orange emitting Si-NCs LED under forward bias (a red square at the probe tips). The device under test is a capacitor with an area of 1000 µm x 1000 µm at high voltage applied.

The device geometry and the layout of cross section have been designed by Alessandro Marconi and Oleksiy Anopchenko.

3.2.2 Active material optimization and structural analysis

Different runs have been fabricated within the HELIOS project. In this section, I will present the CMOS 1 and CMOS 3 batch run and I will enter in the detail of the active material splitting of these two different batches. In the following of this chapter, I will report the experimental characterization of the devices, always referring to the active material splitting here reported.

- ✓ **Single layers**

The silicon nanocrystals material optimization in terms of photoluminescence intensity and emission peak wavelength and optimization of numerous deposition parameters have been performed on a series of monitor wafers grown in two different monitor batches, not reported here. Further Si-NCs layer optimization has been performed via splitting of the growth parameters during the fabrication of the single layer Si-NCs LEDs. This run is called CMOS1 and it has as a goal the choice of the best annealing treatment and of the best silicon content excess. This run is formed by devices with single layer active material. The active material composition tells us the deposition technique (in this case, LPCVD), the thickness of the active material (50 nm) and the percentage of the silicon content excess. The annealing of the samples has been done either in a conventional furnace annealing or by means of rapid thermal processing (RTP). All the details are reported in Table 3.1.

Active layer composition	Wafer Label – Run: CMOS1				
	W1	W2	W3	W4	W5
LPCVD 50 nm 12 %					
LPCVD 50 nm 16 %					
Annealing RTP 1100°C, 5 min					
Furnace annealing at 900°C, 1h, *effective 14 h 30 minutes*					
Furnace annealing at 1100°C, 1h					

Table 3.1. Composition of the active layer of the single layer Si-NCs LEDs.

✓ **Multilayers**

The multilayer geometry of the active material allows achieving a better control of the Si-NCs formation via confined growth of nanocrystals [40], [55], [56]. Moreover, multilayers provide an independent control over the size and density of Si NCs, silicon oxide thickness and composition (stoichiometry) in the direction of the electrical current flow. A small series of monitor Si-NCs multilayers has been grown and characterized (see Table 3.2). This batch of multilayered monitor wafers is called CMOS3 – Control batch. The photoluminescence measurements and the complete optical characterization of this batch have been performed by Nikola Prtljaga. As a result of his characterization, the optimized multilayer growth parameters have been found and multilayer Si-NCs LEDs have been fabricated. This run is called CMOS3. All the details are reported in Table 3.3.

Active layer composition	Wafer Label Run: CMOS3 – Control Batch						
	W19	W20	W21	W22	W23	W24	W25
LPCVD (2 nm 0% + 3 nm 20 %) x10							
LPCVD (2 nm 0% + 3 nm 25 %) x10							
LPCVD (2 nm 0% + 4 nm 20 %) x8							
Annealing RTP at 1100°C, 5 min							
Furnace annealing at 900°C, 1h							
Furnace annealing at 1000°C, 1h							
Furnace annealing at 1100°C, 1h							
Extra annealing at 800°C, 6h							

Table 3.2 Composition of the active layer of monitor Si-NCs multilayers.

Active layer composition	Wafer Label Run: CMOS3			
	W21	**W22**	**W23**	**W24**
LPCVD ((2 nm 0% + 3 nm 20 %) x 10) + 2 nm 0 %				
LPCVD ((2 nm 0% + 3 nm 25 %) x 10) + 2 nm 0 %				
LPCVD ((2 nm 0% + 4 nm 20 %) x 8) + 2 nm 0 %				
LPCVD ((2 nm 0% + 4 nm 25 %) x 8) + 2 nm 0 %				
Furnace annealing at 1000°C, 1h				

Table 3.3. Composition of the active layer of multilayered Si-NCs LEDs.

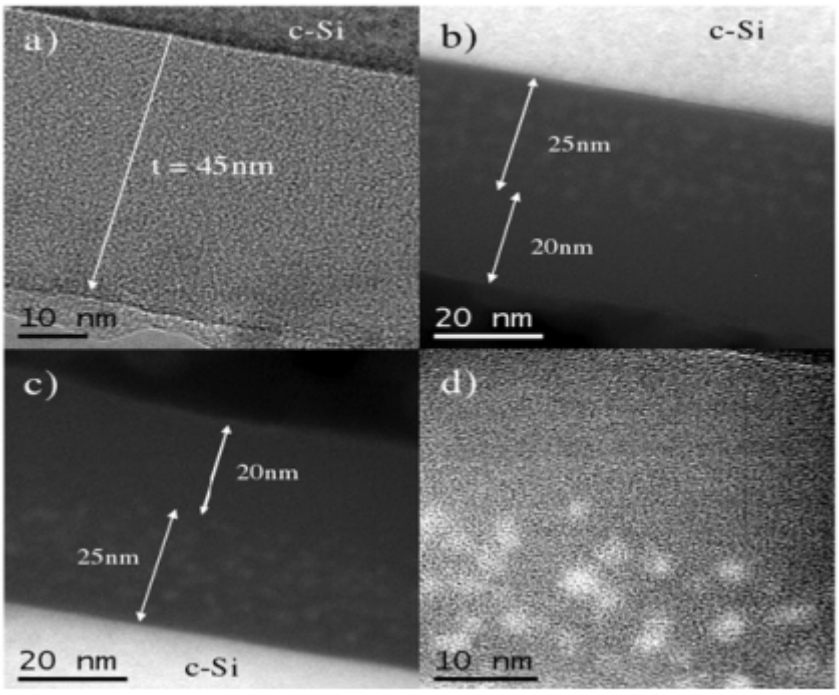


Figure 3.4. **(a)** Unfiltered TEM image revealing a layer thickness of 45 nm; **(b)** and **(c)** Filtered images, obtained filtering around the Si Plasmon peak (17 eV) in different regions of the sample, show the presence of the silicon nanocrystals in the lower half of the active layer close to the substrate. The multilayered structure is hardly maintained and the Si excess aggregation is randomly distributed; **(d)** Diameters of the precipitates ranges between 2.5 nm and 3 nm.

The Si-NCs LEDs have been fabricated by means of the LPCVD technique at the CEA-LETI laboratory, in Grenoble. In Table 3.2 and Table 3.3 the active material is presented as a multilayered structure, with x nm of silicon dioxide (the percentage of silicon content excess is 0%) and z nm of silicon nanocrystals formed after the deposition of some silicon content excess, presented in percentage. These alternating structure is repeated either ten or eight times, depending by the wafer. For the CMOS3 run the annealing was equal for all the wafers and was fixed at 1000 °C for one hour.

In order to check the fabrication process, a TEM image of W21 of the CMOS3 run (see Table 3.3) has been requested. The TEM analysis has been done at the Scientific and Technological Center of the University of Barcelona. Figure 3.4 shows the TEM images obtained. It is evident that the nominal structure is not respected. Some problems occur in the fabrication processes and so in the real devices the multilayered structure is hardly maintained. The sample shows two different zones, a dark one, 20 nm high, and another one of 25 nm thickness, with white dots, which are the silicon quantum dots. The total thickness of the active layer is 45 nm, and so less than the one expected. The darker layer on top can be considered as silicon dioxide. Our hypothesis is that, during the fabrication process, some of the layers on the top of the active layer have undergone an oxidation process. In the second region, instead, it can be clearly observed the presence of the Si-NCs. The size of the quantum dots ranges between 2.5 nm and 3 nm. Even if the total multilayer structure is lost, the Si-NCs dimensions are respected. The structural analysis on the fabricated samples has been done on only W21, but we believe that also the other wafers of this run have undergone the same annealing treatment, and so they have similar problems.

3.3 Single layer and multilayer Si-NCs LEDs

3.3.1 Electrical charge transport

The Si-NCs LEDs operate at high voltages, because of the unwanted thick oxide layer on top of our devices. We have performed a detailed analysis of charge transport and correlate it to the growth parameters and structure of the Si-NCs layer of the CMOS 1 run (see Table 3.1). The objective of this study is the comparison between samples with different silicon content excess and different annealing treatment. We have decided to fit the current-voltage (I-V) curves with two different models. These models are: i) the Poole-Frenkel (P-F) one, which corresponds to thermally activated conduction between localized states in the gap assisted by the electric field [57] and ii) the Fowler-Nordheim (F-N) one, which describes the tunneling of charges through a triangular barrier, from the electrode into the dielectric [58] or between localized states. Note that by localized state we understand defects in the oxide matrix, or Si nanoclusters. More details on these two model, with also the F-N equation, can be found in section §1.4.3. Each of the experimental I-V curves has been fitted with these relations. The plots are reported in Figure 3.5. The fit parameters are the height barrier and the relative permittivity,

respectively. The fitting with both models provides an interesting evolution of the transport properties with annealing treatment, which is believed to be a consequence of the material microstructure. Indeed, the layers annealed by RTP show at low voltages a current that is too large to be originated from Fowler-Nordheim injection. A better agreement with the Poole-Frenkel law is found on a wide range of voltages. However, in layers annealed by conventional furnace, the current gets lower, and a better agreement with the Fowler-Nordheim law is found. This suggests that for the same annealing temperature (1100 ◦C), the injection is more difficult when the annealing time is longer, leading to higher voltages required to promote charges transport. The influence of the annealing treatment on the material properties can have several origins. On one hand, it is well known that an annealing procedure is required to cure the layer from the defects introduced by the processing.

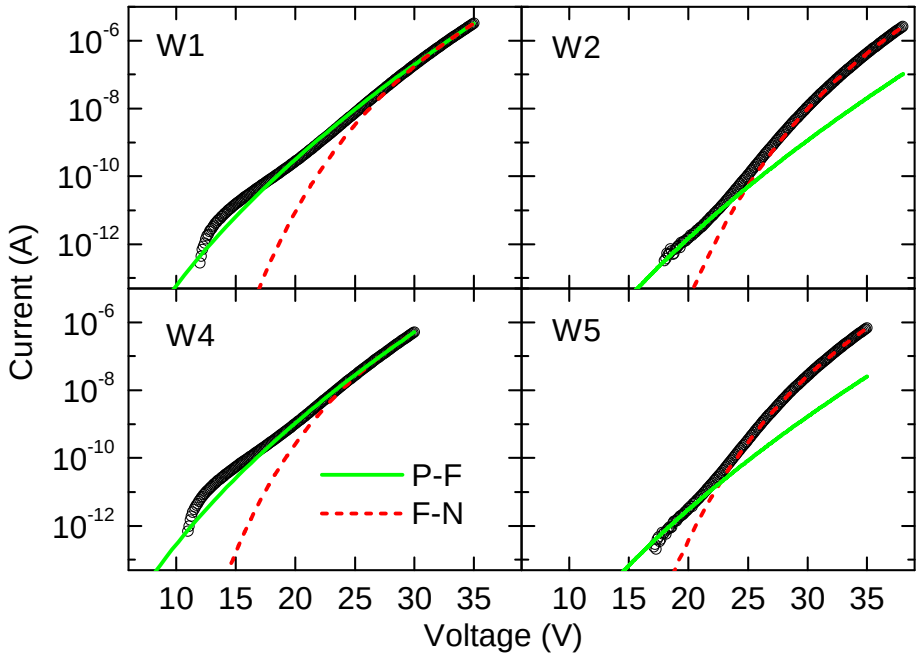


Figure 3.5. Fits of the I-V curves by the models Poole-Frenkel (green continuos line) and Fowler-Nordheim (red dashed line). The labels W1, W2, W4 and W5 refer to Table 3.1.

An annealing of 5 minutes may not be sufficient [59]. On the other hand, at this temperature the formation of Si nanoclusters is expected, as also confirmed by the measured electroluminescence centered at around 800 nm, which is attributed to quantum confinement or to Si-NCs surface states [60], [61]. We suggest that a different nanoclusters size and spatial distribution are formed for each of the annealing treatments. However, the Si excess does not seem to have any specific influence on the transport mechanism for the range of Si excesses studied here. We can just observe larger currents

when a larger Si excess is introduced. To go further we have looked at the relative permittivity we can extract by fitting the I-V curves with the P-F law, or the injection barrier that we can extract from the F-N fit. These values are reported in the Table 3.4. When the P-F model is used to fit the I-V curves at high voltages (larger than 30 V), a permittivity of about 4.5-5 is found for the RTP layers, and less than 2.5 for the layers annealed in the conventional furnace. This latter value is too low to be acceptable, whereas 4.5-5 is a value expected for a Si-rich silicon oxide [41]. In Figure 3.5, the fit by the P-F law has been done by maintaining the permittivity at about 4.5-5. This leads to an agreement with the P-F model at lower voltage, on a reduced range of voltages. Above a threshold voltage, the F-N law is found to fit well the I-V curves. Concerning the barriers heights found from the F-N fit, larger values are found for the layers annealed one hour. These values corroborate that i) injection is more difficult for these layers than for the RTP ones, and ii) the transport is essentially done by electrons, because if holes would be involved, larger values would have been obtained, as holes see a much larger potential barrier than electrons. Note however that the holes injection in the active layer limited to a region close to the Si substrate cannot be discarded [62].

	Height barrier (eV) [F-N]	**Relative permittivity [P-F]**
W1	1.6 ± 0.2	4.5 ± 0.5
W2	2.0 ± 0.3	2.4 ± 0.4
W4	1.3 ± 0.2	5.1 ± 0.5
W5	1.8 ± 0.2	2.5 ± 0.3

Table 3.4. Injection barrier height and permittivity extracted from the fits of the I-V by model Fowler-Nordheim and Poole-Frenkel respectively. The labels refer to Table 3.1.

To summarize the electrical properties found in these Si-NCs LEDs, for devices with long annealing treatments, we found that electrical current obeys the field-enhanced Fowler-Nordheim tunnelling law at high voltages. However, a better agreement with the Poole-Frenkel law is found at low voltages and over a large range of voltages in Si-NCs layers annealed by rapid thermal annealing (RTP). Within the range of Si excess used in our LEDs, we have not observed any significant contribution to the current from bipolar direct tunneling. In comparison to the Si-NCs LEDs presented in the previous chapter, in fact, here the applied bias voltages are one order of magnitude higher. The bipolar direct tunneling has therefore also to be ruled out because of the high voltage applied.

3.3.2 Electroluminescence measurements of optimized LEDs

The results presented here have been obtained from optimized Si-NCs LEDs, namely the single layer Si-NC LEDs W 2 and W3 (see Table 3.1) and the multilayer Si-NCs LED W21 (see Table 3.3). The other LEDs show either similar results or the results that fall short of the objectives. In terms of charge transport, the Fowler-Nordheim injection becomes the most efficient transport mechanism inside the devices, providing higher quantum efficiencies due to the injection of hot electrons impacting directly with nanocrystals, generating e-h pairs suitable for radiative recombination. The I-V characteristics of the studied device are shown in Figure 3.6. The voltages applied to the LEDs are higher than the one applied to the INTEL's LEDs, because of the unwanted thick silicon oxide layer on top of the active layer. The I-V shows a not-rectifying behavior, but it is difficult to compare this current-voltage characteristic with the ones reported in the previous chapter. In the I-V, it has to be noticed the presence of the two big hysteresis loops, both in forward than in reverse bias. As discussed also in Chapter 2, the hysteresis originates from the charge accumulation within the SRO layer. Positive charges are accumulated under forward bias condition.

Electroluminescence (EL) spectra of the optimized single layer and multilayer LEDs are shown in Figure 3.7. The spectra were collected at the same current density of about 1 mA/cm^2. The Si-NCs emission has a broad wavelength range with a peak wavelength at around 800 nm. The light intensity of the multilayer LED is somewhat lower than the single layer LED due to the lower annealing temperature in the fabrication process.

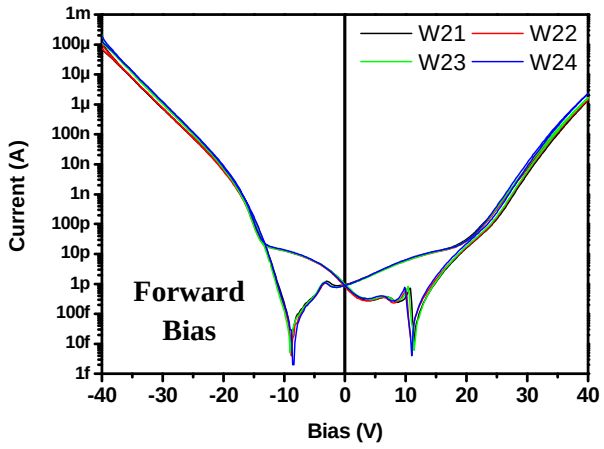


Figure 3.6. I-V characteristics of the CMOS3 multilayer devices.

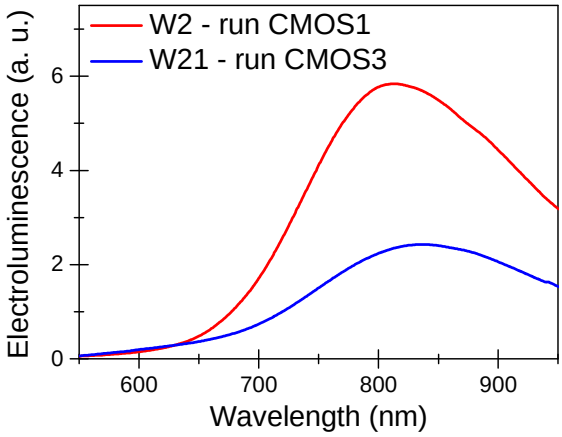


Figure 3.7. EL spectra of the optimized single layer and multilayer Si-NCs LEDs.

AC bias yields improved EL emission (see Figure 3.8). Figure 3.8 shows the integrated EL as a function of the driving frequency. The Si-NCs LEDs are driving with a square waveform under AC excitation. The sample reported is W5, but we can obtain similar results for all the samples under study [63]. The difference between the blue and the red points is the different AC square waveform applied to the device. The red constant line shows the EL signal obtained under DC excitation. We can immediately see that the electroluminescence signal is enhanced. The EL increases significantly as the frequency increases, it reaches a maximum (in this case at around 10 kHz of driving frequency) and, then, it decreases. This increase in EL is attributed to a major injection of carriers, both electrons and holes, up to a maximum frequency. After this, the decrease is attributed to the Auger suppression of the EL due to the finite exciton recombination lifetime [64], [65].

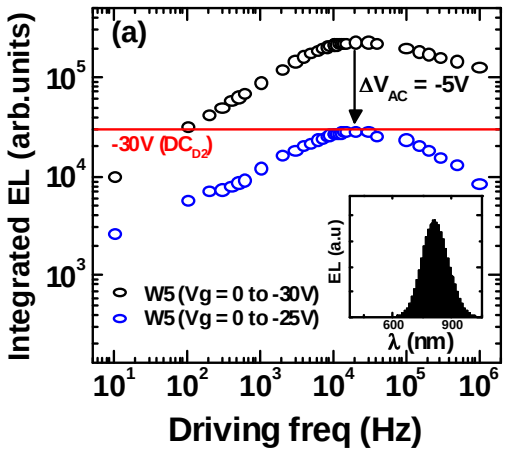


Figure 3.8. Integrated EL intensity as a function of the driving frequency, under a negative square pulse applied. The typical EL spectrum is shown in the inset.

The integrated electroluminescence as a function of the injected current and of the applied voltage is shown in Figure 3.9. The log-log plot of the EL (I) indicates if the behavior is linear, sublinear or superlinear. The slopes are reported on the plot, but we can affirm that the dependence is linear for all the devices under study. The optical power density and external quantum efficiency, EQE, of the Si-NC LEDs as a function of current density in DC bias conditions are shown in Figure 3.10 and in Figure 3.11, respectively. The optical power density increases linearly with the current density and reaches a value of ~2 $\mu W/cm^2$ without any significant sign of power saturation at high current densities. The maximum achieved power density is 7 $\mu W/cm^2$ (not shown in the Figure). However, the operating voltages and the electric fields are high (7 MV/cm), and this fact could have a detrimental effect on the device stability and on the power consumption. The multilayered Si-NCs LEDs show a similar behavior due to a low average Si excess and thick barrier thicknesses. The annealing temperature and Si-NCs formation have a large effect on the LED characteristics. Higher annealing temperatures lead to a larger extent of phase separation of non-stoichiometric silicon oxide and hence better passivation of Si nanocrystals and larger quantum efficiency. However, less defects in silicon oxide matrix that confines the Si nanocrystals also accompanied by larger voltages required for charge tunnelling if the silicon oxide that separates Si nanocrystals is thick and the direct tunneling currents are very small.

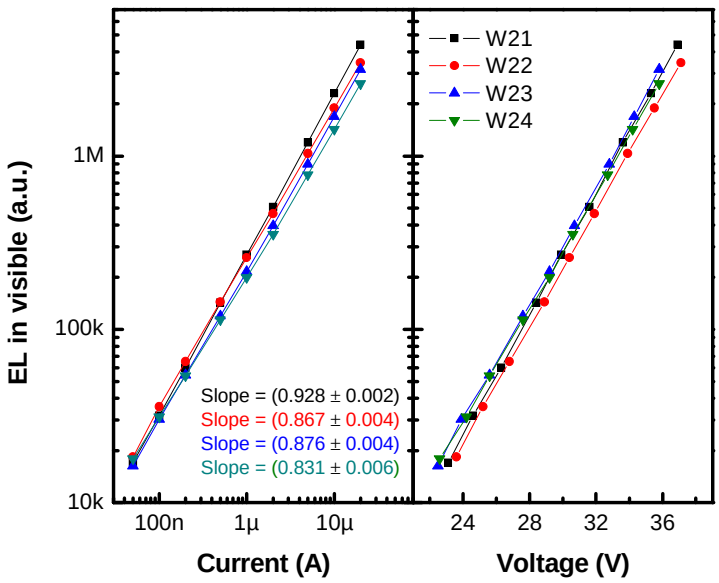


Figure 3.9. Integrated electroluminescence as a function of the injected current/applied voltage for the four multilayered devices presented in Table 3.3 (CMOS3 run).

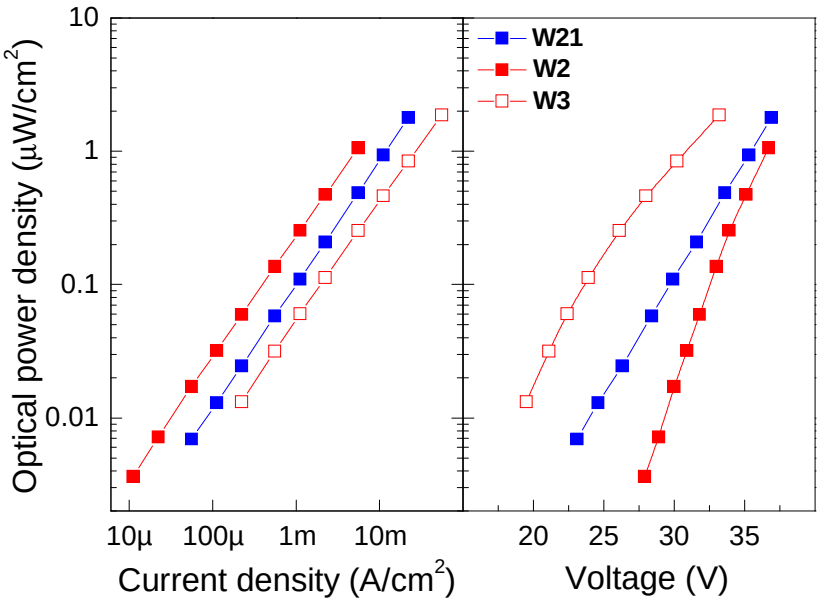


Figure 3.10. Optical power density of single layer and multilayer Si-NCs LEDs as a function of the applied voltage and current density. Annealing temperature of the Si-NC layer is indicated in the legend.

The external quantum efficiency of about 0.03% and 0.01% has been measured in the single layer and multilayer Si-NCs LEDs with optimized fabrication parameters, respectively (see Figure 3.10). The EQE only slightly decreases over the current density range used in the experiment. The better E.Q.E. is obtained in the sample which has undergone the treatment at the highest annealing temperature.

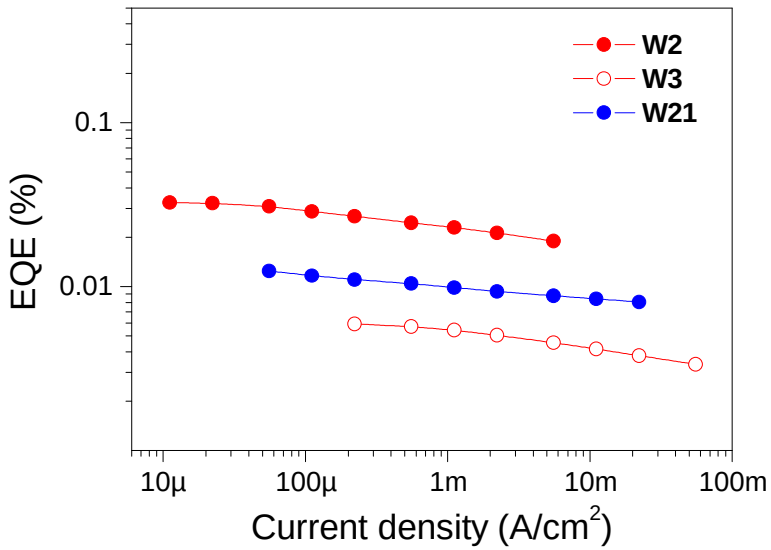


Figure 3.11. External quantum efficiency, EQE, of the single layer and multilayer Si-NCs LEDs as a function of the current density. The maximum EQE value achievable is about 0.03 %.

3.3.3 LEDs summary

Silicon nanocrystals based light emitting devices are designed by A. Marconi and A. Anopchenko and they are fabricated at the CEA-LETI laboratory, in Grenoble. The LEDs emit light at around 800 nm and the light emission is also visible with a standard camera. The most important results obtained with the characterization of different sample batches can be summarized as following:

- ✓ The electrical injection in the Si-NCs LEDs with long annealing treatments obeys a Fowler Nordheim law, while the devices annealed at low temperatures/short time are governed by trap assisted centers (Poole-Frenkel). The onset voltages of electroluminescence for both single and multilayer devices are around 20 V. High voltages are required in these LEDs, since some of the layers on the top of the active layer have undergone an oxidation process, during the fabrication. Direct tunneling cannot be achieved in these Si-NCs LEDs;
- ✓ I-V characteristic are not rectifying, but it is difficult to compare this result with the ones obtained in the previous chapter, because of the high voltage required in these samples. The EL is achieved in forward bias regime and the electroluminescence increases linearly as a function of the injected electrical current;
- ✓ Optimized Si-NCs LEDs have an external quantum efficiency of ~ 0.03 % at low current densities and show several microwatts per square centimeter of optical power density with the peak wavelength at around 800 nm;
- ✓ The main limitation in the LED efficiency is the injection mechanism due to the thick tunneling barrier in the multilayer sample. The unwanted silicon dioxide thick layer on top of the devices does not allow the direct tunneling in our devices. The main injection mechanism is the unipolar. There is room for improving the efficiency of the LEDs by raising the annealing temperature in the fabrication process. Unfortunately, the fabrication of another batch of samples within the HELIOS project was not possible.

3.4 Light Emitting Field Effect Transistors

In this section, a possible way to build an on-chip electrically pumped light source, using a light emitting field effect transistor (LEFET), instead of a MOS capacitor, is reported. The novelty of this approach is that the active material of the transistor gate is composed by an alternating structure with silicon oxide and silicon rich silicon oxide layers. The characterization of this kind of devices will be done by means of both electrical and optical measurements, and the results of this study will help to develop practical optoelectronic and photonic devices, with higher value of external quantum efficiency in a structure with silicon oxide and silicon rich silicon oxide layers. The most important difference between the capacitors and the transistors is that we have more degree of freedom in the use of the device itself, because we can use the source, the drain, the body and the gate.

3.4.1 LEFETs design

The devices studied in this work are light emitting devices based on light emitting field effect transistor. The active region of the device is an alternating structure with a nominal thickness of 50 nm, deposited by the LPCVD technique. A schematic cross section of the LEFET is shown in Figure 3.12.a and the top view of the LEFET and light emitting MOS capacitor is shown in Figure 3.12.b and in Figure 3.12.c, respectively. The study has been performed on n-type LEFETs, with an emitting area of 300 x 300 μm^4 (gate length x gate width). In Figure 3.12.b the four pads for the electrical contacts are also reported: source (S), drain (D), body (B) and gate (G).

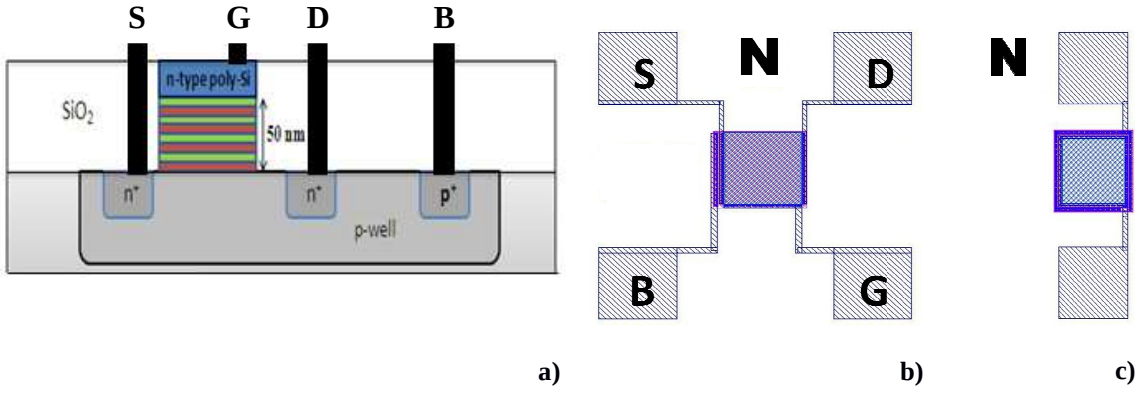


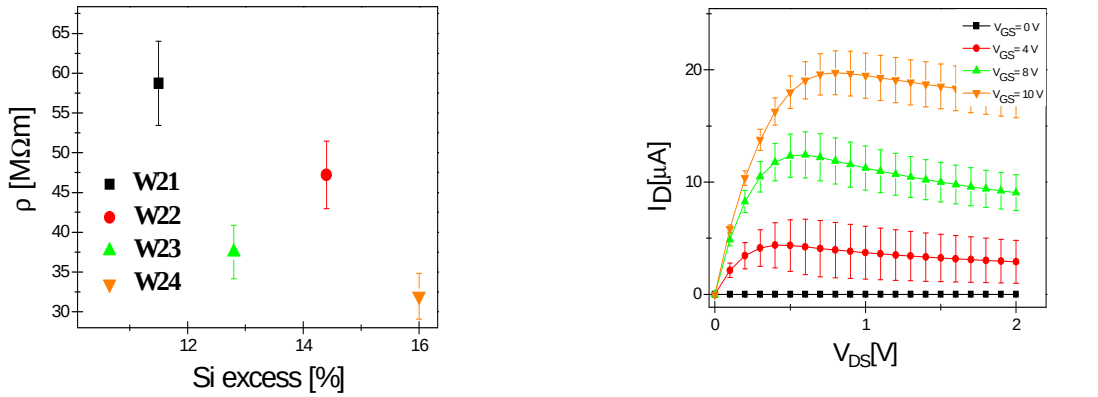
Figure 3.12. **a)** A schematic cross section of the LEFET and top view of **b)** LEFET and **c)** MOS capacitor.

The LEFETs are fabricated always at the CEA-LETI in Grenoble and they present the same active material splitting of the Si-NCs LEDs reported in Table 3.3.

3.4.2 Electrical characterization

- **Current-Voltage characterization**

An electrical characterization has been performed on the different devices. The current-voltage (I-V) characteristic has been recorded using an Agilent B1500A semiconductor device analyzer, at room temperature. The LEFET source terminal is connected to the body terminal, and both are connected to the ground. The current at the drain, I_D, has been monitored first as a function of the voltage between the body and the gate, V_{GS} from -30 V to +30V, and back, fixing the voltage between the drain and the source, V_{DS}, at 2 V, in order to evaluate the resistivity of the gate oxide with Si-NCs, ρ. The LEFET has a non-ohmic behaviour but it is still possible to evaluate the ratio between the electric field and the current density. Figure 3.13.a shows the values of ρ, which have been extracted at 30 V, as a function of the silicon excess. The higher the silicon excess the lower the resistivity of the gate oxide. It has to be noticed that ρ for a LEFET having as active material silicon dioxide is equal to $4*10^3$ MΩ*m. Moreover, the resistivity is lower for the devices with thicker SRO layers of the multilayer stack and hence larger Si-NCs. Secondly, I_D has been collected at a fixed voltage V_{GS} and scanning the potential between drain and source, V_{DS}, from 0 to 2 V. These measurements have been done for different value of V_{GS}, from 0 V to 10 V. Figure 3.13.b shows I_D of W21 as a function of V_{DS}. Once reached the saturation voltage, V_{SAT}, I_D decreases slowly instead of maintaining a constant value.



a) **b)**

Figure 3.13. **a)** Resistivity and **b)** current-voltage characteristic of W21.

- **Capacitance-Voltage characterization**

The capacitance-voltage (C-V) data has been collected at a frequency of 100 kHz. The source and the body terminals have been connected to ground. C-V measurements allow determining the flat band voltage V_{FB}, the flat band capacitance C_{FB}, the dielectric constant and the trapped charge in the devices. The LEFETs show very similar hysteresis curves, but W22 and W24 have a larger hysteresis width in comparison to W21 and W23. Larger is the width, more charge can be trapped in the devices. The charge trapped value can be calculated through the formula $\Delta Q=C_{FB} \times \Delta V$, where C_{FB} is the capacitance at the flat band condition and ΔV the hysteresis width at the capacitance value equal to 80% of the maximum capacitance, C_{MAX}. Figure 3.14 reports a C-V characteristics of W21, showing, C_{FB}, 80% of C_{MAX} and ΔV_{FB}.

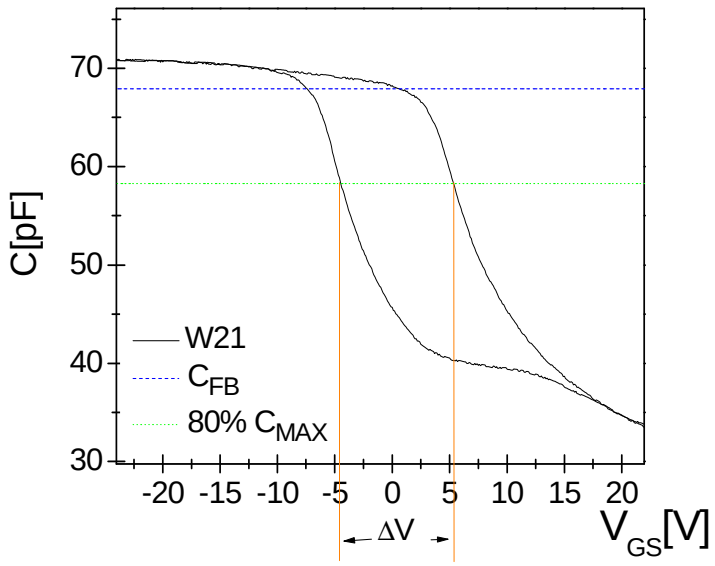


Figure 3.14. C-V characteristic of W21.

The flat band voltage, V_{FB}, can be easily extracted as the voltage in which the capacitance is equal to C_{FB}. C_{FB} is usually computed by using the thicknesses and the dielectric constants $\varepsilon_{r,i}$ of the different parts of the device. The values of the charge trapped in the gate oxide, the $\varepsilon_{r,i}$ and the C_{FB} are summarized in Table 3.5 for all the devices under study.

	W21	W22	W23	W24
ΔV[V]	9.86 ± 0.05	11.49 ± 0.05	10.70 ± 0.05	11.05 ± 0.05
C_{FB} [pF]	66.3 ± 0.5	63.4 ± 0.5	65.7 ± 0.5	64.8 ± 0.5
$\varepsilon_{r,i}$	4.6 ± 0.2	4.4 ± 0.2	4.4 ± 0.2	4.3 ± 0.2

Table 3.5. V_{FB}, C_{FB}, $\varepsilon_{r,i,}$ and the density of total charge, holes and electrons trapped in the device.

3.4.3 Optical characterization

- **Photoluminescence measurements**

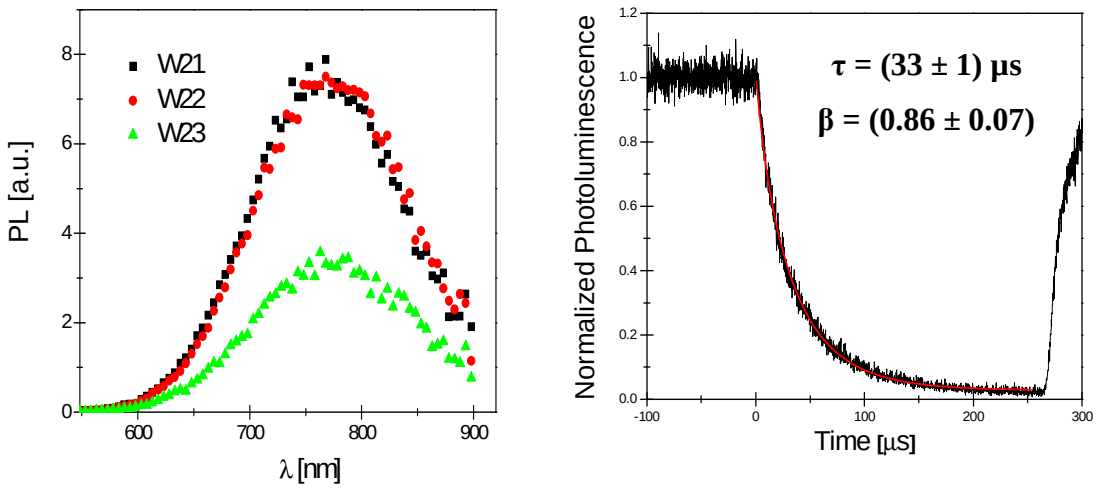
For the photoluminescence (PL) measurements, the 354.7 nm line of Nd:YVO_4 laser with an average power of 0.1-5.0 W has been used. During the continuous wave (CW) PL measurements, the laser beam passed through an attenuator to keep the power intensity constant at 20 mW. The detection system consisted of a monochromator coupled to a GaAs photomultiplier with an overall resolution of 2 nm for the visible range. PL was measured on monitor silicon wafers with the same processed silicon oxide multilayers. The spectra of the different samples, reported in Figure 3.15.a, show a similar shape, but not the same intensity: W23's intensity is lower than W21 or W22. This difference in the intensity can be explained by the different ratio between Si and SiO_2. In fact, we are near the maximum of the total luminescence emission as a function of SiO_2/Si, which implies that a variation of this percentage induces a lower intensity in the PL [66]. In addition, the absence of W24 in the monitor wafers batch did not allow further considerations, such as the intensity as a function of the different structures. The peak wavelength is different for all the samples, due to the different size of the nanocrystals for each sample. This behaviour confirms the presence of Si-NCs in the sample, and, even if the multilayer structure is hardly maintained, the alternating deposition is still important to determine the properties of the Si-NCs, particularly size and size distribution. After that, the time-resolved measurements have been done. The excitation has been performed modulating the laser beam by a mechanical chopper which was modulated by a square wave. The same square wave has been sent to a multichannel scaler SRS 430. The resolution of the measurements is of μs, while the modulation frequency of 19.00 Hz has been chosen to guarantee the attainment of steady-state condition. The power beam has been maintained constant at 9.5 mW. The PL decay is not exponential, but it is well described by the

stretched exponential function, as shown in Figure 3.15.b, for W21. The mathematical expression is the following:

$$PL\,(t) = PL\,(t = 0) \cdot \exp^{(-\frac{t}{\tau})^{\beta}}$$

where PL (t) and PL (t = 0) are the photoluminescence intensity during the decay and at t=0, respectively, τ is the decay time and β is called the dispersion factor. This parameter tells us the distribution of the silicon quantum dots size. In general, β < 1 represents a distirbution of indipendent single exponentials (from nanocrystals of a certain size as determines by the observation wavelegnth) with different lifetimes.

The physical origin of such behaviour is still a matter of discussion, the most commonly accepted explanations are related to the exciton migration between inter-connected nanocrystals, the variation of the atomic structure of Si-NCs of different sizes and the carriers tunnelling from Si -NCs to distribution of non-radiative recombination traps [67]. The recombination time for all the samples is around 35 μs, which is in agreement with the estimated size of the nanocrystals (between 2.5 and 4.0 nm). β values are between 0.66 and 0.87. W21 exhibits the lower τ_{PL} and the higher β, which means that the nanocrystals formed in W21 are the smallest one and with narrow size distribution. It can therefore be assumed that the energy transfer takes place with a good efficiency in W21. The values of all the different samples are summarized in Table 3.6.



a) **b)**

Figure 3.15. **a)** Photoluminescence spectra and **b)** time resolved photoluminescence for W21, with the mathematical fitting performed using a stretched exponential function.

	W21	W22	W23
λ [nm]	769 ± 1	774 ± 1	776 ± 1
τ_{PL}[μs]	33 ± 1	37 ± 2	35 ± 1
β	0.86 ± 0.07	0.66 ± 0.04	0.77 ± 0.05

Table 3.6. Parameters extracted from the photoluminescence characterization.

- **Electroluminescence measurements**

Electroluminescence (EL) measurements have been performed applying a direct current (DC) voltage between the body and the gate terminals of the LEFET. Also in this case, source and body have been grounded. All the devices under study show EL. The voltage region in which it has been possible to make the measurements is limited in forward bias between -20 V and -40 V, and between 20 V and 35 V in reverse bias. The lower limit is given by the fact that below 20 volts there is no EL, the upper one is the maximum voltage which could be reached before the device breakdown. The normalized spectra at different voltage applied at the gate are shown in the Figure 3.16. It has been also observed, that at different voltage, the position of the wavelengths for peaks changes, showing a red shift when the amplitude of the voltage applied decreases. This is due to the fact that different voltages allow activating Si-NCs with different size. W21, with W22, shows a minor variation of the position of the peak as evidence of the better uniformity of size distribution of the nanocrystals. Figure 3.17 shows the dependence, in forward bias, of the integrated EL as a function of the injected current. The trends are linear with respect to the injected current through the gate, I_G. This result is in a great accordance with the one reported for the Si-NCs LEDs in the previous section of this chapter (see Figure 3.8). The maxima and the minima peak's wavelength and the slopes of the plotted EL (I_G) are all summarized in Table 3.7 for all the samples.

	W21	W22	W23	W24
λ_{min} [nm] (at -40V)	777 ± 4	782 ± 4	772 ± 4	789 ± 4
λ_{max} [nm] (at -25 V)	805 ± 4	809 ± 4	806 ± 4	822 ± 4
$Slope_{forward}$	0.95 ± 0.05	0.90 ± 0.05	0.95 ± 0.05	0.88 ± 0.05

Table 3.7. Maxima and minima peak's wavelength and the EL (I) slopes.

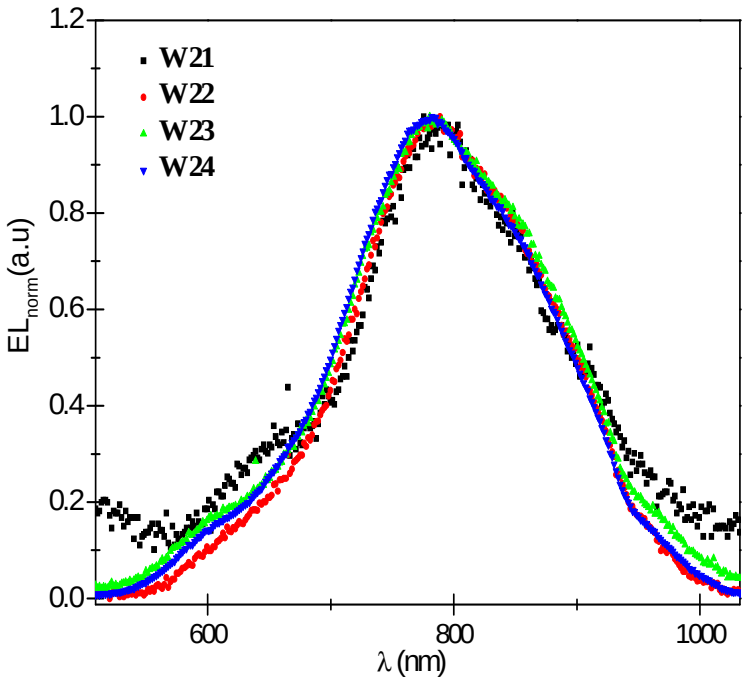


Figure 3.16. Normalized EL spectra for all the devices under study.

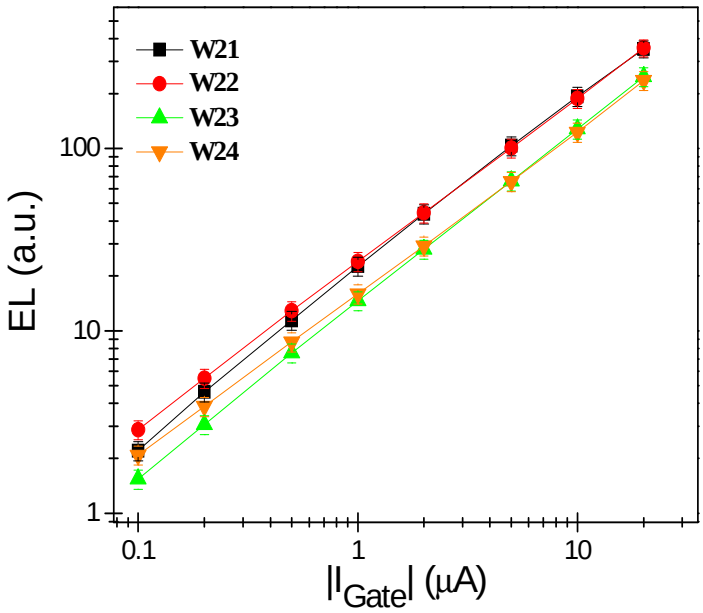


Figure 3.17. Integrate electroluminescence as a function of the injected current in a log-log plot.

From these measurements it has also been possible to evaluate the optical power, the external quantum efficiency and the power efficiency. The forward bias regime shows the higher electroluminescence intensity, which implies a stronger optical power density, and, at the same time, a larger quantum external efficiency and the larger value of power

efficiency. This fact is due to the kind of excitation which is given by impact excitation by electrons and so it is more efficient in the forward regime condition. The values of EQE achieved are one order of magnitude lower than the ones obtained with the MOS capacitor. The properties of the LEFET under alternate current (AC) regime have also been studied. The voltage applied between the body and the gate is taken as an RMS drive voltage. In this case, it has been observed that, beyond a certain frequency threshold, around 10 kHz, electroluminescence increased profoundly, due to the e-h wave function overlap, until a maximum frequency (700 kHz), where other recombination processes - particularly Auger's ones - become dominant. It has to be noticed that an alternate current regime allows having a good luminescence even at lower voltages than in DC regime. This is in agreement with previous works on similar silicon nanocrystals based light emitting devices [49], [64].

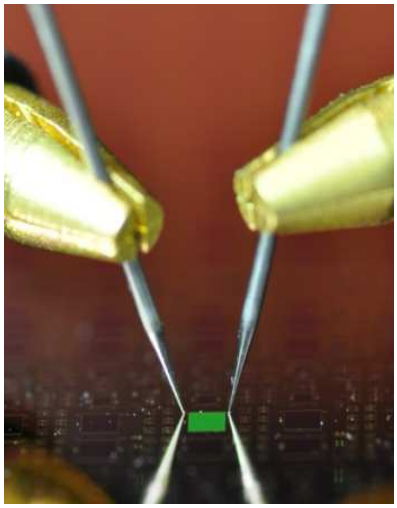
Lastly, two different experiments in AC polarization have been performed. The first one has been done polarizing the gate with a negative voltage applied and connecting the source and the body with a square waveform signal. The second one, instead, polarizing the source with a positive applied bias and connecting to the AC signal the gate and the body. These experiments have been done in order to try to reproduce the Walters experiments [65], [48]. In all the performed measurements, we have never seen an increase of the electroluminescence signal, both changing the voltage and the frequency values. In all the cases, we do see electroluminescence from defects in the matrix or from the bulk silicon, but not an enhancement of the luminescence coming from the Si-NCs. We believe that these results are the best that we can obtain with such devices that operate at higher voltages than the one required in order to have a real working device compatible with the silicon photonics scenario.

3.4.4 LEFETs summary

Light emitting field effect transistors, with an active region composed by an alternating structure of silicon nanocrystals and silicon dioxide, have been tested by means of electrical, optical and electro-optical characterization. The samples under study have different values of silicon content excess and different values of the silicon oxide barrier thicknesses. The devices paired by the similar percentage of silicon excess show similar results. From the performed measurements, we can observe that the increase of the silicon excess per layer does not improve the opto-electrical properties. The better suggestion in order to build an efficient light emitting field effect transistor is the combination of low percentage of silicon excess with thinner silicon oxide layers. These two factors together allow a better growth of the nanocrystals and a narrow size distribution. The unipolar injection of the electrons is the main excitation mechanism in these devices, in which the impact excitation dominates. The measurements using an alternating current scheme have shown an increase in the efficiency of the devices.

Chapter 4

Erbium Doped Silicon Nanocrystals Light Emitting Devices



Visible light emission from a device with silicon nanocrystals and Er^{3+} ions. The devices have been fabricated at the CEA-LETI center in Grenoble.

In this chapter, erbium implanted silicon rich silicon oxide based light emitting devices are presented. The investigation and the study of the optical and the electrical properties of the LEDs under direct current and alternating current schemes are studied in order to understand the injection mechanisms and estimate the energy transfer between the silicon quantum dots and the erbium ions. A detailed study of the role of the silicon excess and of the silicon dioxide barrier thickness is here reported. At the end of the chapter, the best active material will be chosen in order to fabricate erbium doped silicon nanocrystals based optical cavities, which will be the topic of the next chapter. The erbium doped silicon nanocrystals light emitting devices are labelled as Si-NCs:Er LEDs.

4.1 Si-NCs:Er LEDs: Design and fabrication

4.1.1 Sample layout: design and active material splitting

A schematic figure of the light emitting devices layout is shown in Figure 4.1, which presents also a zoom on the chosen active material layer. The layout of the mask is the same presented in the previous chapter (see Figure 3.1). The active material optimization, in terms of photoluminescence intensity and coupling efficiency between the Er^{3+} ions and the silicon quantum dots, has been performed on a series of monitor wafers. All the details about the active material optimization and the photoluminescence measurements can be found in the reference [36]. The samples used are thin Er^{3+} doped (by ion implantation) films of alternating silicon rich silicon oxide (SRO) and SiO_2 layers deposited on a crystalline silicon wafer by low pressure chemical vapor deposition (LPCVD) in a standard CMOS line. Thin films (d ~ 50 nm) have the advantage that can be studied by electrical [68], optical [69] and optoelectronic means [70]. For example, deposition starts with a d = 2 nm thin SiO_2 layer deposited on p-type crystalline silicon wafer on top of which is deposited a d = 3 nm thick SRO layer with nominal silicon excess of 20 at. %. The procedure is repeated ten times in order to reach the desired thickness of d ~ 50 nm for optimum performance. A d = 2 nm thin layer of SiO_2 is finally deposited on top. After the deposition, the samples are thermally treated in order to induce phase separation and amorphous silicon nanoparticles growth and formation (the annealing temperature is 900°C for 1 hour) [71]. Subsequently, the samples are implanted with erbium ions (dose: 1 x 10^{15} at./cm^2 and energy: 20 keV) and thermally treated for a second time ($T_{post\text{-}annealing}$ = 800°C for 6 hours) in order to recover the implantation damage. Table 4.1 presents the composition of all the fabricated LEDs, highlighting the differences in the active material layers. The symbols in the table are the same explained in the previous chapter for Table 3.3.

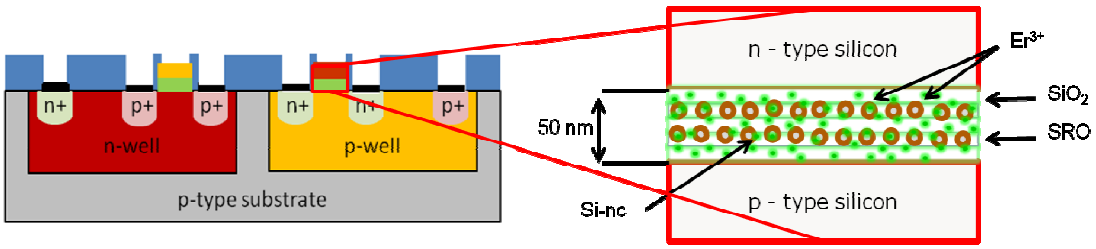


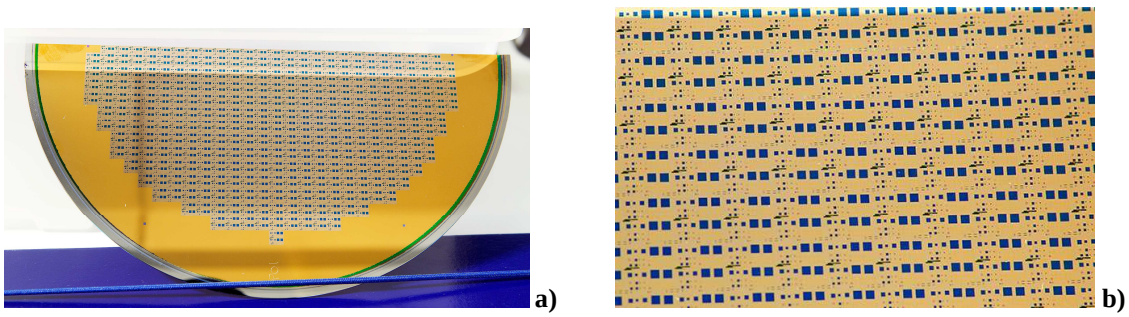
Figure 4.1. **(left)** Er-doped Si-NCs LED layout. **(right)** A schematic zoom of the Er-doped Si-NC active material structure, SRO stands for silicon rich silicon oxide.

Active layer composition	Wafer									
	W8	W9	W10	W11	W12	W13	W14	W15	W 16	W17
LPCVD 50 nm 12%	■									
LPCVD 50 nm 16%		■								
LPCVD ((2 nm 0% + 3 nm 20%) x 10) + 2 nm 0%			■							
LPCVD ((2 nm 0% + 3 nm 25%) x 10) + 2 nm 0%				■						
LPCVD ((2 nm 0% + 4 nm 20%) x 8) + 2 nm 0%					■					
LPCVD ((2 nm 0% + 4 nm 25%) x 8) + 2 nm 0%						■				
LPCVD ((3 nm 0% + 3 nm 20%) x 8) + 3 nm 0%							■			
LPCVD ((3 nm 0% + 3 nm 25%) x 8) + 3 nm 0%								■		
LPCVD ((3 nm 0% + 4 nm 20%) x 7) + 3 nm 0%									■	
LPCVD ((3 nm 0% + 4 nm 25%) x 7) + 3 nm 0%										■
Furnace annealing 900°C 1 h	■	■	■	■	■	■	■	■	■	■
Er implantation 10^{15} cm^{-2} @ 20 keV	■	■	■	■	■	■	■	■	■	■
Post-implantation annealing 800°C 6 h	■	■	■	■	■	■	■	■	■	■

Table 4.1. Composition of the active layer of the Si-NCs:Er LEDs.

4.1.2 Sample fabrication and structural analyses

The samples have been fabricated in a standard complementary metal-oxide-semiconductor (CMOS) line in Grenoble, at the CEA/Léti Minatec center. Figure 4.2 shows a photograph of a fabricated wafer, with in evidence a zoom on a single chip. As shown in the picture, on the chip there are several LEDs, with different active areas. All the measurements reported in this chapter have been performed on light emitting devices with a square active area of 300 µm x 300 µm.



a) **b)**

Figure 4.2. Photographs of the fabricated 6” wafer **(a)** and of a zoom on the different dies **(b)**.

For transmission electron microscopy (TEM) JEOL 2010-FEG (200kV) scanning transmission electron microscope was used, equipped with a GIF spectrometer for the Energy-Filtered Transmission Electron Microscopy (EFTEM) imaging mode. The samples for the TEM observations were prepared through conventional mechanical polishing with a final Ar^+ bombardment using PIPS Gatan system. The TEM analysis has been performed at the University of Barcelona. Erbium concentrations has been determined by secondary ion mass spectrometry (SIMS) calibrated with a sample of known erbium concentration. The silicon excess was calculated with the formula (1 - x/2)/(1 + x), with x equal to the ratio of the oxygen concentration and the silicon concentration as measured by X-ray photon spectroscopy (XPS). The erbium concentration profile in our fabricated thin films has been determined by SIMS and it is reported in Figure 4.3 (a). The peak concentration, N_{peak}, equal to 5.2 x 10^{20} at./cm^3, is located in the centre of the active layer, at approximately ~ 20 nm below the sample surface. The average erbium concentration is $N_{average}$ = 2.9 x 10^{20} at./cm^3. A silicon excess of 9 % was determined by XPS. The thickness of the active material d ~ 44 nm was found by TEM. The TEM image of the sample is reported in Figure 4.4, with in evidence the total thickness of the active layer and the localization of the Er^{3+} clusterization. Note that the Er^{3+} concentration in our sample was chosen based on previous reports which indicate long lifetimes and high emission intensities, i.e. no cooperative photoluminescence quenching effects [53]. Erbium clusters are visible as a dark spotted layer in TEM image (see Figure 4.3 (b)). This erbium cluster layer is located at d ~ 20 nm below the sample surface and it is approximately 15 nm wide (see both the Figures 4.3 (b) and 4.4). It contains the (55 ± 5) % of the total number of erbium ions (shaded area in the Figure 4.3(a)). This is a first insight on what could limit the Er^{3+} emission capability as the clustered erbium ions emit light very inefficiently [72]. However, not all of the Er^{3+} in this layer may be clustered and, on the other hand, due to the finite resolution of TEM, the erbium clustered region could be wider, as small erbium clusters (formed by a few atoms only) may escape detection. It is worth mentioning that similar local inhomogeneity in erbium ions spatial distribution and tendency to clusterize in silicon rich oxide films have been reported previously in thin films prepared with very different deposition techniques [73], [74]. Thus, this type of behavior is not inherent to the LPCVD technique, but it is quite general for Er^{3+} concentrations larger than 10^{20} at./cm^3. In the following sections of this chapter, I will present the opto-electrical results obtained in these samples and we will see how this erbium clusterization affects the optical performances of our LEDs.

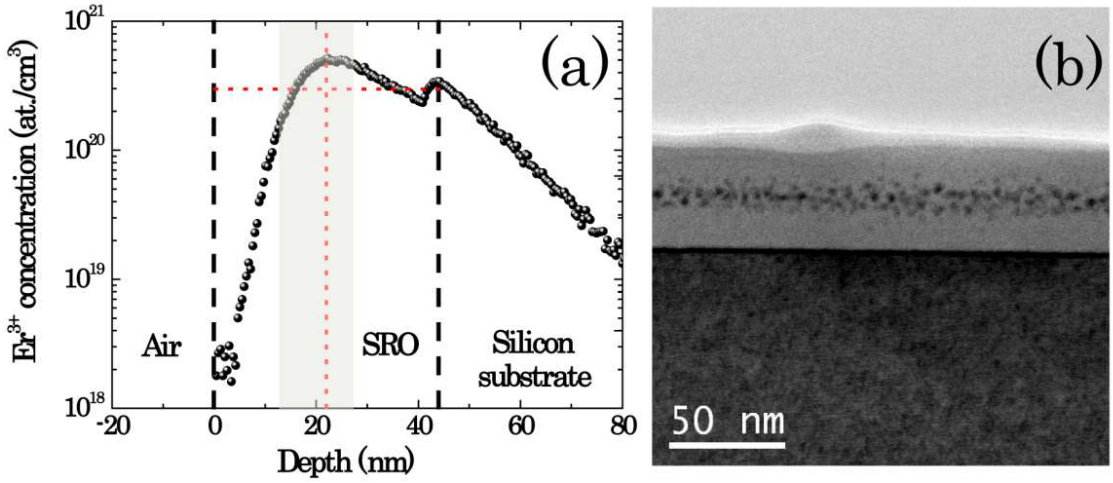


Figure 4.3. **(a)** Semi-log plot of Er^{3+} concentration profile in the studied samples obtained by SIMS. Thick vertical dashed lines indicate interfaces between air/SRO and SRO/ silicon substrate. Vertical red dotted red line corresponds to the peak Er^{3+} concentration and the horizontal red dotted red line to an average Er^{3+} concentration in the active layer. The shaded area corresponds to the layer where erbium clusters are visible in TEM images. **(b)** Bright field scanning TEM image of the sample W10[1].

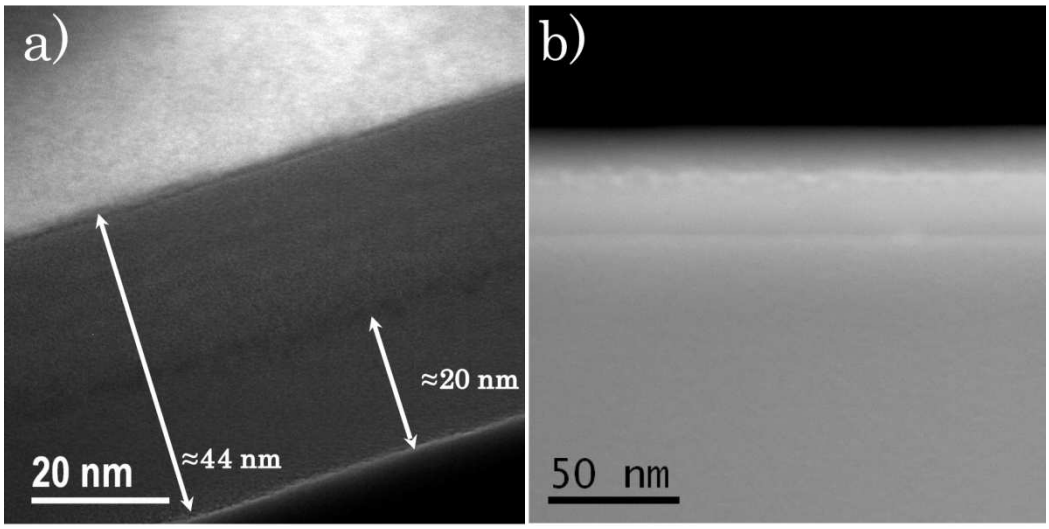


Figure 4.4. **(a)** Energy filtered TEM (EFTEM) image of the sample W10. This image has been obtained by filtering at 15 eV (c-Si plasmon peak). **(b)** High angle annular dark field TEM image of the sample W10.

The Er^{3+} emission can be observed in our samples both by non-resonant (see Figure 4.5 (a) - λ_{exc} = 476 nm with an excitation photon flux $\Phi_{exc} = 3 \times 10^{20}$ ph./cm^2) and, by resonant optical excitation. The electrical excitation, both under DC and AC conditions, will be the object of my study and it will be discussed respectively in the sections §4.2 and §4.3. In Figure 4.5 (b), it is reported as well a visible photoluminescence (PL) spectrum under CW UV optical excitation (λ_{exc} = 364 nm, Φ_{exc} =

[1] The TEM images were performed at the Laboratory of Electron Nanoscopy at the University of Barcelona.

3 x 10^{18} ph./cm^2). The broad PL band in Figure 4.5 (b) situated at λ = 750 nm is attributed to residual Si-NCs PL. The additional peak at 550 nm, which is observable only under UV optical excitation or electrical bias, could be associated with direct excited state emission ($^4S_{3/2}$ – $^4I_{15/2}$) radiative Er^{3+} transition visible due to its high emission cross section. Moreover, the presence of cooperative up-conversion (CUC) processes are observed by the shortening of the lifetimes of the 1.535 μm Er^{3+} emission with increased excitation photon flux.

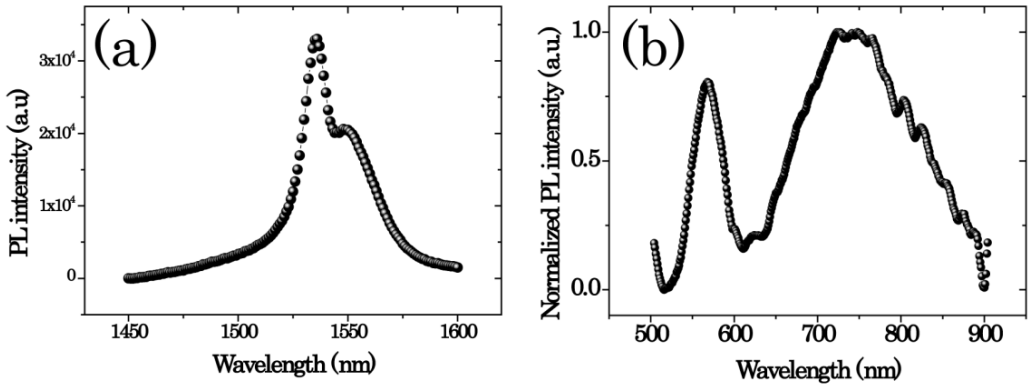


Figure 4.5. **(a)** PL spectrum of the $^4I_{13/2}$ – $^4I_{15/2}$ radiative erbium transition in the studied sample under non-resonant optical excitation. **(b)** Normalized visible PL spectrum under CW UV optical excitation.

Before starting with the physical analysis of the phenomena and the injection mechanisms, I have performed some tests for the homogeneity of the LED fabrication across the 200 mm silicon wafer. Figure 4.6 shows the electroluminescence (EL) intensity and its variation as a function of the applied voltage for 40 different Si-NCs:Er LEDs of the wafer W8. This plot shows a good uniformity of the chips fabricated among the same silicon wafer. We will see in the following of the thesis that this reproducibility of the measurements among different chips on the same wafer will be a critical issue, because of some fabrication problems occur during the fabrication of the optical cavity sample batch.

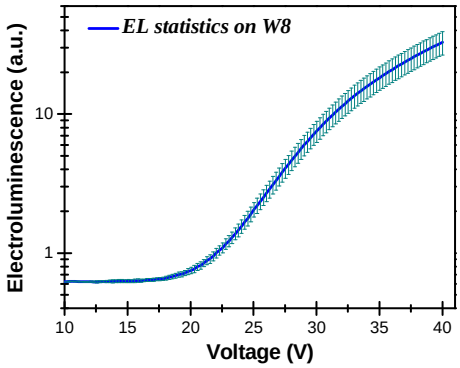


Figure 4.6. EL as a function of the applied voltage for W8. The small error bars show a good homogeneity of the Si-NCs:Er LEDs fabrication on the 200 mm silicon wafer.

The EL intensity has been measured at randomly selected locations on the wafer. Small error bars indicate a good homogeneous growth of the silicon nanocrystals layer across the wafer.

4.2 Si-NCs:Er LEDs: Opto-Electrical Characterization in DC

4.2.1 Single Layer vs. Multilayer

The multilayer approach in the growth of the silicon nanocrystals composite material allows the independent control of the nanocrystals size and density [75]. After a high-temperature annealing, the thickness of the SRO layer in the multilayer structure determines the nanocrystals size, while the excess silicon content of the SRO layer determines the nanocrystals density. In addition, a tight control over the silicon oxide layer quality and thickness which separates the silicon quantum dots in the multilayer structure is possible. These features are enough to create an easy recipe in order to engineer the band gap energy of the Si-NCs via thickness/composition profiling of a multilayer SRO/SiO_2 structure. In this section, a comparison between different Si-NCs:Er LEDs, based or on a single or on a multilayer structure, in terms of light emitting power efficiency and external quantum efficiency of the erbium ions, is reported. Figure 4.7 shows the layout of the studied device and Table 4.2 shows a summary of the devices analyzed in this section. I will compare three different multilayered devices with a single layer device, which has the same silicon content excess of one multilayer wafer. The basic structure studied is a MOS capacitor, in which the gate oxide is replaced by the erbium doped silicon nanocrystals based layers.

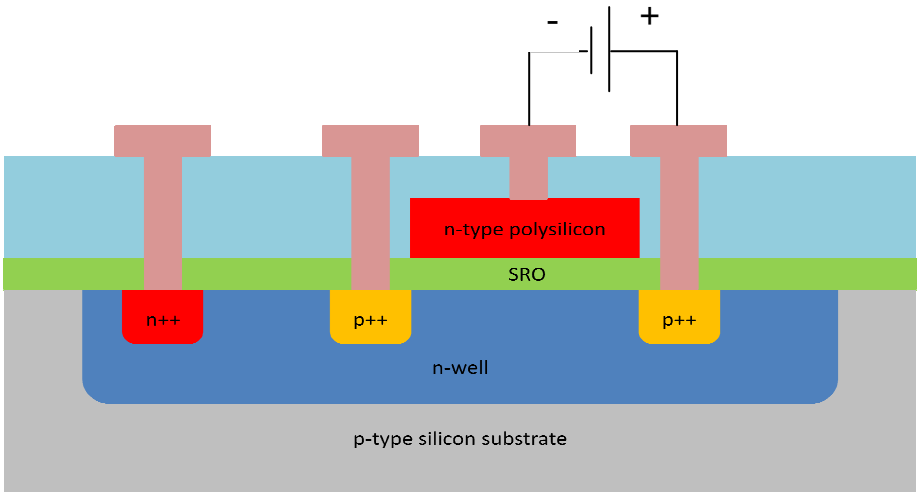


Figure 4.7. Device description: the cross-section is a MOS capacitor, in which the gate oxide is replaced by Er^{3+} ions sensitized silicon rich silicon oxide.

Device	Structure	Er-implanted matrix	Si excess
W10	Multilayer	LPCVD (2 nm 0% + 3 nm 20%) x 10	11.5 %
W11	Multilayer	LPCVD (2 nm 0% + 3 nm 25%) x 10	14.4%
W13	Multilayer	LPCVD (2 nm 0% + 4 nm 25%) x 8	16%
W8	Single layer	LPCVD 50 nm	12 %

Table 4.2. Summary of the devices under study in this section.

The light emitting diodes under study have low silicon content excess and, hence, low conductivity, which means high operating voltages. In direct current (DC) regime, the Er^{3+} ions are excited by impact excitation, as high energy transitions of erbium has been clearly observed in the visible region of the spectra. Figure 4.8 shows the electroluminescence spectra as a function of the applied voltage both in the visible and in the infrared (IR) wavelength regions. On the top of the figure, the Er^{3+} transitions are reported. The main excitation mechanism is the impact excitation done by hot electrons, because of the high voltage applied. In the visible wavelength range, we do see the lines of the erbium emission corresponding to high energetic transitions. The high applied voltages are required because of both the silicon dioxide barrier and the erbium ions clusterization. The erbium transition at 580 nm tells us why we do see the LED emitting in the green (see Figure in the introduction of the chapter). Figure 4.9 shows the integrated electroluminescence intensity of the peak in the IR region as a function both of the applied voltage and of the injected current. In the plot shown, it is reported only for W10, which is the best multilayer sample under study, and for W8, in order to do a comparison between the single layer and the multilayer Si-NCs:Er LEDs. In fact, both W8 and W10 active materials have the same thicknesses (about 50 nm) and about the same average silicon content excess. We found larger voltages for the multilayered devices. However, both the devices presented here show very similar electroluminescence intensities. Starting from this point, the power efficiency, defined as the ratio between the optical power and the electrical power (see Table 1.1), in the IR has been evaluated and reported in Figure 4.10 as a function of the injected current. The most important result is that the multilayers have allowed increasing the power efficiency of the devices by about 1.5 times with respect to the single layer ones. The maximum value of power efficiency achieved is 1.5×10^{-2} %, referred to W10 at an injected current of 100 nA.

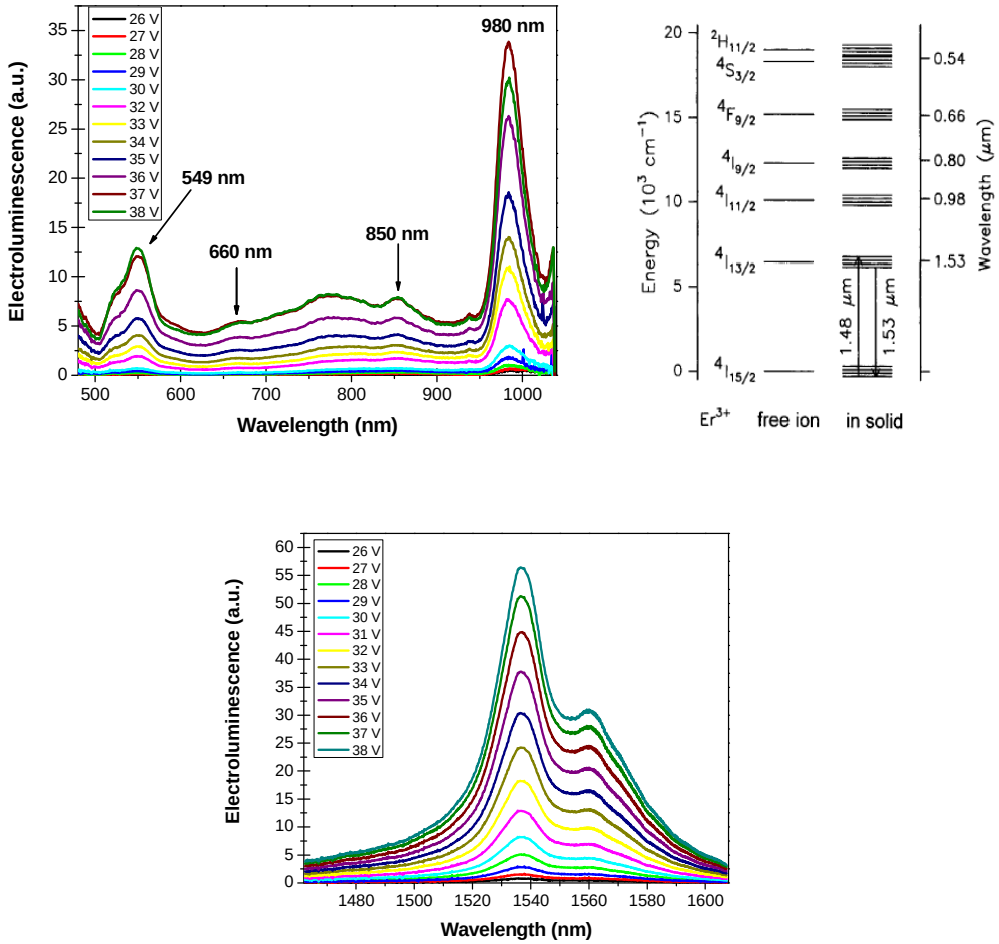


Figure 4.8. Electroluminescence emission at 1.54 μm **(bottom)** and in a visible range **(top-right)** of a 300 x 300 μm^2 n-type MOS LED at several applied voltages, which are indicated in the legend. Arrows with the numbers shows the Er^{3+} emission peak wavelengths – see the transitions diagram **(top-left)**. The spectra are normalized to the spectrometer response.

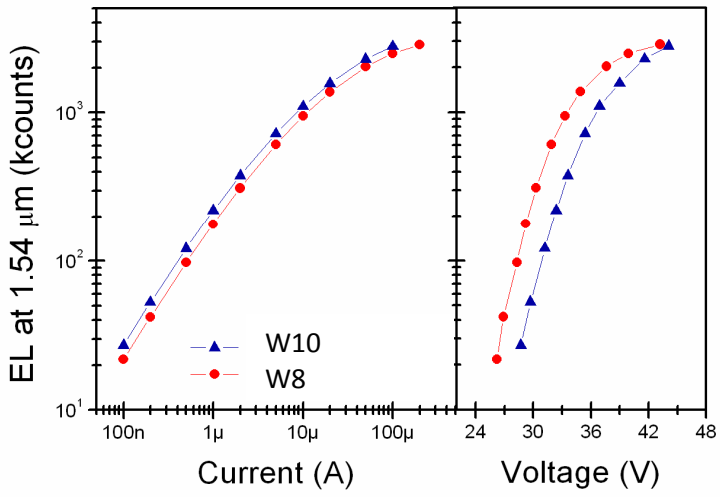


Figure 4.9. Electroluminescence behavior as a function of the injected current and the applied voltage for a multilayer (blue) and a single layer (red) light emitting diode.

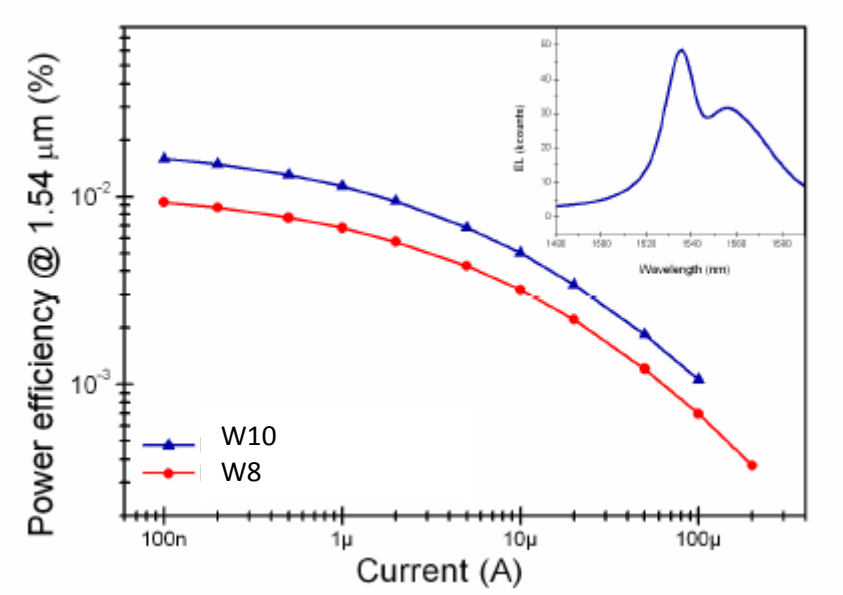


Figure 4.10. Power efficiency as a function of the injected current for a multilayer (blue) and a single layer (red) LED. In the inset, an example of the IR EL spectrum at 1.54 µm for W10 is shown (at an injected current of 50 µA).

Figure 4.11 shows the external quantum efficiency as a function of the injected current for the different multilayer LEDs with different thicknesses of oxide and SRO, which means different concentration of silicon nanocrystals and different silicon content excess values. As shown in the plot, the maximum value of E.Q.E. is achievable in W10, and it is equal to 0.4 %, which is one of the higher values reported in the literature. The maximum value reported in such devices is 1% [76], but we have to take in mind the fabrication problems occur in our devices.

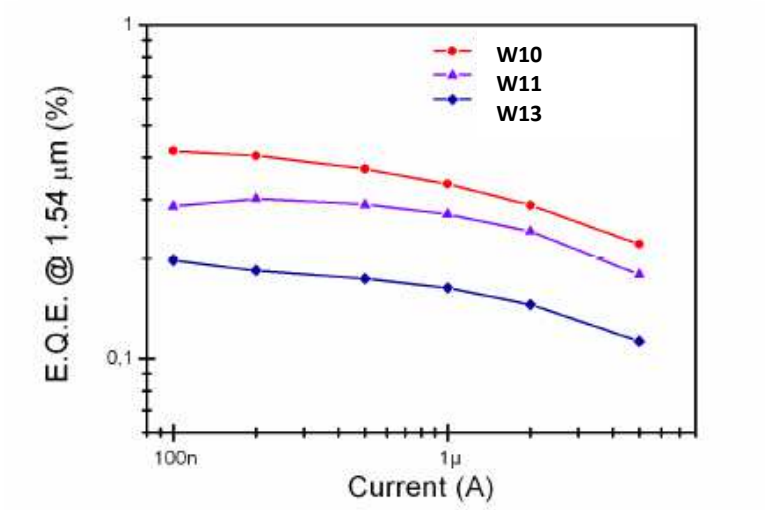


Figure 4.11. E.Q.E. as a function of the injected current for P1, P2 and P3.

The best result has been obtained on the multilayer with the lowest silicon content excess value and this fact suggests us that more studies need to be performed on the role of the silicon content excess in the multilayered devices.

4.2.2 Role of silicon content and oxide barrier thickness in MLs devices

The study presented in this section has been done on all the multilayered devices presented in the samples batch. Referring to Table 4.1, the study has been done on the samples W10-W17. This study is important in order to chose the best parameters for the fabrication of a silicon nanocrystals erbium doped based optical cavity (*§ Chapter 5)*. The n-type CMOS Si-NCs:Er LEDs are excited with an electric signal under direct current (DC) condition in accumulation regime, applying a negative voltage over the n-type gate electrode, with the p-type substrate grounded. This configuration is the most convenient because we drive the device under the forward bias condition. The injected current under both accumulation and inversion regimes is shown in Figure 4.12 for a single n-type MOS capacitor. In this plot, is shown the current-voltage (I-V) characteristic for W10. Similar characteristics have been measured in the other devices. Again, as the I-V shown in Figure 3.6, there is a big hysteresis loop, originated from the charge accumulation at the interfaces. The current density versus the electric field plot (J-E plot) can be well fitted by the Fowler-Nordheim (F-N) expression. This fact could be predictable, because of the high bias voltage, which has to be applied to the devices in order to have a detectable EL.

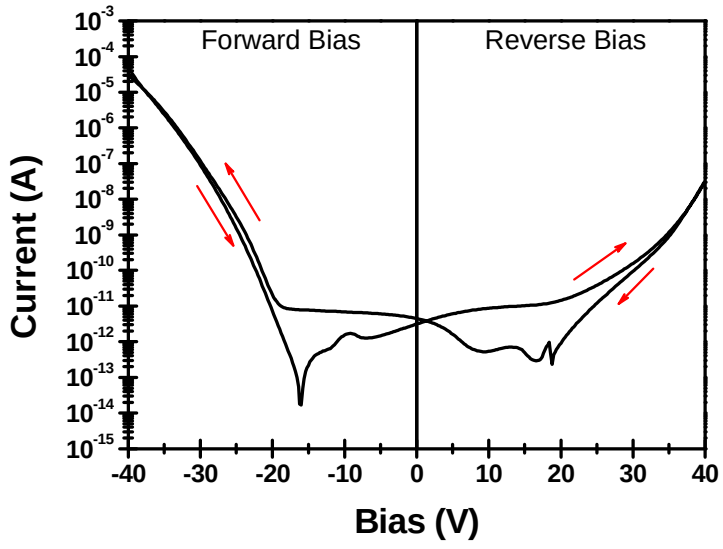


Figure 4.12. I-V characteristic of W10. The arrows show the bias scanning direction during the measurements.

Figure 4.13.a shows the J-E plots for all the devices under study, while Figure 4.13.b is showing the F-N barrier height (ϕ_B), extrapolated from fitting the plot with the Fowler-Nordheim expression, as a function of the silicon content excess. It can be easily underlined that there is a correlation between the silicon excess, the oxide layer thickness and the F-N barrier height. The barrier height decreases with the increase of the silicon excess.

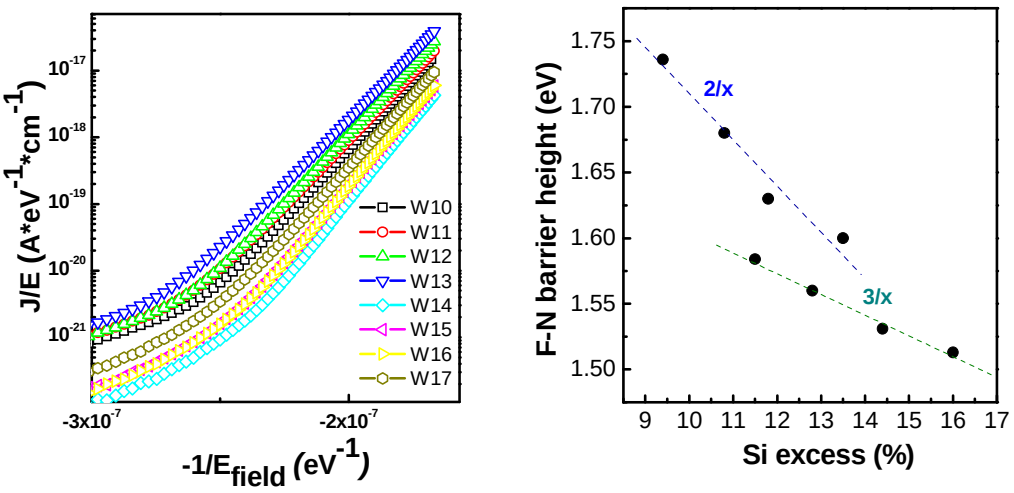


Figure 4.13. **(left)** Fowler-Nordheim fit for all the multilayered devices under study and **(right)** F-N barrier height as a function of the silicon content excess. The F-N barrier height differs between the devices with 2 nm thick of SiO_2 barriers (called 2/x samples in the plot) and the ones with 3 nm thick barriers (3/x samples in the plot).

Figure 4.14 (top) shows the infrared EL intensity as a function of the silicon excess in different multilayered devices at a fixed injected current of 1 μA, with silicon content excess in the range between 9% and 16%. Extrapolating the EL intensity dependence on the silicon excess to zero values gives us a higher value of the E.Q.E. than the one measured in the Er^{3+}-doped LPCVD and thermal silicon dioxide. The same value of E.Q.E. is reached at about 6% of silicon excess. The figure also shows (right axis, red symbols) that lower operating voltages are achievable with higher silicon excess and/or thinner silicon oxide scaffold that confines the Si-NCs. These LEDs can operate at lower voltages and emit at around 850 nm. Figure 4.14 (bottom) shows instead the infrared EL intensity as a function of the silicon excess in different multilayered devices at a fixed applied voltage of 32 V. As shown in the figure, two groups of devices can be clearly distinguished. The EL signal intensity differs between the devices with 2 nm thick of SiO_2 barriers and the ones with 3 nm thick barriers. This fact confirms our hypothesis that the main injection mechanism is the unipolar one and that the most important parameter

for understanding the injection in our Si-NCs:Er LEDs is the voltage and not the current. This fact can be clearly correlated to the F-N injection mechanism and to the energy of the electrons (since the voltage is more related to the energy than the current).

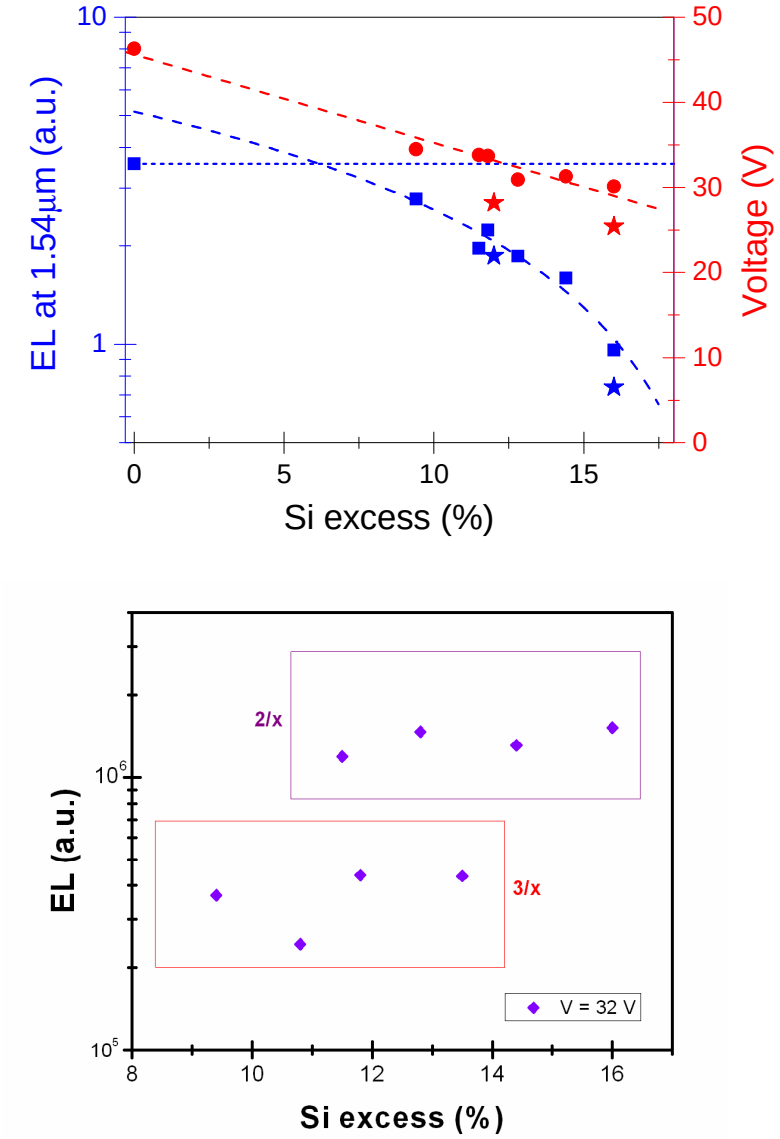


Figure 4.14. Integrated EL as function of the silicon content excess, evaluated at a fixed injected current of 1 µA **(top)** and at a fixed applied voltage of 32 V **(bottom)**.

In conclusion, the electroluminescence behaviour as a function of the silicon content excess confirms that, increasing the Si excess, the IR emission decreases. All the results presented in this section and in the previous one confirm that the multilayers have allowed increasing the power efficiency roughly by 1.5 times with respect to the single layer devices. However, there is still the problem of high operating voltages both for the single and the multilayers Si-NCs:Er LEDs. This problem can only be solved with a new samples batch, which was not possible because of the ending of the HELIOS project.

4.3 Bipolar pulsed excitation of the Si-NCs:Er LEDs

The energy transfer mechanism between silicon nanocrystals and erbium ions is well documented under optical excitation. Walters et al. [49] and Peralvarez et al. [77] demonstrated sequential injection of electrons and holes into Si nanocrystals under the bipolar pulsed excitation of Si-NCs LEDs. Priolo et al. suggested this excitation scheme as a solution to overcome nonradiative Auger de-excitation of Er^{3+} in Si-NCs:Er^{3+} LEDs [78]. Miller et al. calculated a modal gain of 2 dB/cm in a slot waveguide confined Si-NCs:Er^{3+} under the pulsed excitation which mitigates excited carrier absorption [79]. In this section, we will evaluate the erbium excitation mechanisms and emission in the Si-NCs:Er^{3+} LED under electrical pumping using both direct current and bipolar pulsed excitation schemes, i.e., when the polarity of the applied voltage pulse is periodically changed. In particular, we will compare two different LEDs, one based on the silicon nanocrystals and one codoped with the Si-NCs and the erbium ions. The schematic layout of the n-type CMOS LED is shown in Figure 4.15. The direct current bias polarity convention is also reported in the figure.

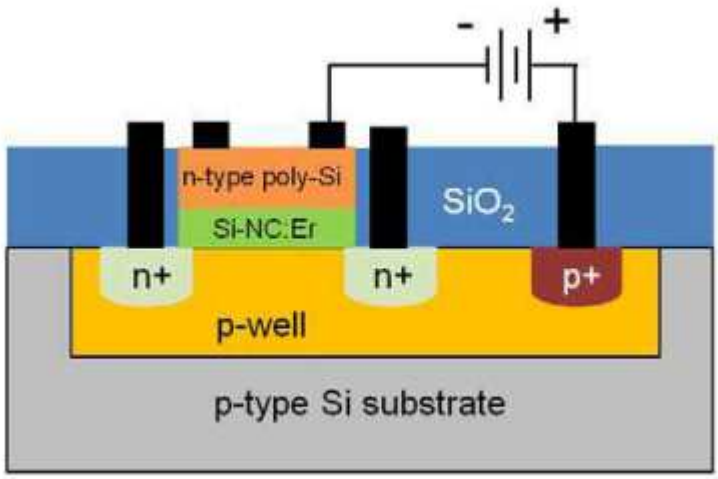


Figure 4.15. A schematic cross section of the n-type CMOS Si-NCs:Er LED layout. Green color stands for the Er^{3+} doped silicon nanocrystals layer, blue – oxide, and black – titanium-aluminum-copper metal contact sandwich.

4.3.1 Direct current excitation

Electrical charge transport in our Si-NCs LEDs is due to electric field-enhanced tunneling of electrons with the involvement of either defects or confined energy states of Si-NCs [80], [81]. Erbium implantation produces deep energy trapping levels which

change the transport properties of the Si-NC LED [82]. This is supported by the DC I-V and C-V characteristics shown in Figure 4.16. The I-V curves of both the Si-NCs and the Er-doped Si-NCs LEDs are shown in a voltage range where EL signal is observed under forward bias (Si substrate is in accumulation). EL emission is also observed under reverse bias in both undoped and doped Si-NC LEDs, but at higher voltages and with lower quantum efficiency. The I-V curves are well described by the Fowler-Nordheim field-enhanced tunneling law with effective energy barrier heights of 1.4 and 1.9 eV for Si-NCs and Si-NCs:Er LED, respectively (assuming an effective electron mass of 0.3 m_0) [83]. The Er-doped device is less conductive than the undoped device, which we ascribe to charge trapping at deep energy levels due to Er ion implantation. This is also supported by the C-V measurements (see Figure 4.16). A hysteresis loop is observed in the C-V curves, which is due to charge trapping. The hysteresis is wider for the Er-doped Si-NCs LED than for the undoped Si-NCs LED. Trapped charge density estimated from C-V hysteresis width of the Si-NC LED is 4.3×10^{12} cm^{-2}. Assuming one trapped electron per Si-NCs, this value serves as a good estimate of the Si-NCs area density [84].

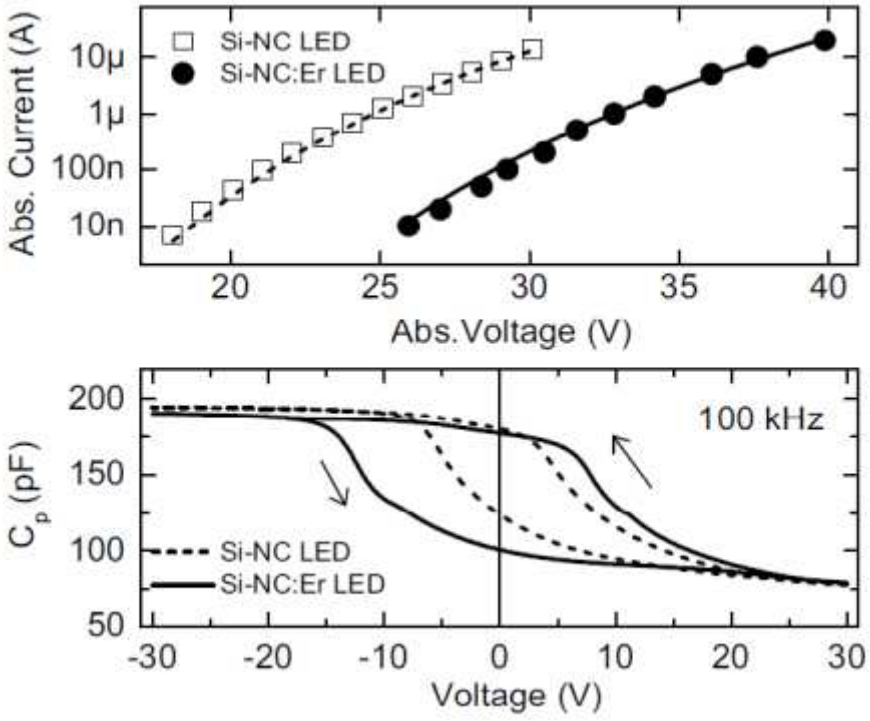


Figure 4.16. **(top)** Forward I-V characteristics of Si-NCs and Si-NCs:Er LEDs. Symbols are experimental data values at which the EL is observed, lines are fits to the Folwer-Nordheim tunneling law. **(bottom)** C-V characteristics of the Er3+ doped and undoped Si-NCs LEDs. The signal frequency is 100 kHz. The arrows show the bias scanning direction during the measurements.

Figure 4.17 (top panel) shows the integrated spectral EL intensity of the Si-NCs and the Si-NCs:Er LEDs as a function of injection DC current in the visible range and at wavelengths bracketing the 1.54 µm Er emission, respectively. For low injection currents, EL intensity at 1.54 µm increases linearly with the DC current. However, at high currents a sublinear growth with injected current is observed. On the contrary, the visible emission from Si-NCs increases almost linearly (with a slope of 0.91±0.01 in the log-log coordinates) as a function of the current. The saturation of the 1.54 µm emission may be attributed to both a limited amount of optically active Er ions and to the onset of non-radiative recombination processes [85]. The presence of the last ones is highlighted by the decrease of the luminescence decay time shown in Figure 4.18.

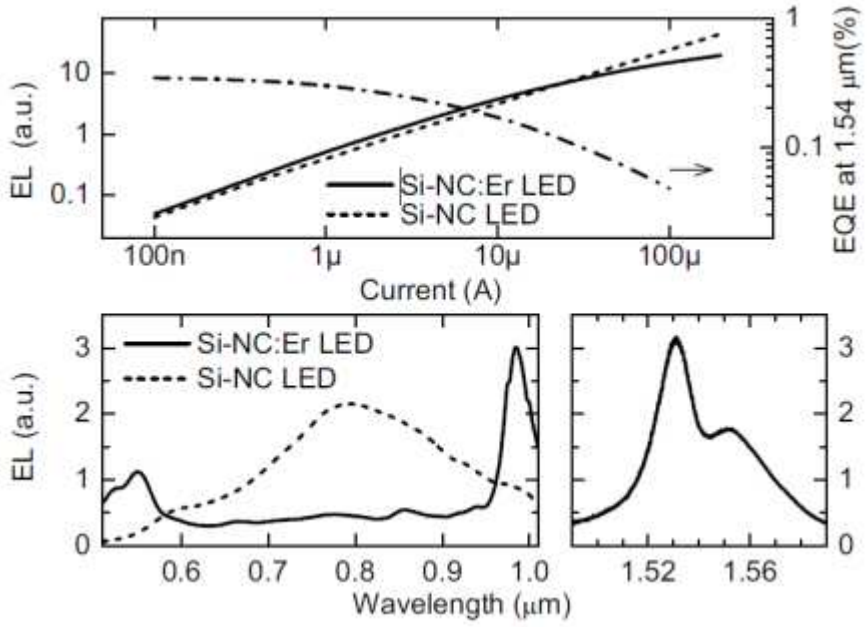


Figure 4.17. **(top)** Integrated EL spectral intensity with wavelengths bracketing 1.54 µm (left axis, solid line) and in the visible range (left axis, dot line) for Si-NCs:Er LED and Si-NCs LED, respectively, as a function of DC injected current. Please note that absolute values of the EL intensity in the visible and IR ranges are not to compare (the y-axes are not the same). The dash-dot line shows the corresponding E.Q.E. values at 1.54 µm (right axis). **(bottom)** EL spectra at the injected current of 2µA.

Figure 4.17 also shows the E.Q.E. of Er-doped Si-NCs LED emitting at 1.54 µm. It is noteworthy that these E.Q.E. values are among the best values reported so far for the Er-doped silicon LED (see for example Refs. [86], [87]). The EL spectra of the Si-NCs LED and of the Si-NCs:Er LED for a same injected current of 2 µA are shown in the bottom panel of Figure 4.17. The emission of the Si-NCs LED is characterized by a broad peak centered at around 770 nm, which originates from excitonic recombinations into the Si-

NCs. The Si-NC:Er LED emission spectrum shows in addition to the broad Si-NC emission several sharp peaks at around 550, 660, 850, 980, and 1535 nm due to the excited Er^{3+} states emission (presence of the peaks at 660 and 850 nm is more evident at higher currents). It has to be noted that the green emission at 550 nm is not due to the Er up-conversion because the peak intensities of the various emission bands increase linearly as the injection current increases. The linear increase is observed in a broad range of currents up to 20 μA. At larger currents, we observed some signs of the cooperative up-conversion. High driving voltages along with the presence of the multiple Er^{3+} peaks indicate that Er^{3+} emission is mainly due to direct impact ionization of Er^{3+} ions and not to indirect Er^{3+} excitation via energy transfer from the Si-NCs. On the other side, the energy transfer between Si-NCs and Er^{3+} ions cannot be completely ruled out since the Si-NCs emission peak is much weaker in the Si-NC:Er LED than in the undoped device.

Another argument for the interaction between the Er^{3+} and the Si-NCs is the value of the excitation cross-section of the Er^{3+} itself. This can be estimated by measuring the exponential rise and decay time of EL [78], [88]. This evaluation could be explained by taking into account a nearly two level system. Starting from the dynamic rate equation:

$$\frac{dN_2}{dt} = \sigma \frac{j}{e}(N_{total} - N_2) - \frac{N_2}{\tau_{decay}}$$

with

$$\frac{1}{\tau_{decay}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{non-rad}}$$

where σ is the effective absorption cross section, J is the incident current density, e the single electron charge, τ_{decay} is the total lifetime (radiative - τ_{rad} - and non-radiative - $\tau_{non-rad}$), and N_{total} and N_2 the total implanted and the excited Er^{3+} ions in the first energy level, respectively. Also, knowing that the electroluminescence is proportional to $N_2/\ \tau_{decay}$, the following relation can be obtained [53]:

$$\frac{1}{\tau_{rise}} = \frac{1}{\tau_{decay}} + \sigma \frac{j}{e}$$

being σ the absorption cross section of the luminescent centers.

The result is shown in Figure 4.18. The excitation cross-section value extracted from the data is $(5 \pm 2) \times 10^{-14}$ cm^2. Note that the evaluation is based only on the rise and decay times for driving voltages larger than 30 V.

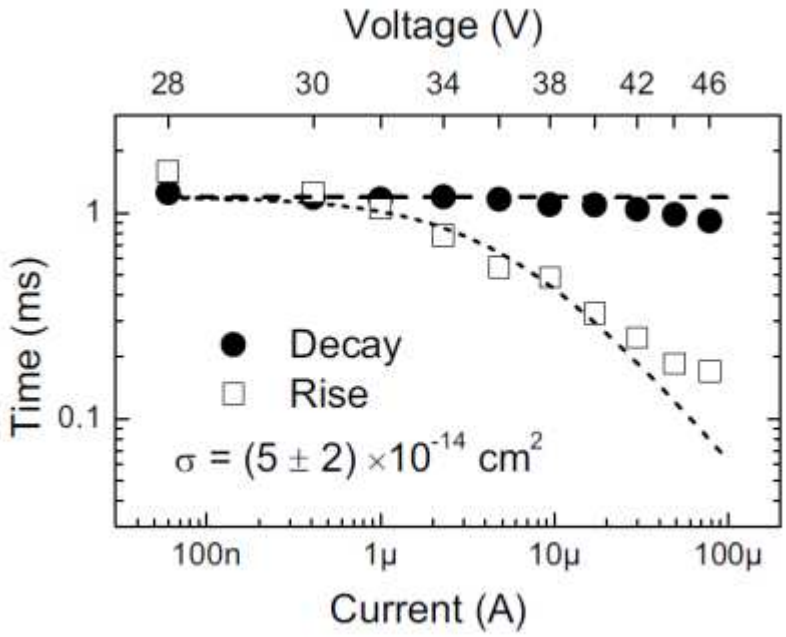


Figure 4.18. Exponential decay and rise times of an integrated EL spectral intensity in IR as a function of LED driving voltage (top x-axis) and the corresponding current taken from the DC I-Vs (bottom x-axis). Measurement uncertainty is smaller than the symbol sizes. The Er^{3+} excitation cross-section value estimated from the data is $(5 \pm 2)x10^{-14}$ cm^2. The lines are fitted functions with a constant value of the decay time of 1.2 ms and an excitation cross-section value of $5.9x10^{-14}$ cm^2.

For lower driving voltages, the 1.54 μm EL rise time exceeds (1.20 ± 0.02) ms, which is equal to the EL decay time. We also note that the EL decay time is similar to the measured 1.54 μm photoluminescence (PL) lifetime of (1.31 ± 0.05) ms. We measured an excitation cross-section value which is larger than the known value of direct impact excitation of Er^{3+} in SiO_2, $(6 \pm 2) \times 10^{-15}$ cm^2 [89], and which is close to the indirect Er^{3+} excitation cross-section value for Er^{3+} coupled to the Si-NCs. It is noteworthy that the decrease in the decay lifetime only moderately accounts for the decrease in E.Q.E. shown in Figure 4.17. Saturation of optically active Er^{3+} concentration might account for the rest of this decrease. Summarizing, the results of the DC excitation presented in this section suggest that the electrical current is due to electron tunneling mediated by Si-NCs in the Si-NCs LED and Er^{3+}-related defects in the Si-NCs:Er LED. They also show that Er^{3+} is primarily excited by impact of high energy electrons. The impact of holes is believed to be small because of a negligible hole current due to the larger valence band offset of Si and Si-NCs than the conduction band offset [90].

4.3.2 Bipolar pulsed excitation

Figure 4.19 shows the spectrally integrated EL intensity at 770 nm and 1.54 μm as a function of the driving frequency, f, for a bipolar pulsed excitation scheme. Here the LEDs are driven by varying the bias periodically and rapidly (within ~400 ns) from forward to reverse and from reverse to forward with a square waveform at a frequency f. At low driving frequencies, f << 1 kHz, the EL intensity at 1.54 μm (bottom panel in Figure 4.20) decreases a little with the frequencies for high driving voltages and increases for low driving voltages, being much weaker for the low bias. As the driving frequency approaches 800 Hz, which corresponds to the inverse of Er^{3+} emission lifetime, the EL intensity decreases (increases) for high (low) bias. In a frequency range f >> 1 kHz, which we name a moderate frequency range, it changes only slightly for both the high and low bias. This behavior is accompanied by an increase of the peak EL intensity at 770 nm (see Figure 4.19, top panel; high bias). It should be noted that the onset frequency of this increase is around 800 Hz unlike the undoped Si-NCs LED where the EL starts to significantly increase above 10 kHz. The EL decay lifetime of Si-NCs is around 5 μs (measured by both PL and EL), which corresponds to a frequency of 200 kHz. These high frequencies are not available with our instruments so that the lifetime of Si-NCs does not limit the EL intensity in the studied frequency range.

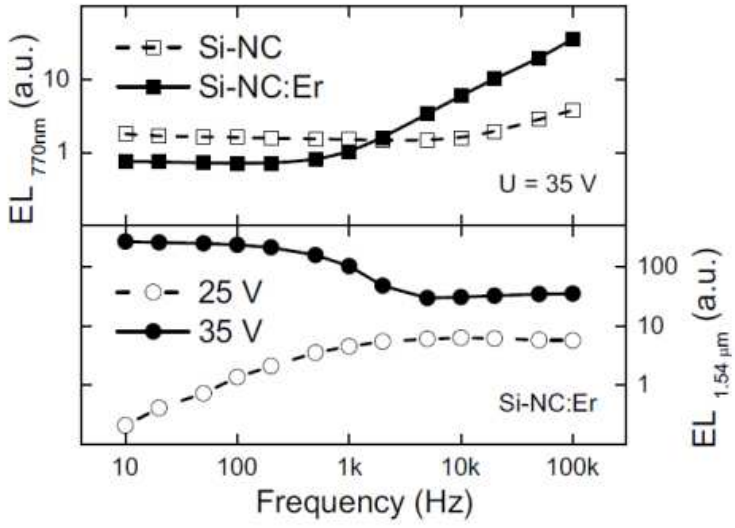


Figure 4.19. **(top)** Peak EL intensity at 770 nm as a function of bipolar-pulse driving frequency with a fixed RMS voltage of 35 V for both Si-NCs and Si-NCs:Er LEDs. **(bottom)** Integrated EL spectral intensity in a wavelength range bracketing 1.54 μm as a function of bipolar-pulse driving frequency at a fixed RMS voltage of 25 and 35 V for the Si-NCs:Er LEDs. The meaning of the different symbols is stated in the figure legend.

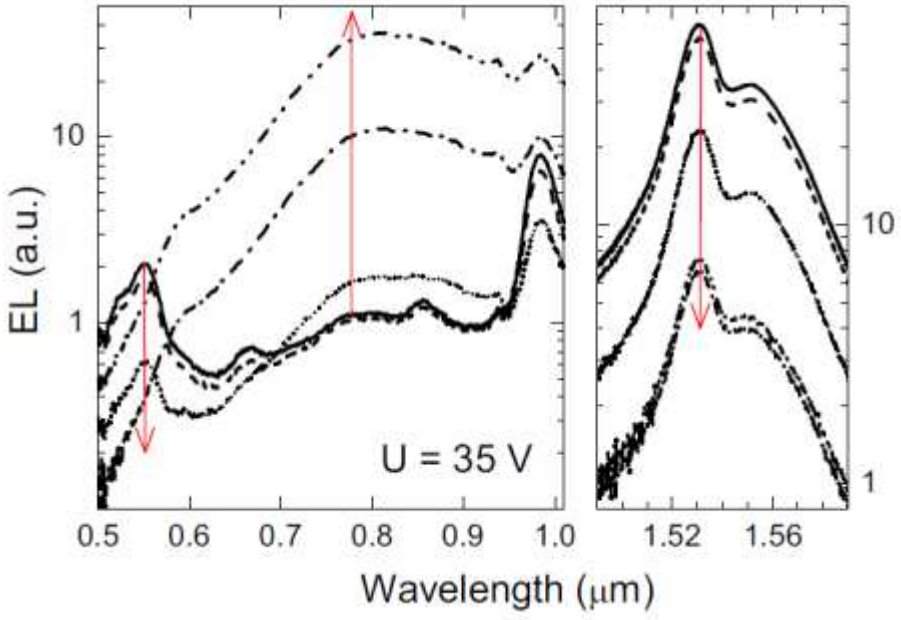


Figure 4.20. The electroluminescence spectra at 10, 100, 1k, 10k, and 50 kHz for the Si-NCs:Er LEDs shown in Figure 4.19. The ascending frequency order is indicated by the red arrows.

The frequency dependence of the EL intensity is reflected in evident changes of the Si-NCs:Er LED spectral characteristics, which are shown in Figure 4.20. The multiple excited Er^{3+} states emission peaks weaken and the peaks at 550, 660, and 850 nm disappear at the moderate frequencies. The Si-NCs emission peak emerges. We attribute these changes to a change in the dominant excitation mechanism of Er^{3+} ions: from electron impact to the energy transfer between Si-NCs and Er^{3+} ions. Under the pulsed excitation scheme, sequential injection of electrons and holes into Si-NCs takes place at the bias transitions. More efficient injection into Si-NCs at high injection frequencies provides additional indirect Er^{3+} excitation by means of the energy transfer at the bias transitions. This explains an increase of the Er^{3+} emission at 1.54 μm with injection frequency at low voltages (no emission by impact). Note that in these samples only ~1% of the total Er^{3+} population is coupled to the Si-NCs, which was obtained using optical excitation. Therefore, it is this 1% of Er^{3+} ions which shows an increased excitation due to a better energy transfer from the Si-NCs. If the injection frequency is smaller than the Er^{3+} emission rate of about 800 Hz, both Si-NCs and Er^{3+} are in relaxed states and follow the frequency. If the excitation frequency is higher than the Er^{3+} emission rate (while still smaller than the Si-NC emission rate of 200 kHz), Er^{3+} stays in an excited state and further excitation is limited by non-radiative processes.

The fact that the energy transfer between Si-NCs and Er-ions becomes a dominant Er^{3+} excitation mechanism at the moderate frequency range is further supported by the voltage dependence of EL intensity at 1.54 µm shown in Figure 4.21. The voltage dependence is stronger for low than for moderate injection frequencies. It is important that the EL signal in the moderate frequency range is observed at lower driving voltages than in DC or low frequency excitation, namely the onset of EL was measured at around 18 V_{RMS} (see Figure 4.21). Beyond this value, the charge trapping in the oxide arrests EL. The energy transfer remains the main excitation mechanism of Er^{3+} up to about 36 V_{RMS} at moderate frequencies. This is supported by the EL spectra shown in the bottom panel of Figure 4.21. There are no Er^{3+}-related peaks at wavelengths below 980 nm at low-to-moderate voltages, while an Er^{3+} peak centered at around 550 nm is observed at 38 V_{RMS}. At high voltages, for example around 36 V_{RMS}, and moderate frequencies, the EL emission is dominated by impact excitation. Table 4.3 summarizes the obtained results in a broad range of excitation frequencies and voltages in terms of a dominant excitation mechanism of Er^{3+}-ions under electrical pumping.

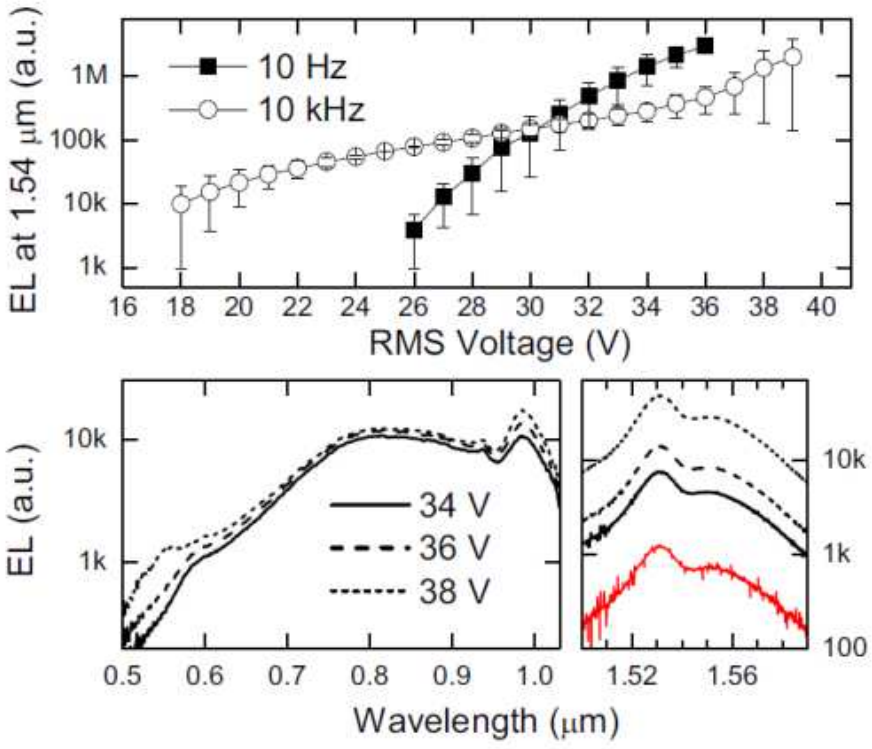


Figure 4.21. EL intensity at 1.54 µm as a function of RMS voltage under bipolar pulsed electrical excitation for two driving frequencies of 10 Hz (squares) and 10 kHz (circles). The low panels show EL spectra at 34, 36, and 38 V_{RMS} at 10 kHz. Notice an appearance of the Er^{3+} emission band at 550 nm at 38 V. The lowest red line at the right is the EL spectrum for 30 V_{RMS} at 10 Hz. No light emission was detected in the visible region at 30 V_{RMS} and 10 Hz.

	Low frequency, f < ~ 1 kHz	**Moderate frequency, 1 kHz << f < 200 kHz**
Low voltages, U < 25 V	N/A	Transfer
Moderate voltages, 25 V < U < 36 V	Transfer and Impact	Transfer
High voltages, U > 36 V	Impact	Impact

Table 4.3. Er^{3+} excitation mechanisms. Low frequency stands for driving frequencies lower than the Er emission rate, moderate frequency – frequencies higher than the Er emission rate, but lower than the EL decay rate of the Si-NCs.

In conclusions, energy transfer between the Si-NCs and the erbium ions becomes a dominant excitation mechanism of Er^{3+} ions in a moderate-to-high frequency range of square waveform electrical excitation, at which sequential injection of electron and holes takes place. This allows driving the Si-NCs:Er LEDs at significantly lower voltages and using small duty cycles. When bipolar charge injection is achieved in DC, the Er^{3+} excitation will be via the energy transfer as in the luminescence processes.

4.4 Conclusions

Erbium doped silicon nanocrystals based light emitting devices have been designed and fabricated at the CEA-LETI, in Grenoble. The most important results obtained in the characterization of different sample batches can be summarized as following:

- Both single layer and multilayer structures of Si-NCs:Er are used as the active light emitting material. The multilayers have allowed increasing the power efficiency roughly by 1.5 times with respect to the single layer devices;
- Optimized Si-NCs:Er LEDs have 0.5% of external quantum efficiency at low current densities and show a hundred microwatts per square centimeter of optical power density at the wavelength of 1.54 μm;
- Both direct and alternating current excitation schemes of the Si-NCs:Er LEDs have been studied. We have found that the Er^{3+} ions are excited mainly by impact of high energy electrons under direct current excitation. However, a change in Er^{3+} excitation mechanism is observed under a pulsed excitation when sequential injection of electrons and holes into the Si-NCs takes place. This change, which is due to the coupling between Si-NCs and Er^{3+} ions, allows us to drive the Er-doped Si-NCs LEDs with significantly lower voltages than in DC;
- The optimized active material of Er-doped Si-NCs is a multilayer structure with 2 nm of silicon dioxide and 3 nm of SRO. This active material has to be used in erbium doped silicon nanocrystals based optical resonator structures.

Chapter 5

Erbium Doped Silicon Nanocrystals Optical Cavities

In this chapter, I will speak about erbium implanted silicon rich silicon oxide based optical cavities. A complete optical and electrical characterization is presented, with in evidence a comparison between a sample with the silicon quantum dots and a samples without it. The possibility to have optical gain and to use this device as an optical amplifier, by means of electrical pumping, is here investigated. At the end of the chapter, experimental measurements on Er^{3+} doped ring resonator are reported and some future perspectives which could be done in order to have optical gain in such devices.

5.1 The mask layout

A new mask layout, different from the one presented in the previous chapter, has been designed and it is shown in Figure 5.1. The die is divided into three different regions. One region is dedicated to the ring resonator structures. 27 different structures are present and they are the combinations of three waveguide widths, three ring radius per waveguide width and three coupling distances per ring radius. Another region is dedicated to the Fabry-Perot cavities. Six different structures are present and they are divided in three different waveguide widths and two cavity length per waveguide width. The third region is dedicated to the test structures. In that region, erbium doped silicon nanocrystals based slot waveguides of different widths and lengths are present in order to estimate the waveguide propagation losses. Structures composed by a series of bend with different waveguide widths and radii are used to estimate the bend losses. Several other structures

are dedicated to the electrical tests in order to evaluate the contact resistivity in the lateral and longitudinal directions.

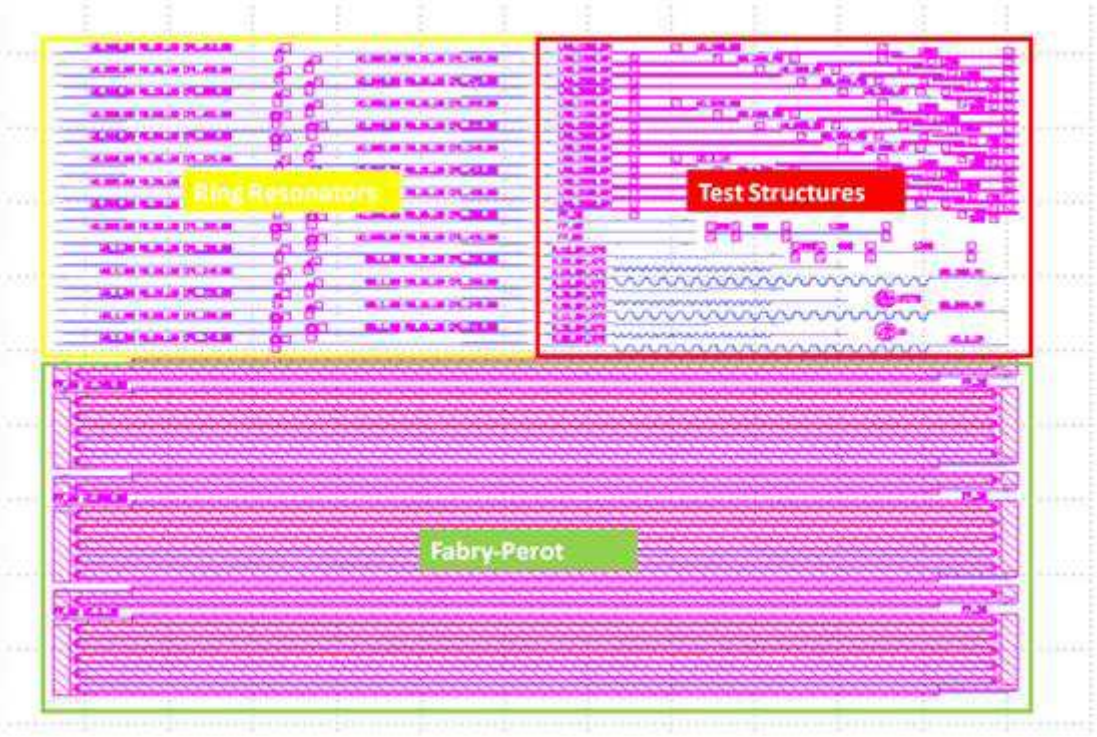


Figure 5.1. Die layout of the new designed mask.

Figure 5.2 shows a picture of a zoom on the different dies on a fabricated wafer, in which we can see the three different regions reported before in the design and here effectively fabricated. In the first section, I will present the results on the slot waveguides, while in the second one the characterization of the ring resonator. Every section will be divided in design, simulation and experimental characterization with the description of the used setups.

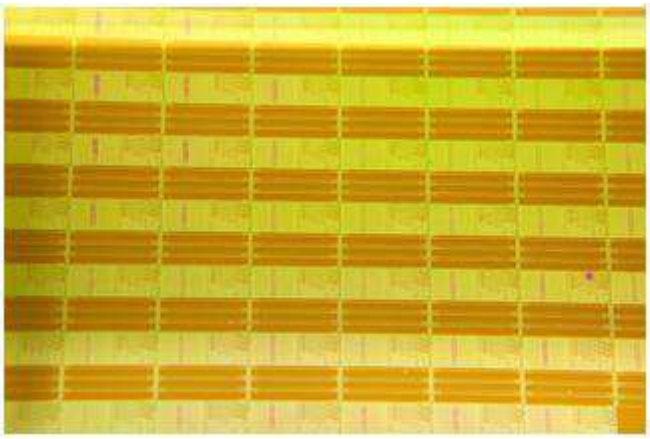


Figure 5.2. Photograph of a zoom on the different dies on a fabricated wafer.

5.2 Si-NCs:Er slot waveguides: Design and Fabrication

In this section, I will describe the design, the simulation and the active material splitting chosen. Moreover, the fabricated samples and the experimental setup will be reported. The novelty of the experimental setup is the convergence of photonics and electronics within a single chip, with the two probes for the electrical contacts and the two infrared tapered fibers for the optical signals, all adapted in a standard commercial electronics probe station.

5.2.1 Sample layout: design and simulation

The slot waveguide scheme has been demonstrated that can offer the possibility of electrical injection and can increase the light confinement in the gain region [91]. This waveguide configuration enables to concentrate a large fraction of the guided mode into a thin low index material layer (slot) sandwiched between two high-index strips. In our case, the slot waveguides are formed by two thick silicon layers separated by a thin (~ 50 nm) erbium doped silicon rich silicon oxide layer, where most of the optical mode can be confined. There are two possible slot orientations that could be considered for the realization of a slot waveguide based amplifier: vertical and horizontal [92] [93]. In the vertical configuration, significant optical losses may be induced by slot wall roughness [94]. Although significant progresses have been made recently [95], multi-layered material deposition on side walls remains a rather challenging task even by the conformal growth [94]. On the contrary, horizontal slot Er^{3+} doped SRO structures, which might also consist of alternating layers of SRO and SiO_2, are easier to deposit and process [96]. Therefore, we opt for a horizontal slot configuration. In this configuration, field enhancement effects due to the slot waveguide geometry are observed for transverse magnetic TM polarization only. While very precise control of device dimensions can be achieved by using electron beam lithography, optical lithography is preferred for industrial applications and mass production. Unfortunately, electrically driven devices have a very complex design, involving multiple lithographic patterning steps [97]. Thus, special attention has to be paid in order to relax optical alignment constrains between different mask levels. Another relevant issue is the choice of the slot wall material. Polycrystalline silicon (polysilicon) or amorphous silicon can be used [98]; polysilicon being better suited for electrical-injection devices due to a better electrical mobility. This motivates our choice of a polycrystalline silicon top cladding. Low optical losses in

polysilicon can be achieved by long high temperature annealing in the presence of hydrogen [98]. However, this may be impractical as it may interfere with optimum thermal budget for Er^{3+} doped SRO films and causes dopant out-diffusion. Therefore, to reduce the optical losses it is more convenient to minimize the fraction of the light guided in the polycrystalline part, while still maintaining a high fraction of field in the slot region. This can be achieved by an asymmetric geometry of the slot waveguide (see Figure 5.3.a). The asymmetric geometry still allows for a large field fraction in the slot region while minimizing the field in the polysilicon top cladding layer (see Figure 5.3.b and Figure 5.3.c). The slab character of the polycrystalline silicon top cladding allows for extremely easy lithographic patterning of electrodes since the top polysilicon width does not influence critically the optical waveguiding in the TM polarization. The structure optimization (layer thicknesses) has been performed with a commercially available fully vectorial mode solver based on film mode matching (FMM) method (FIMWAVE, Photon Design). The structure optimization and the optical mode simulations have been done by Nikola Prtljaga. The whole structure is defined on commercially available SOI wafer with a 220 nm thick silicon layer on the top of a buried oxide (2 µm thick).

The active material thickness in the slot was fixed to 50 nm, an optimum value for a slot waveguide amplifier [99], [79] and a maximum value for which efficient electrical injection in multilayer samples has been demonstrated [68], [100]. In his work, Miller reports a maximum Er^{3+} modal gain of 2 dB/cm in a slot waveguide with 50 nm thick active material [79]. The waveguide width of 1µm has been chosen in order to increase the active material volume. For this width the fundamental TM mode displays high confinement in the slot region (see Figure 5.3.a), while the higher order modes exhibits high radiative losses and, practically, do not contribute to light propagation. The thicknesses of the top cladding and bottom electrodes, which form side slabs named wings in the following, have been chosen in order to maintain good electrical conductivity while still inhibiting the mode leaking towards the wings (see Figure 5.3.a and Figure 5.3.b). Moreover, as the optical field does not penetrate in wings, doping can be increased providing good electrical contacts. Additionally, the slot parameters chosen for the fabrication are quite robust with respect to fabrication induced variations, including the changes of active material thickness or refractive index (different silicon excess, thermal treatments, see Figure 5.4).

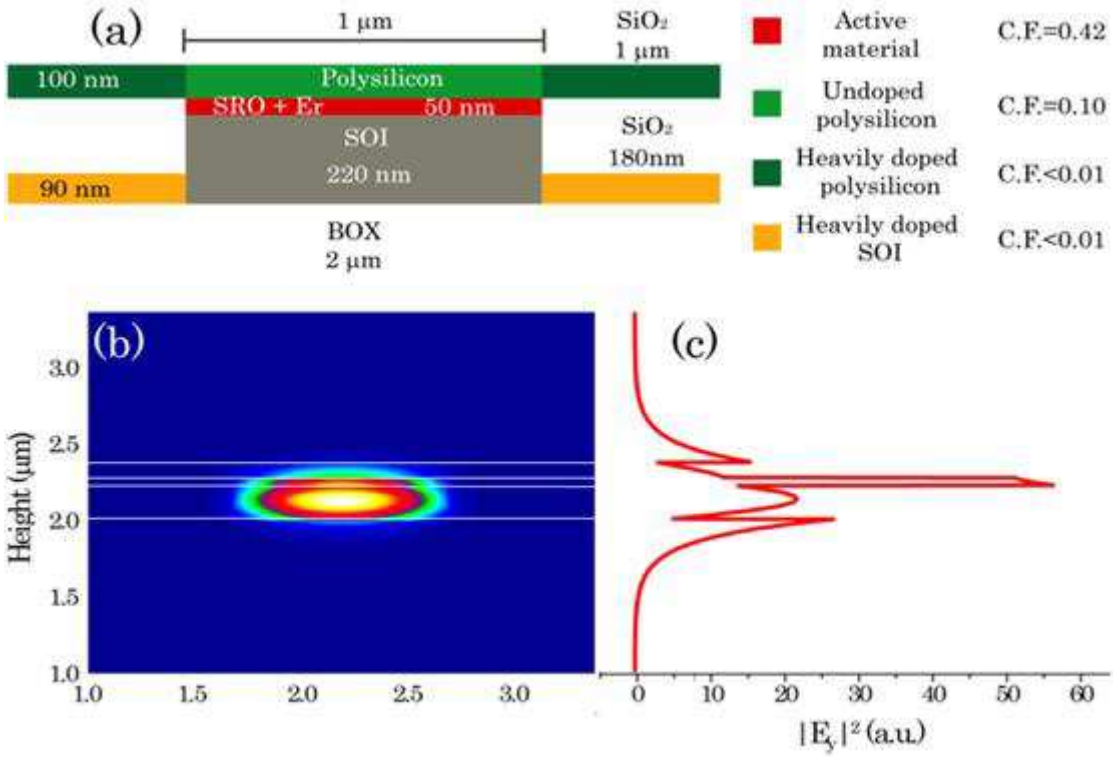


Figure 5.3. **(a)** Schematic of the asymmetric slot waveguide for electrical injection. C.F. stands for confinement factor which gives the fraction of the optical electric field in the indicated area. **(b)** Intensity profile of the fundamental TM mode. **(c)** Vertical electric field profile of the fundamental optical TM mode.

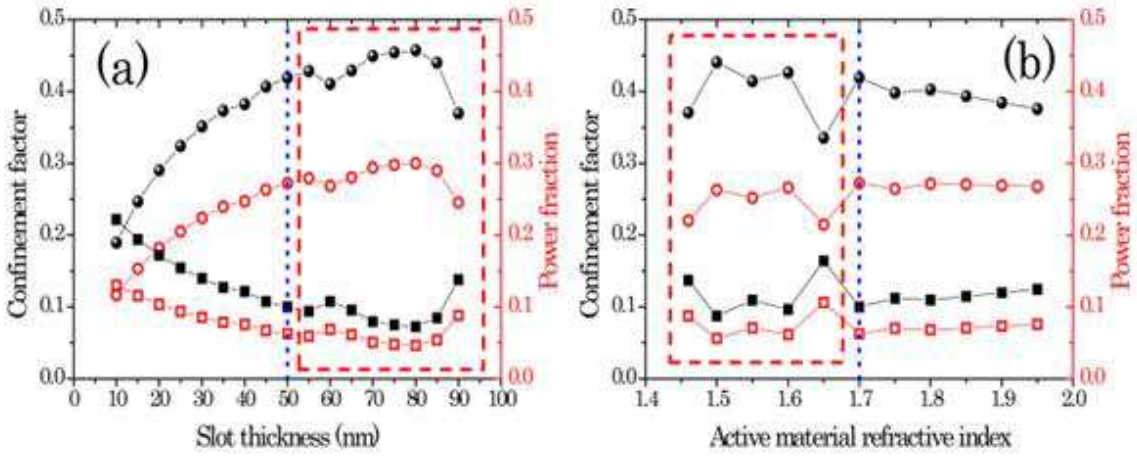


Figure 5.4. Confinement factor (black full symbols) and power fraction (red empty symbols) of the fundamental TM mode in the slot region (circles) and polysilicon top cladding (squares) as a function of **(a)** active material thickness and **(b)** active material refractive index. Vertical blue dotted line indicates nominal parameters. Red dashed square indicates the range of parameters for which fundamental TM mode experiences additional radiative losses due to "leaking" towards the waveguides "wings".

5.2.2 Sample layout: devices fabrication and experimental setup

The waveguides have been fabricated on SOI wafers in a 200 mm CMOS pilot line of the CEA, Lèti. The schematics of the typical process flow are reported in Figure 5.5. Commercially available SOI wafers with 220 nm of lightly doped p-type Silicon (Si) layer on a 2-μm-thick buried oxide (BOX) were used for device manufacturing. The device layer was implanted with boron to form a concentration gradient, with high concentration near the BOX and light doping in the proximity of the surface ($10^{17}/cm^3$). The active layer with a thickness of 50 nm was grown on Si (see Figure 5.5.a). It consists either of stoichiometric or non-stoichiometric (silicon rich) oxide. Stoichiometric silicon oxide was an high temperature oxide (HTO) and was used as a reference sample. Silicon rich silicon oxide (SRO) was deposited by low pressure chemical vapor deposition (LPCVD) in a multilayer sequence. A layer of 2 nm of silicon dioxide and a layer of 3 nm of SRO, with a nominal silicon content excess of 20%, were repeated ten times. The gases used are N_2O and silane, only the ratio changes for the SiO_2 and the SRO layers. For the SRO step, the time is 16 minutes and 30 s, with a ratio between the N_2O and the SiH_4 equal to 200/40 sccm, while for the oxide step the time is 26 minutes and the ratio between the gases 960/40 sccm.

A measured overall silicon content excess in the stack of 8.7% was determined *ex-situ* by the x-ray photoelectron spectroscopy (XPS). The active layers were then annealed at 900 °C for 1 hour. This thermal treatment promotes the phase separation and the silicon nanocluster formation in SRO active layer. TEM analysis shows a loss of layering in the annealed film. Erbium was finally introduced by ion implantation with a dose of $10^{15}/cm^2$ and energy of 20 keV. A peak Er^{3+} concentration of $\approx 3.5\times10^{20}/cm^3$ in the centre of the active layer was determined by the secondary ion mass spectrometry (SIMS). Erbium clustering was also observed. The waveguide has been defined by etching 90 nm of the silicon layer on the BOX (see Figure 5.5.b). The waveguide formation is followed by boron implantation into the areas outside the slot region ("wings") and silicon dioxide deposition (see Figure 5.5.c). The post-implantation annealing is performed at 800 °C for 6 hours in order to activate both the Er^{3+} ions and the boron implant. Afterwards, the hard mask on the top of the waveguide surface is removed in a chemical-mechanical polishing/planarization (CMP) steps (see Figure 5.5.d). An undoped top polycrystalline silicon layer 116-nm thick is deposited by LPCVD at 620 °C (see Figure 5.5.e). The top polysilicon layer is doped outside the slot area (wings) with phosphorus to an electron

concentration of $10^{19}/cm^3$. A CMOS compatible Ti/TiN/AlCu metal stack is used for contacts (see Figure 5.5.f). Figure 5.6.a shows the layout of the fabricated waveguides. The real thickness of the active layer is ≈ 40 nm. To couple the light in and out, the waveguides are ended with an adiabatic taper and a grating coupler. The SEM images of cross section of the fabricated waveguide show that the initial design is reproduced in the fabrication.

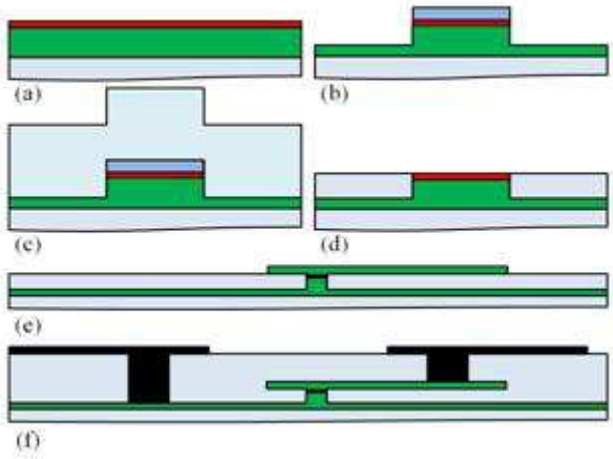


Figure 5.5. Schematic overview of the processing steps for the realization of the Er^{3+} doped electrically driven asymmetric horizontal slot waveguide. **(a)** Deposition on the lightly boron doped SOI wafer (light blue – BOX, green – silicon layer) of the active layer (red - Er^{3+} doped SRO or silica); **(b)** Waveguide definition by a partial 90 nm etch of the silicon layer on the BOX (the blue layer is a mask layer); **(c)** – The bottom electrode in the wings are implanted with boron while the mask layer protect the waveguide core; the whole structure is then covered with an oxide; **(d)** – Excess silica and hard mask (blue) are removed in a CMP (chemical mechanical polishing) step; **(e)** – The top polycrystalline silicon cladding is deposited and defined yielding the slot waveguide; **(f)** – Vias openings and metal deposition define the metal contacts (black), for electrical injection in the slot waveguide.

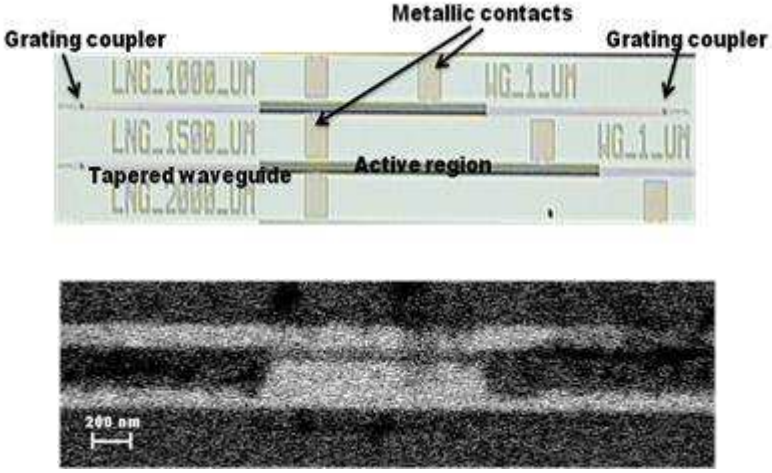


Figure 5.6. **(a)** Top view optical image of the waveguides. Note that Er^{3+} was implanted only in the region covered by the metal line (label active region). **(b)** SEM image of the fabricated

waveguide cross-section. Dark and light regions correspond to silicon oxide and silicon respectively.

In the following sections, the waveguides containing the layer with the Er^{3+} ions in silica will be labeled as Er:SiO_2, while the ones with the silicon nanocrystals will be labeled as Er:Si-NCs. Table 5.1 reports a summary of the devices under study, with in evidence the fabrication parameters. The digit in percent is the silicon excess content.

	P01 – Er:Si-NCs	**P02 – Er:SiO_2**
LPCVD *Multilayer* ((2 nm 0% + 3 nm 20%) x 10) + 2 nm 0%	**X**	
Thermal oxide (50 nm)		**X**
Annealing at 900°C for one hour	**X**	**X**
Er implantation	**X**	**X**
Post-annealing at 800°C for six hours	**X**	**X**

Table 5.1 Fabrication details and summary of the devices under study.

The realized structures have been experimentally characterized, both electrically and optically. The whole setup has been built on a commercial probe station (Suss MicroTec PM8), where both optical and electrical probes have been used. The optical probes have been realized by using single mode tapered fibers facing the gratings with the optimized input angle, which is equal to 25° with respect to the normal (spot diameter of 2.5 ± 0.3 µm at a working distance of 14 ± 2 µm). A photograph of the probes during a measurement is shown in Figure 5.7.

The electrical analysis has been performed using a semiconductor device analyzer (Agilent B1500A). The connections to the device are achieved via triaxial cables, terminated with a sharp probe tip contacts. Optical characterization has been done using two different infrared tunable lasers (NetTest Tunics BT or Santec TSL-210F). The transmitted signal is analyzed with an optical spectrum analyzer (OSA Anritsu MS9710B). To measure electroluminescence, a photon counting module (IdQuantique Id201) is used. As a vision system for alignment purposes, an infrared camera mounted on a microscope has been used.

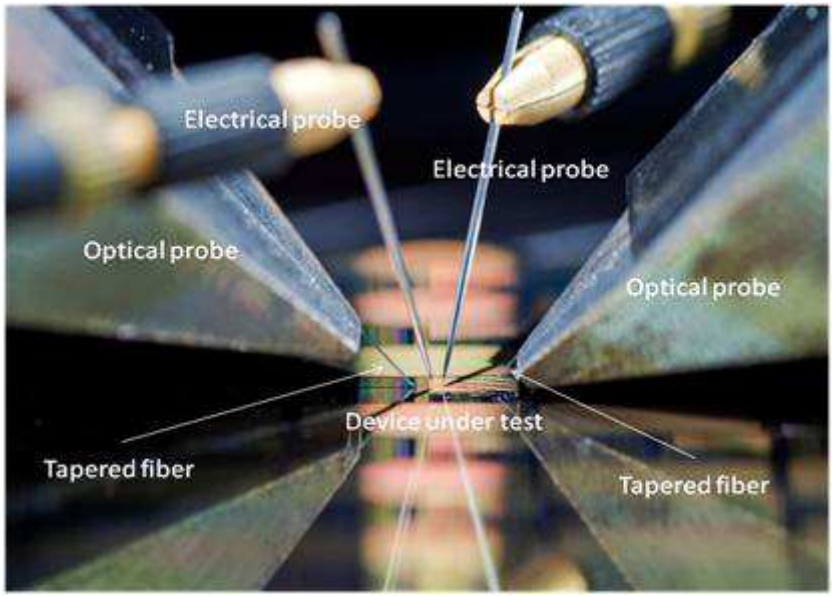


Figure 5.7. Details of the experimental setup. The photograph shows a zoom on the measurement region, with the two probes for the electrical contacts and the two infrared tapered fibers for the optical signals.

5.3 Electrical and optical characterization

5.3.1 Electrical characterization

Current-Voltage (I-V) characteristics show a rectifying behavior with a larger conductivity in the Er:Si-NCs waveguides. In forward bias, the silicon nanoclusters enhance the electrical conductivity, leading to higher currents for the same voltage bias On the other hand, these high currents lead to a low breakdown voltage. In fact, while for the Er:Si-NCs waveguides the maximum voltage is around 40 V, for the Er:SiO_2 devices higher voltage (up to 48 V) can be applied without breaking the device. Similar behaviors have been already observed in light emitting diodes with the same active material, and discussed in the previous chapter.

Figure 5.8.a shows the J (E) characteristics under forward bias of the active slot waveguides for the two slot active materials studied. Forward bias means here that a DC negative voltage has been applied to the n-type doped top electrode. This yields electron injection at the top electrode and hole accumulation at the lower interface. We will not give here details on inversion (reverse bias) characteristics as the currents involved are orders of magnitude lower (rectification) and thus light emission is very poor. As demonstrated in earlier test capacitors of a similar type driven into accumulation, the hole

transport through the slot can be ruled out due to the large energy offsets between the valence bands of silicon and those of SiO_2 or SRO, which are between 4.0 and 4.7 eV. Instead, the band offset for electrons is between 1.6 and 3.1 eV (depending on the silicon excess precipitation). Nevertheless, one expects a certain degree of hole injection and trapping at the lower interface (seen as displacement current) as demonstrated in pulse programming of Si-NCs memories.

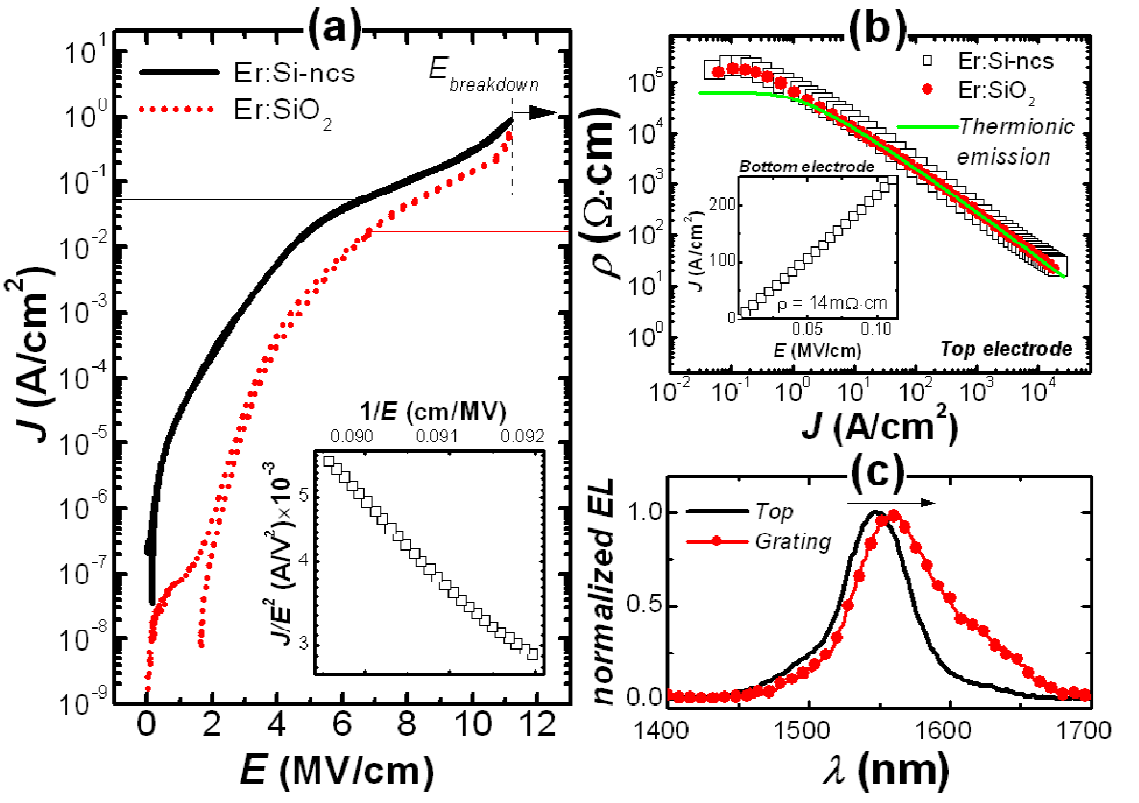


Figure 5.8. **(a)** Current density versus applied electric field J(E) characteristics for the Er:Si-NCs device (solid line) and the Er:SiO_2 device (dotted line) up to device breakdown. Horizontal lines mark the onset of electroluminescence for the two devices. Inset, the Fowler-Nordheim plot for the Er:SiO_2 device. **(b)** Resistivity values of the top electrode for the Er:Si-NCs device (empty squares) and the Er:SiO2 device (filled dots) as a function of the injected current density. The line shows the fit of the data with the thermionic emission model. Inset, J(E) characteristic for the bottom electrode. **(c)** Comparison between the emitted EL spectrum collected from the active waveguide surface (straight line) and from the output grating coupler (dotted lines).

The devices were biased up to device breakdown that was usually between 11 and 12 MV/cm, value which is compatible with a high quality silica layer grown on silicon [101]. The voltage sweeping step was fixed at 10mV/s which is small enough for achieving quasi-static I (V) curves by allowing trap charging/discharging quasi-equilibrium at each step (as seen from the pulsed polarization dynamics of the system). The horizontal lines in the figure 5.8.a represent the current density threshold for EL

emission (red for the Er:SiO_2 device and black for the Er:Si-NCs device). Specifically, the threshold field for light emission was around 6.5 MV/cm for both samples and threshold currents were 64 mA/cm^2 for the Er:Si-NCs device and 26 mA/cm^2 for the Er:SiO_2 device. These values of threshold field correlate with the onset of the Fowler-Nordheim tunneling current, which starts to dominate at around 6 MV/cm. This fact is well in agreement with what reported in the introduction, i.e. see Figure 1.19. We can consider this threshold as a profound modification of the transport properties of electrons through the layer: i) For voltages below this threshold the current is bulk limited and proceeds by hopping between trap states (either tunnel or Poole-Frenkel type as deduced from fittings not shown) for which carriers remain cold and do not gain enough energy to excite Er^{3+} ions and ii) For voltages above this threshold the electrons are injected into the conduction band of SiO_2 or SRO and are accelerated by the strong electric field up to average final energies between 3.0-4.5 eV for fields between 6-11 MV/cm, as shown by DiMaria *et al.* from Montecarlo simulations [101]. Accelerated electrons have thus enough energy to impact and excite Er^{3+} ions to the first excited level (0.8 eV-1550 nm) and even to upper levels (1.27 eV-980 nm, 1.46 eV-850 nm,…- for details see the Er^{3+} transitions in Figure 4.8); the EL spectroscopy of the upper levels of Er^{3+} (up to 2.54 eV-488 nm emission) can be nicely seen in the emission spectra of MOSLED capacitors, as shown in the previous chapter. As said before, above the EL threshold, the I(V) characteristics are well within the Fowler-Nordheim tunnelling dependence (see the inset of Figure 5.8.a). The Fowler-Nordheim formula is not reported here, because it was already presented in the previous chapters. A fit of the experimental data can be done using that expression. The fit to the data yields an effective barrier height of 1.9 ± 0.4 eV (1.1 ± 0.3 eV) for the Er:SiO_2 (Er:Si-NCs) layer. These values are considerably lower than the ones reported in the MOS capacitors (see Figure 4.13), which we believe it is due to the presence of the lightly doped top polysilicon in the slot waveguide region as we will demonstrate here in the following. The injected current in the active layer is in fact preceded by the conduction mechanisms taking place within the upper lightly doped (high resistivity) polysilicon layer. These mechanisms were further validated by measuring additional test devices, where two metal stripes were contacted to the two side-wings of the top electrode. The results are showing a current density dependent resistivity - from 10^5 Ω·cm (at 1MV/cm) down to 15 Ω·cm (at 11.5MV/cm), as seen in the figure 5.8.b. Therefore the dominant conduction mechanism through the lightly doped polysilicon was

thermionic emission over the potential barriers at the grain boundaries (grain boundary carrier trapping mechanism) [102]. In this case, the expression for the current density (J) is:

$$J = 2A^{*}T^{2}\, exp\left(\frac{-q\varphi_b}{kT}\right) sinh\left(\frac{qV}{2kT}\cdot\frac{\langle a\rangle}{L}\right)$$

where A^{*} is Richardson's constant, φ_b is the potential barrier height at the grain boundary, kT is the thermal energy, L is the length of the polysilicon layer, $\langle a\rangle$ is the mean grain size and V the total applied voltage. From this equation, the resistivity can be obtained:

$$\rho = \frac{V}{LJ} = \frac{V}{2A^{*}LT^{2}} \frac{exp\left(\frac{q\varphi_b}{kT}\right)}{sinh\left(\frac{qV}{2kT}\cdot\frac{\langle a\rangle}{L}\right)}$$

A good fit to the experimental data is obtained with a potential barrier height of (0.43±0.05) eV and a mean grain size of (15±2) nm (green line in Figure 5.8.b). Note that these values agree with previous reports on similar material [103]. On the contrary, the bottom electrode showed an ohmic behaviour (see inset of Figure 5.8.b) with a resistivity of 14 mΩ·cm. As a result, the low barrier height φ_b found at the electrode-active layer interface can be explained by assuming that injected electrons already face the electrode-active layer interface with energies above the conduction band (warm electrons) as a consequence of the thermionic transport and acceleration due to the voltage drop within the lightly doped polysilicon electrode. Figure 5.8.c shows instead the normalized Er^{3+} spectra collected either at the active waveguide surface (straight line) or at the output grating coupler (dotted line) for a bias of 10 MV/cm. The typical Er^{3+} emission spectrum is observed. Er^{3+} is excited mainly by impact excitation due to the highly energetic carrier after acceleration in the SiO_2 or SRO. Note a shift of about 10 nm and a different line shape between the two spectra. Since this shift and line shape difference are not observed when EL is collected from a cleaved facet of the active waveguide, they are thought to be due to the filtering action of the output grating due to some unavoidable random errors in its fabrication [104].

A more detailed analysis and study of the optical properties and the electroluminescence signal is presented in the following sections.

5.3.2 Optical characterization

- **Grating couplers**

The light is coupled in and out from the erbium doped silicon slot waveguides by using gratings. The distance between the grating and the active part (i.e. the one Er^{3+} doped) waveguide is 0.8 mm. Figure 5.9 shows the layout of these structure from the top view. Firstly, I characterized the input gratings. This study has been performed by using only one grating and collecting the light directly from the output facet of a cleaved waveguide. The gratings were designed to couple in only TM light which is the one where the field enhancement in the slot region is achieved. The grating coupler pitch and depth are 810, and ≈ 166 nm, respectively. Indeed only the TM polarized light was transmitted and no light could be detected when the polarization was rotated by 90 degrees. Then, a laser light was scanned in the region between 1500 nm and 1600 nm and the incident angle is varied to look for optimum coupling efficiency. Figure 5.10 shows the transmitted intensity at a fixed wavelength of 1540 nm as a function of the incident angle (with respect to the normal). The optimum coupling angle is 25° at which a coupling efficiency of -(24 ± 2) dB is achieved. Scanning the signal wavelength at this angle the transmission spectrum reported in Figure 5.10.b is obtained. It has to be noticed that changing the coupling angle the peak of the transmitted spectrum shifts as expected [105].

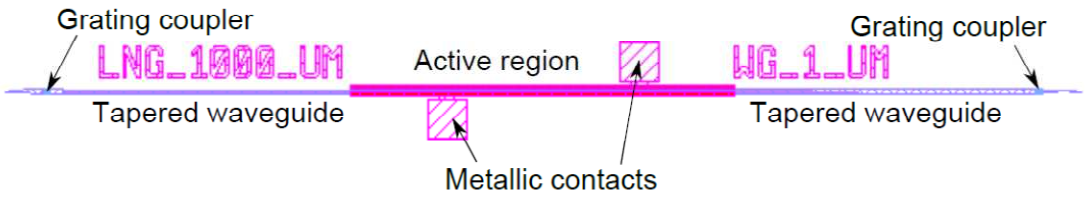


Figure 5.9. Layout of the test structure, which includes the two grating couplers, the adiabatic tapers, and the active waveguides (central purple part). In evidence also the two metallic contacts, which will provide the electrical current to the active area of the device.

- **Propagation losses**

Propagation losses have been evaluated by using waveguides with different lengths (1-3 mm). The propagation losses are (40 ± 5) dB/cm in the region between 1500 and 1600 nm for both waveguide types. No wavelength dependence is observed.

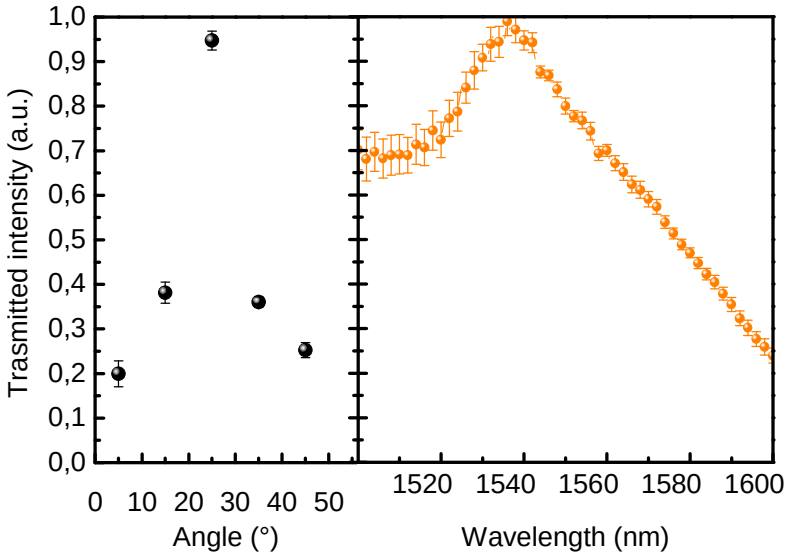


Figure 5.10. Transmitted intensity in a 1 mm long waveguide as a function of the incident angle **(a)** and as a function of the wavelength **(b)**.

Therefore, the Er^{3+} absorption losses – estimated to 3 dB/cm at 1540 nm [106] – are masked by scattering losses due to processing defects, mainly associated to the CMP process. This is inferred since a significant variation of the propagation losses from die to die on the same wafer has been observed, with fluctuations in excess of ± 20 dB. The random variations in the waveguide thickness due to the imprecise CMP could lead to mode leaking towards the heavily doped wings, and consequently to combined effect of radiative and free carrier absorption losses. This explanation is confirmed by a simple estimation with the values of the free carrier absorption in silicon reported in literature [107]. It is moreover worth mentioning that the scattering/absorption losses in polysilicon top cladding are probably contributing as well, despite the asymmetrical design of the slot waveguides. From similar measurements performed on the waveguide P02, comparable values of propagation losses have been found. This result leads to the conclusion that the losses are mainly due to the waveguide itself, and not to the active layer.

- **Electroluminescence**

An electro-optical characterization has been performed by monitoring the electroluminescence (EL) as a function of the applied biasing voltage. The stronger EL is observed in the devices without the nanoclusters than in the device with the silicon nanoclusters for the same applied voltage. In Figure 5.11.a, the electroluminescence spectrum when the emission is collected by placing a fiber directly on top of the

waveguide is reported. This EL spectrum evidences that we excite the Er^{3+} ions by impact excitation caused by hot carrier injection. In Figure 8b is reported the EL collected by a tapered fiber from the output grating as a function of the applied voltage for the Er:SiO_2 waveguides. This shows that light is guided in the active part of the device and emitted from the grating. The voltage range, where the EL signal can be detected, is very small (only 10 V – see Figure 5.11.b) and peaked at high voltages. The optical power density collected is in the range of tens of $\mu W/cm^2$, increases linearly with the electric field applied and superlinearly with the injected current. Interestingly, the light intensity does not depend appreciably on the waveguide length. Figure 5.11.c shows this dependence for both the Er:SiNCs and the Er:SiO_2 waveguides at a fixed applied voltage, respectively of 40 V and 44 V. These data indicate that the collected emission is coming from a region close to the grating independently on the waveguide length due to the high propagation losses.

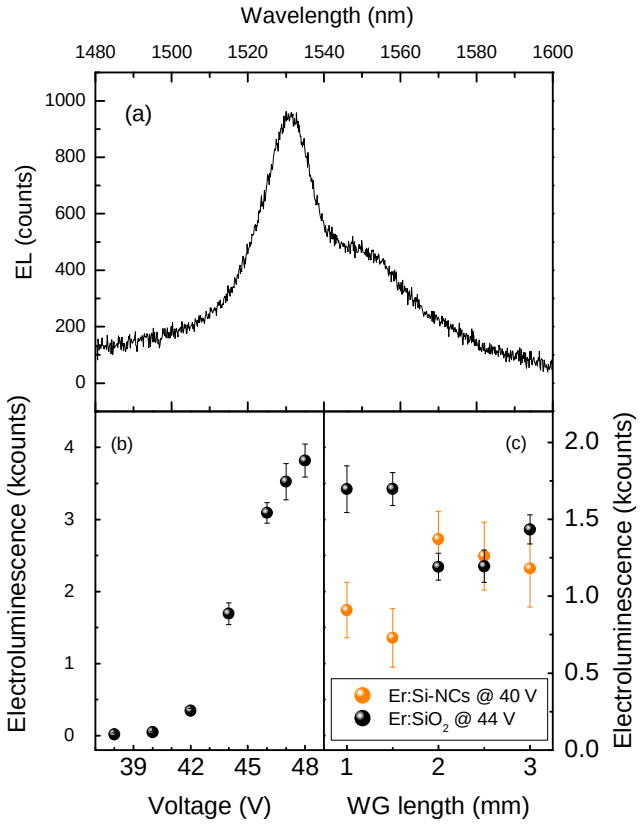
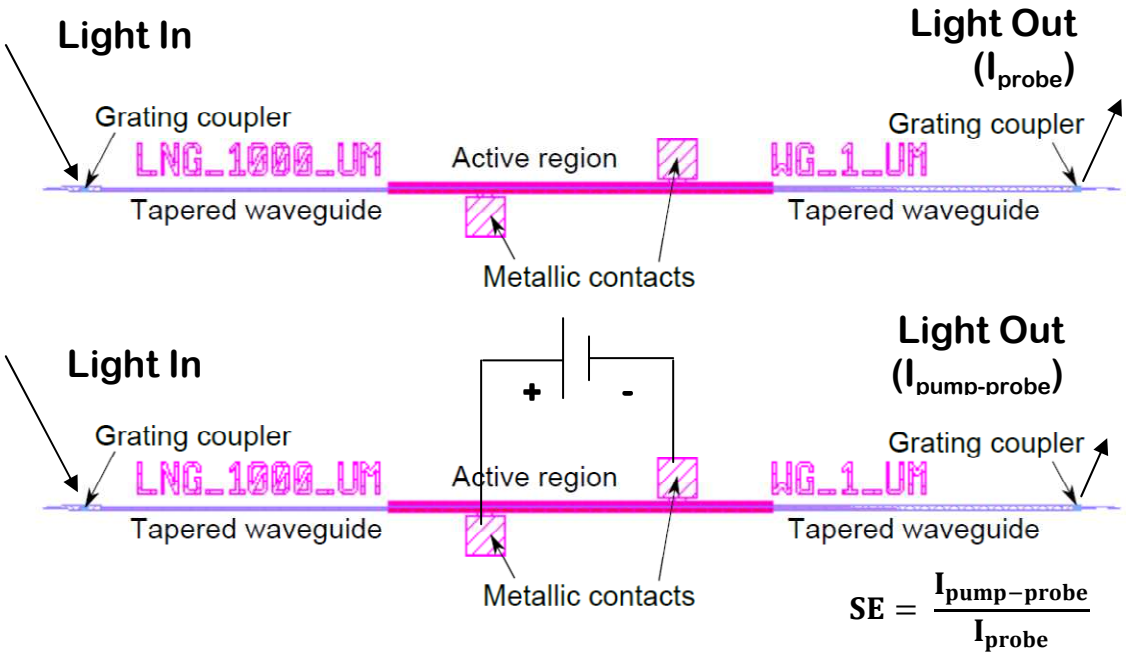


Figure 5.11. **(a)** EL spectra for a voltage of 44 V, collected from the top of the Er:SiO_2 waveguide. **(b)** EL signal as a function of the applied voltage for the 1 mm long Er:SiO_2 waveguide. Signal is collected at the grating output. **(c)** EL as a function of the waveguide length for the two different devices at a fixed applied voltage of 40 V and 44 V, respectively. The optical signal is collected at the grating output.

- **Pump-probe experiment**

Finally, I tested the transmission of a probe signal as a function of the applied voltage. This experiment is similar to a typical pump-probe experiment, but the novelty of this approach is that the probing signal remains the optical one, while the pumping is electrical. This experiment could give insights on the suitability of this approach for an on-chip optical amplifier. Figure 5.12 shows on top the scheme of the experiment with the definition of the parameters I_{probe} and $I_{pump\text{-}probe}$ and, on the bottom, the plot of ratio between the transmitted signal at an applied bias U versus the transmitted signal for U = 0 V – this quantity is usually named signal enhancement (SE) – as a function of the applied bias voltage. The reported data are for a signal wavelength of 1550 nm and for the Er:Si-NCs waveguides. We observed that the SE decreases for increased bias voltage. No dependence on the signal wavelength is observed too. We attribute this effect to charge accumulation in the Si-NCs [108] or defects in the oxide and to the free carrier absorption (FCA) phenomenon, caused by the injected current in the silicon slot waveguide. The losses are higher in forward bias (negative voltage applied to the gate) than in the reverse one, because the injected electron current is higher, too. Very interestingly, in the Er:SiO_2 waveguides the behavior of the SE is not monotonic, but at higher injection rate, in the forward polarization regime, it starts to increase. This absorption bleaching is observed for voltages lower than -40 V. The reasons of this interesting behavior are under further investigations. The main point that has to be underlined is that the overall loss of the device, at the maximum electrical pumping level, is only -6 dB, pointing out to a loss reduction of the 2 dB with respect to the optical losses at the lower levels of electrical pumping. However, the magnitude of this enhancement is larger than the maximum estimated enhancement value calculated from the emission cross-section of Er^{3+} in this active material and the Er^{3+} concentration. This fact, together with the weak spectral dependence of the enhancement, point out to a set of different factors (change in electrical transport across device, heating etc.) influencing the optical losses in studied devices under high electrical pumping. In fact, the optical losses increase, due to the injected current, because of absorption of the injected charges, accumulation of carriers in the interfaces and the refractive index change due to the injected carriers. Assuming that the accumulated charges change only the refractive index, for our doping concentration, a change of the refractive index of the order of $\Delta n = 0.01$ is expected [109]. Due to this change, we estimate a maximum increase of the propagation losses of 10 dB/cm, due to

the higher overlap of the optical mode with lossy regions of the waveguide. Thus it can be concluded that the refractive index change is probably of secondary importance with respect to the optical losses induced by free carrier absorption and accumulation. In conclusions, we do observe guided EL caused by emission from electrically excited erbium ions. Unfortunately, due to the high propagation and the FCA losses, no optical amplification has been observed. A necessary condition to develop silicon-based optical amplifiers which exploit the Er^{3+} ions as active material is to improve significantly the process to reduce the propagation losses.



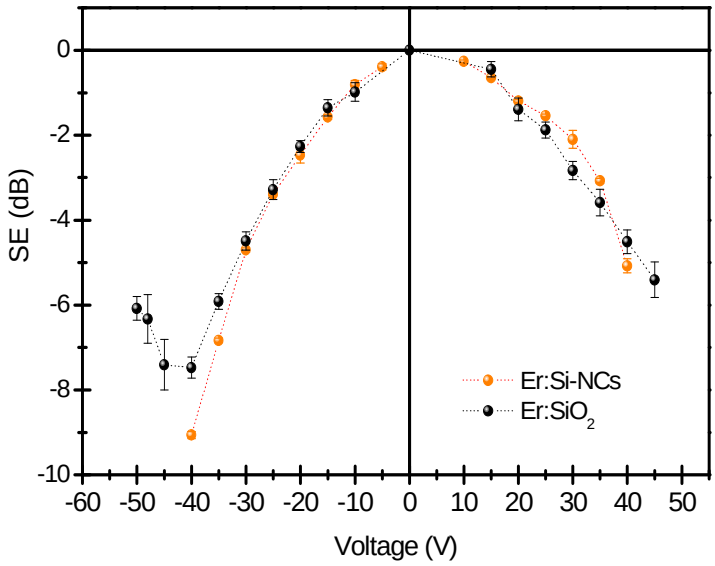


Figure 5.12. **(top)** Scheme of the pump-probe experiment. **(bottom)** SE as a function of the applied voltage for the two different waveguides, 1 mm long, at a fixed probing wavelength of 1550 nm.

5.4 Infrared photoconductivity of Si-NCs in the waveguides

In this section, I will experimentally investigate the infrared (IR) absorption and the photocurrent generation in Er-doped Si nanoclusters incorporated into silicon slot waveguides. The slot waveguides studied here are the same reported in all the chapter and presented in the section 5.2. The experimental setup is the same reported in the previous section (see Figure 5.7). The laser used for this experiment is the tunable infrared Santec TSL-210F, because of its possibility to reach also higher wavelength, as 1.6 μm.

We ascribe the observed IR photocurrent generation and the photovoltaic effect of Er-doped Si nanoclusters to the presence of the deep gap states in Si nanoclusters, the states through which Si nanoclusters sensitize Er^{3+} ions.

The Current vs. voltage, *I-V*, characteristics of the slot waveguide with Er-doped Si nanoclusters under dark and 1.5 μm guided light transmission are shown in Figure 5.13. The hysteresis loop observed under a voltage scan from +40 V to -40 V and backwards is a result of charge trapping in the slot region. The *I-V* curve under light transmission/illumination is collected at the maximum available optical power of 11 mW incident on the optical fiber grating coupler (~ 44 μW of power coupled to the waveguide). There is an apparent increase in current under illumination. The generated photocurrent (the difference between current under illumination and current in the dark) increases with the applied voltage bias and the increase is larger under forward bias (a photoconductivity regime) than reverse bias condition (a photodiode regime) of the *p-i-n* waveguide device. It is noteworthy that the photocurrent generation is a broadband effect, which has been observed in a wavelength range of 1500-1600 nm (see also Figure 5.14). This broadband photoconductive effect should be differentiated from room temperature sub-band gap light emission/absorption in silicon due to optically active defects, which is often observed in SOI membranes and implanted silicon [110]. We attribute the photo-carrier generation to the presence of deep gap states in Si nanoclusters.

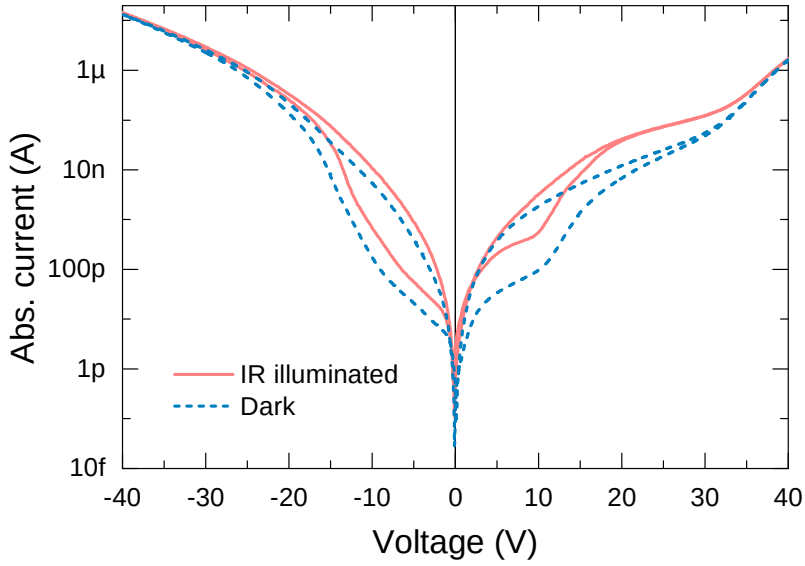


Figure 5.13. Current-voltage characteristics of the Er-doped SiO_x waveguide in dark and under 1.5 µm guided wave illumination (optical power ≈11 mW) showing photoconductivity. The hysteresis loop is observed under a voltage scan from +40 V to -40 V and backwards and is a result of charge trapping. Voltage ramp rate is ≤ 100 mV/s.

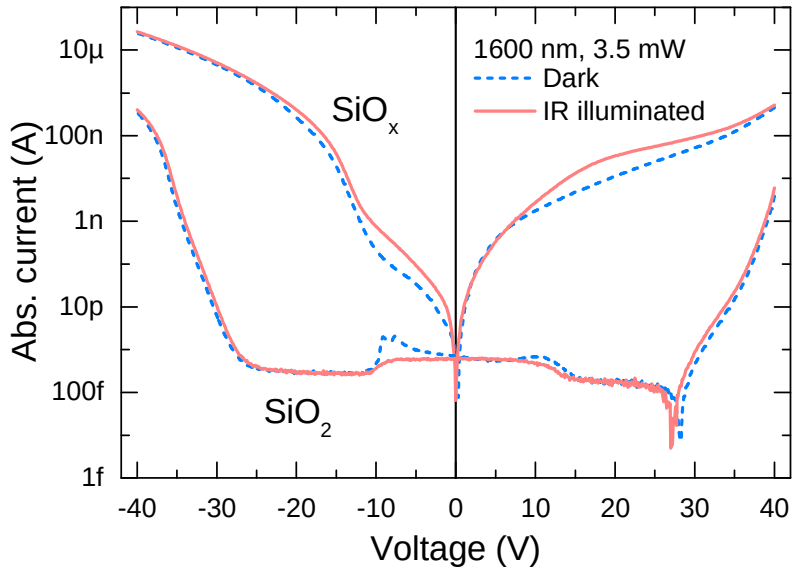


Figure 5.14. Current-voltage characteristics of the Er-doped SiO_x (upper curves) and SiO_2 (bottom curves) waveguides in dark (dotted lines) and under waveguide illumination (solid lines) with a wavelength of 1.6 µm (optical power ≈ 3.5 mW). Voltages are scanned from + 40 V to -40 V. The data show the presence of the photoconductive effect at a longer wavelength than the absorption band of Er ions. The photoconductive effect is negligible in the Er-doped stoichiometric oxide.

We have also ruled out the contributions of waveguide interface states, sub-oxide defects due to the Er implantation, and Er up-conversion based on the results presented in Figure 5.14. Figure 5.14 shows the I-V characteristics of the same Er-doped Si nanocluster device under transmission of 1.6 µm light. The photoconductive effect is

observed at a wavelength longer than the Er absorption band. Figure 5.14 also shows I-V curves both in dark and under light transmission of an equivalent (reference) device with an Er-implanted stoichiometric oxide in the slot. The reference device shows much lower, but measurable conductivity, and negligible photocurrent generation in the IR region (I-V at 1.6 μm is shown only in Figure 5.14). These results support our hypothesis that the photoconductivity is due to the Si nanoclusters. It is noteworthy that we have studied an optimized system of Er ions coupled to Si nanoclusters. However, we did not observe any increase in Er up-conversion due to neither light enhancement in the slot waveguide nor due to sensitizing of Er absorption with Si nanoclusters.

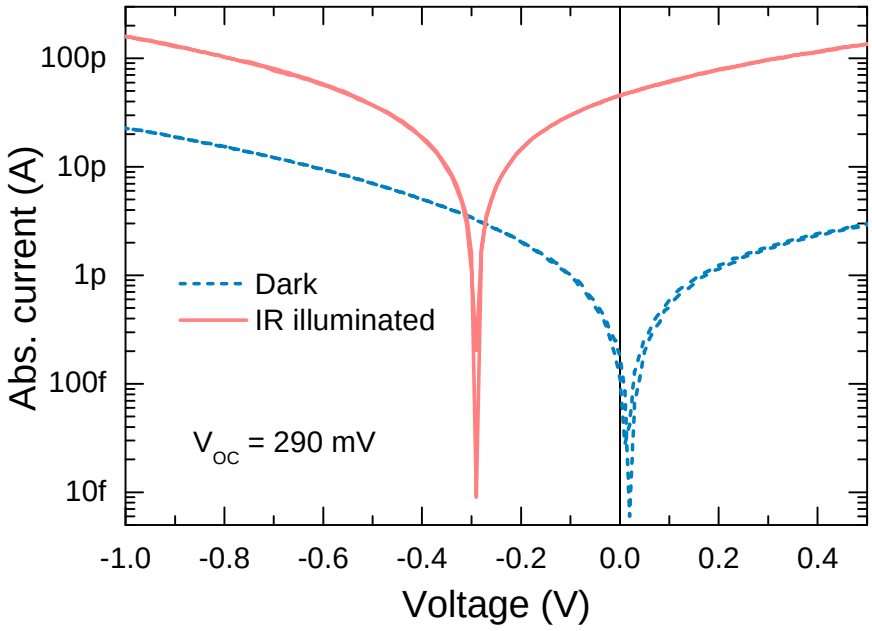


Figure 5.15. Current-voltage characteristics of the Er-doped SiOx waveguide in dark and under 1.5 μm guided wave illumination (optical power ≈7 mW) bracketing 0 V and showing photovoltaic effect with an open circuit voltage Voc = 290 mV. Voltage ramp rate is ≤ 10 mV/s.

The room temperature *I-V* characteristics bracketing 0 V and showing generated photovoltaic effect with an open-circuit voltage V_{oc} = 290 mV are shown in Figure 5.15 when a light signal of photon energy (wavelength) of 827 meV (1.5 μm) and of an optical power of around 7 mW is used. This V_{oc} value is related to the deep gap states in the Si quantum dots. The occupation of these states is evaluated by measuring photocurrent vs. light intensity at different bias polarities.

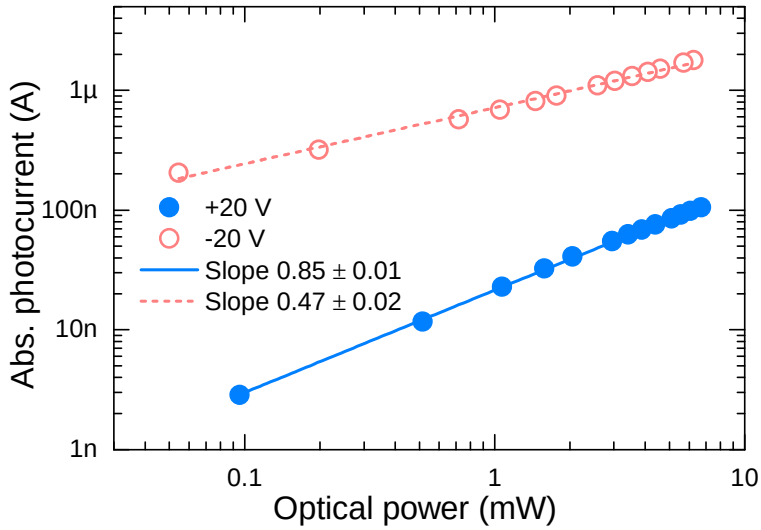


Figure 5.16. The absolute value of the photocurrent as a function of optical power incident on a waveguide grating coupler for two opposite electrical bias polarities. Lines are linear regressions through the experimental data points with the slopes indicated in the figure legend.

Figure 5.16 shows the absolute value of the photocurrent as a function of optical power incident on a waveguide grating coupler for two opposite electrical bias polarities. The photocurrent follows a power-law dependence on light intensity. The power law exponents are 0.47 and 0.85 for forward and reverse bias conditions, respectively. The exponent value is a measure of the position of the Fermi level (in dark) with respect to the sub-gap states [111], [112]. Under forward bias conditions the photocurrent is controlled by bimolecular recombination dynamics at the unoccupied sub-gap states lying above the Fermi level. This results in the exponent value of 0.47. Under reverse bias conditions the photocurrent is controlled by a linear recombination process with the deep gap states lying below the Fermi level and being populated with electrons.

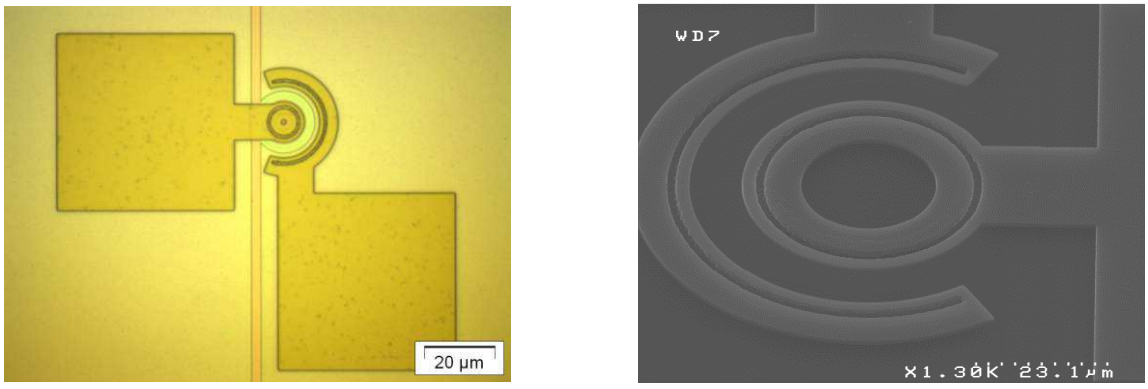
In conclusion, IR photoconductive and photovoltaic effects have been observed in Er-doped Si-NCs incorporated in a silicon p-i-n slot-waveguide. The effects are ascribed to the presence of deep gap states in silicon oxide due to the Si-NCs. These subgap states contribute to the electrical conductivity of the photonic devices with Si nanostructures. The room temperature open circuit voltage of the p-i-n waveguide device is 290 mV under monochromatic guided wave illumination with the photon wavelength of 1.5 µm. The light intensity exponent is found to take a value close to 0.5 and 1 for forward and reverse-bias conditions, respectively. The former is attributed to bimolecular recombination, and the latter is a characteristic of a linear recombination process with the states being populated with electrons.

5.5 Erbium doped ring resonators

Electrically driven erbium-doped SiOx horizontal slot ring-resonators coupled to slot waveguides have been designed, fabricated and tested. The objective was to engineer an injection laser cavity. Despite electroluminescence has been observed, no laser oscillations are reported due to a combination of several factors, which are here discussed.

5.5.1 Design and fabrication

Electrically driven silicon slot waveguide ring resonators coupled to slot waveguides are designed, simulated and fabricated. The active material of the ring resonator is Er-doped multilayered SiOx. It has to be noticed that the Er^{3+} ions are present only in the cavity – the ring resonator – and not in the waveguide. In this way, it will be possible to electrically inject currents only inside the resonator. The samples are fabricated by using Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. After the deposition, all the samples are thermally treated to yield the phase separation, the silicon precipitation and the nanocrystals formation. The annealing treatment is equal for all the samples (900 °C for one hour). Then, erbium is introduced in the active layer using ion implantation with a dose of 1 x 10^{15} atoms/cm^2 and energy equal to 20 keV. After the implantation, the samples are additionally annealed to recover implantation induced defects and to activate the implanted erbium ions. This second annealing treatment is performed at 800 °C for six hours. The layout of an electrically injected ring resonator optical cavity coupled to the slot waveguide is shown in Figure 5.17.



a) ***b)***

Figure 5.17. **a)** Photograph with a zoom on the ring resonator and on the electrical contacts. **b)** SEM image of the fabricated device.

A series of the ring resonators with various ring radii and waveguide widths were designed. A complete list of the structures is reported in Table 5.2.

WG number	WG width (nm)/RR radius (nm)	Coupling gap (nm)
1	WG300 / RR15	410
2	WG300 / RR15	440
3	WG300 / RR15	480
4	WG300 / RR25	475
5	WG300 / RR25	505
6	WG300 / RR25	545
7	WG300 / RR50	495
8	WG300 / RR50	525
9	WG300 / RR50	565
10	WG500 / RR15	345
11	WG500 / RR15	375
12	WG500 / RR15	415
13	WG500 / RR25	460
14	WG500 / RR25	490
15	WG500 / RR25	530
16	WG500 / RR50	365
17	WG500 / RR50	395
18	WG500 / RR50	435
19	WG1000 / RR15	200
20	WG1000 / RR15	220
21	WG1000 / RR15	240
22	WG1000 / RR25	200
23	WG1000 / RR25	220
24	WG1000 / RR25	240
25	WG1000 / RR50	200
26	WG1000 / RR50	220
27	WG1000 / RR50	240

Table 5.2. A complete list of the devices showing waveguide (WG) widths, ring resonator (RR) radii, and coupling distances.

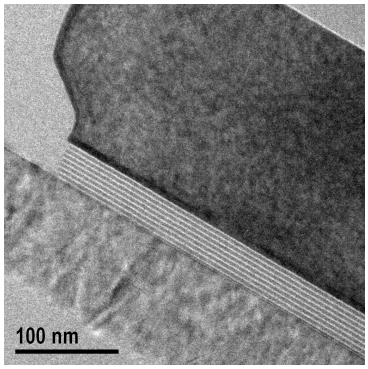


Figure 5.18. High-resolution cross-sectional TEM images of a ring resonator coupled to the slot waveguide. The multilayer structure of the active SiO_x material deposited by PECVD is clearly observed. The multilayer thickness is around 40 nm.

Figure 5.18 shows high resolution cross-sectional TEM images of a fabricated device. The multilayer structure of the active SiO_x material is clearly observed with the total multilayer thickness around 40 nm. The coupling distance between the ring resonator and slot waveguide (see Table 5.2) has been selected on the basis of our study of the critical optical coupling between a slot ring resonator and a slot waveguide. An example of the computed coupled intensity dependence on the gap distance is shown in Figure 5.19.

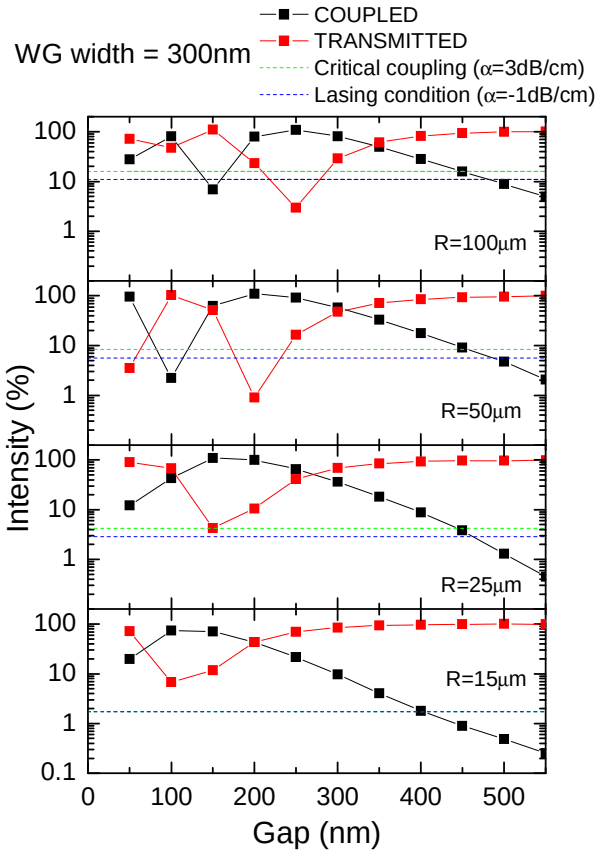


Figure 5.19. Transmitted and coupled intensity fractions as a function of the gap distance for different ring radii for a waveguide width of 300 nm. The coupling factor for critical coupling and lasing conditions are also reported (dashed lines).

5.5.2 Experimental characterization

- **Optical transmission**

Firstly, I have measured transmittance spectra of devices with different active materials. An example of the optical transmission spectra from the ring resonator coupled to the slot waveguide is shown in Figure 5.20. The quality factors vary significantly among different devices and active materials. The best values are in a range between 1.5×10^4 and 2.6×10^4.

The Q factor of the ring resonator with the radius of 50 µm, reported in Figure 5.20, is equal to (24400 ± 800). The measured free spectral range (FSR) dependence on the ring resonator radius (see Table 5.3) is in a good agreement with the theoretical dependence. We have not observed a dependence of FSR on the wavelength in a wavelength range of 1530-1570 nm. This fact leads to the conclusion that the erbium ions contribution in the FSR is masked by the high propagation losses. Waveguide propagation losses estimated from the quality factors are in a range of 27-41 dB/cm for the PECVD active material. These values agree well with the propagation losses measured in a series of slot waveguides with various lengths by the cutback technique and reported in the previous sections.

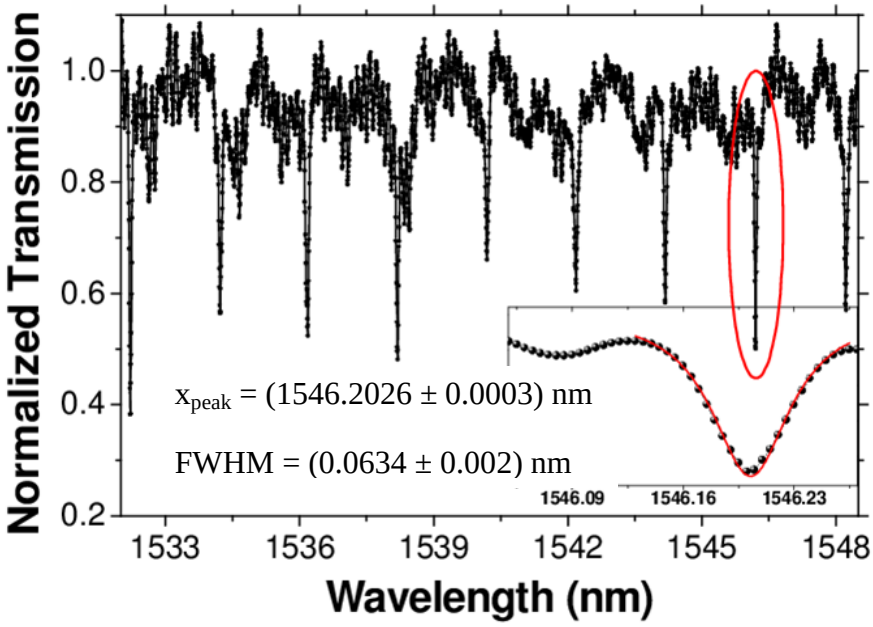


Figure 5.20. Transmission spectrum of a ring resonator with the radius of 50 µm.

Ring radius (µm)	FSR (nm)
15	7
25	4
50	2

Table 5.3. Rounded values of the free spectral range (FSR) measured as a function of ring radii.

- **Electrical characterization and electroluminescence**

Current-voltage, I-V, characteristics of a large series of ring resonators have been measured (see Figure 5.21). The I-V data scatter significantly among different devices, which we attribute mainly to a nonuniform CMP processing (on this argument you can

also see the section 5.3.2). Some I-V curves show rectifying behavior, which is characteristic of the *p-i-n* heterojunction. In bulk, device conductivity is low due to the low conductivity of the Er-doped SiO_x material and undoped region of the top polysilicon clad.

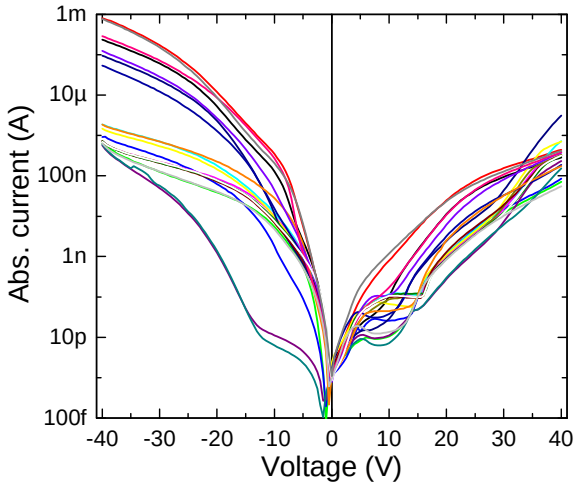


Figure 5.21. An example of I-V characteristics done on a series of ring resonators measured at different locations on the same silicon wafer.

Electroluminescence (EL) was measured from the top of the ring resonator (see Figures 5.22 and 5.23). EL spectrum is characteristic of Er emission. EL is observed at high voltages only, which implies impact excitation of the Er ions. This is consistent with our EL studies of LEDs and slot waveguides, reported in the previous chapters. I were unable to measure EL from the ring resonator coupled to the passive waveguide using either optical fiber grating couplers or bare waveguide facets because EL intensity is beyond our measurement capacities. This is due to large grating coupler losses, coupling and propagation losses, and small light emission area/volume. For example, the largest ring resonator area is an order of magnitude smaller than the luminescent waveguide area.

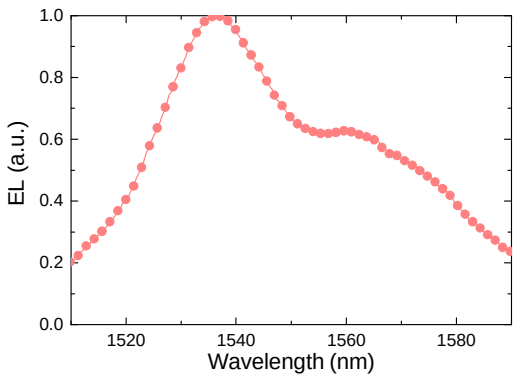


Figure 5.22. Normalized EL spectrum of a ring resonator measured at the applied bias of 50 V.

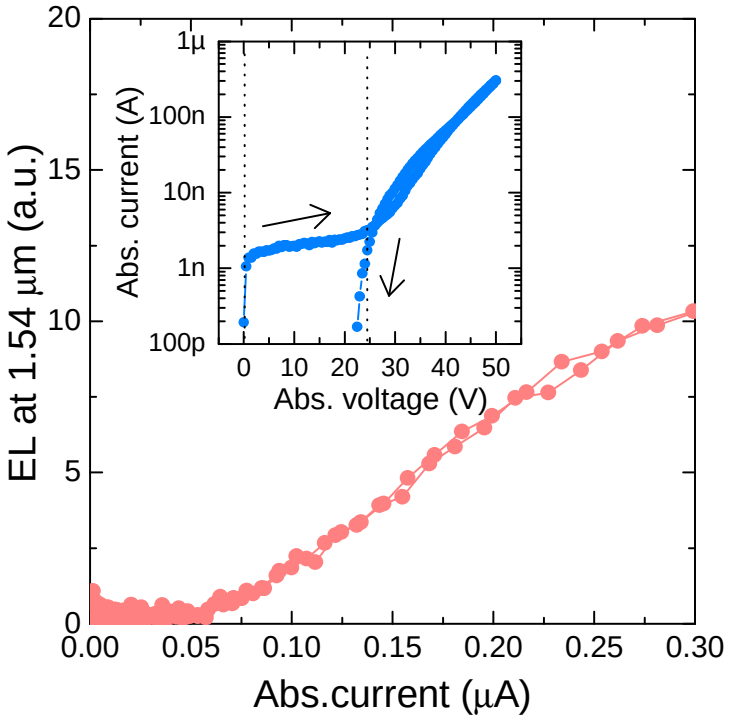


Figure 5.23. EL intensity at 1.54 µm as a function of injected current collected simultaneously with the I-V characteristic shown in the inset. The EL is observed at high voltages only, which implies impact excitation of the Er^{3+} ions. The optical power collected is in the order of tens of pW.

- **Transmission under electrical injection**

The transmittance spectra of a 1-µm wide slot ring resonator with the radius of 50 µm coupled to the slot waveguide are shown in Figure 5.24. The transmitted intensity decreases with increasing bias, which might be ascribed to a combination of several factors: increased losses in the slot waveguide and ring resonator due to electron injection, a change in the coupling due to the complex refractive index change, and to an experimental temporal drift of detector readings. The quality factor of the resonances decreases by 25% due to electron injection into the slot of the ring resonator (see Figure 5.25). Electron injection increases carrier absorption losses and lead to the decrease of the quality factor. A systematic blueshift of the resonances has been observed (cf. Fig. 5.25 and Fig. 5.26). This blueshift is due to the refractive index change because of electron injection and charge trapping in the ring slot. The blueshift dependence as a function on the voltage bias is reported in Figure 5.26: the blueshift itself is due to the carrier effect and that the thermal effects are insignificant. This result agrees with what we have found for the slot waveguides with the same active material.

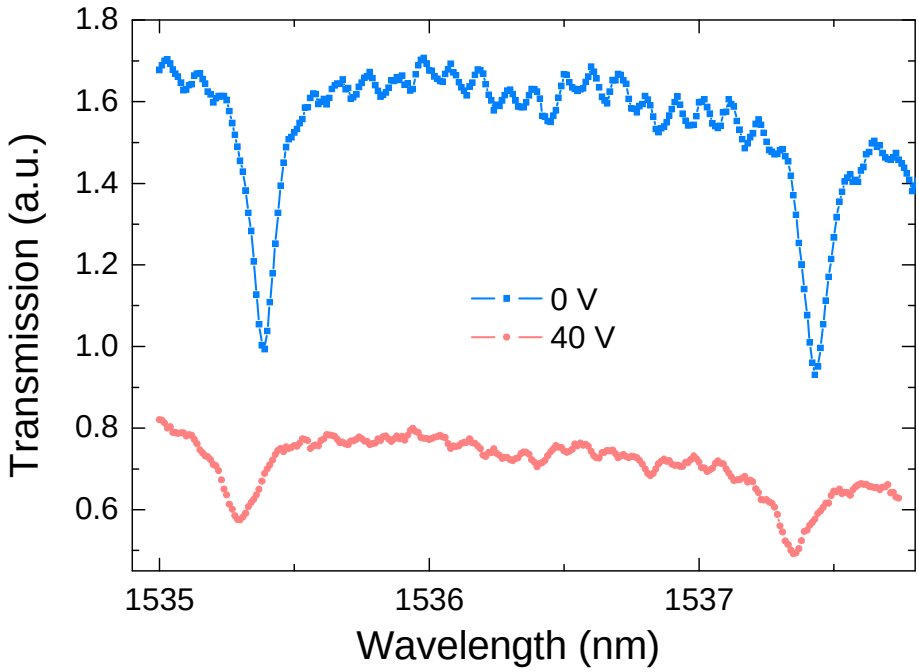


Figure 5.24. Transmittance spectra at zero and 40 V bias of a 1-μm wide slot ring resonator with the radius of 50 μm coupled to the slot waveguide.

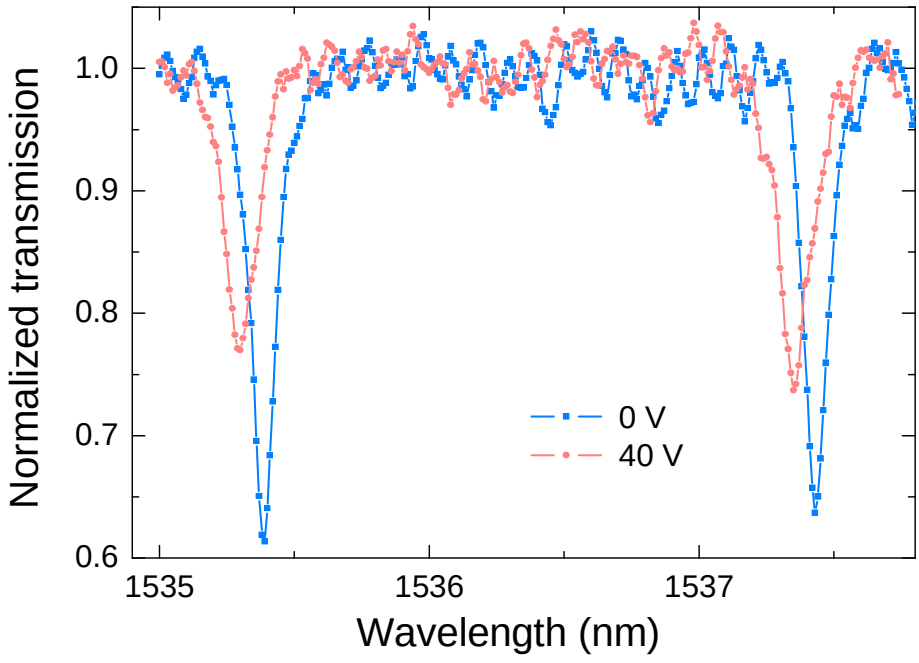


Figure 5.25. Normalized transmission spectra as shown in the previous Figure.

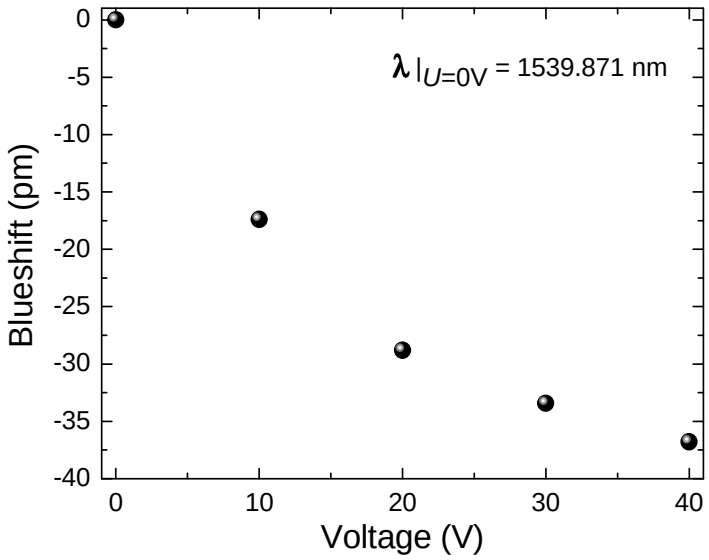


Figure 5.26. A square root dependence of the blueshift on applied bias.

5.5.3 Grounds for the lack of the active functions

We have not observed active functions in our erbium doped ring resonators due to a combination of several factors, which can be summarized as follows:

- High propagation losses in the slot waveguides.
- Low conductivity of the active Er-doped SiO_x, which results in charge accumulation in the slot region and an enhanced absorption and losses
- Erbium clustering due to high concentration in the middle of the active layer.
- Nonuniform fabrication process, mainly due to the CMP step and thermal oxidation of the top silicon layers of multilayered SiO_x.

5.6 Conclusions

In this chapter, I reported on the development, the fabrication, and the testing of Er^{3+}-doped silicon based optical cavities.

Electrically driven slot waveguide amplifiers have been designed and fabricated. I built different set-ups for the waveguides characterization which allows us to test the structure both optically and electrically without dicing the wafers. Probe stations have been upgraded to include on-wafer electro-optical measurements. Optical tests are performed and high propagation losses are found in all the samples. This results lead to the conclusion that the losses are mainly due to the waveguide itself, and not to the active layer. Electrical tests and opto-electrical measurements show that it is possible to have electroluminescence light and that the losses increase when an injected current is flowing into these devices. The electroluminescence signal is mainly due to the impact excitation of the erbium ions, while, on the contrary, the signal attenuation is due to the free-carrier absorption and charge accumulation. At high voltages, we observed absorption bleaching, which can be optimistically interpreted as due to the positive role played by stimulated emission in the Er^{3+} ions.

Moreover, electrically driven erbium doped horizontal slot ring-resonators coupled to the slot waveguides have been designed, fabricated and tested for the first time. The Er^{3+} electroluminescence from the top of the ring resonator is observed, but the emission is very low and the propagation losses are very high. Optical ring resonators show good quality factors, but device fabrication is not uniform and requires additional improvements. A better design of the grating couplers could be a large asset. Slot waveguide propagation losses have to be reduced to make a real working device. Despite not demonstrating optical amplification, this study shines some light on the path to achieve an all-silicon electrically driven optical amplifier.

Chapter 6

Conclusions and Future Perspectives

In this work, fabrication and experimental characterization of erbium and silicon nanocrystals based light emitting devices for lightwave circuits are presented. This thesis is the result of the work done in three years of PhD study, in collaboration with the Bruno Kessler Foundation, the Intel corporation and the CEA-LETI laboratory, and thanks to the support of the European Commission through the project ICT-FP7-224312 HELIOS.

The thesis is divided into two main topics. The first one is related to the study and the experimental characterization of silicon nanocrystals based light emitting devices, while the second one concerns the study done on erbium doped silicon nanocrystals based optical cavities, from the design and the simulation, up to the optical and the electrical characterization. All the characterizations have been performed at the Nanoscience Laboratory of the University of Trento.

Light emission silicon nanocrystals based devices are designed, fabricated and experimentally tested. Light emitting MOS capacitors and light emitting field effect transistors, with an active region composed by an alternating structure of silicon nanocrystals and silicon dioxide, have been realized. The samples under study have different values of silicon content excess and different values of the silicon oxide barrier thicknesses. The better suggestion in order to build an efficient light emitting source is the combination of low percentage of silicon excess with thinner silicon oxide layers. These two facts together allow a better growth of the nanocrystals and a narrow size distribution. The more efficient injection mechanism in such devices is the direct tunnelling at low voltages applied. In the light emitting devices fabricated within the HELIOS project unfortunately this was not possible, because of an unwanted oxidation

layer in the active material. In the light emitting devices fabricated within the INTEL project, we have found differences in the current-voltage characteristics and in the time resolved measurements. We believe that the differences between the devices have to be researched in a different quality of the oxide. The measurements done using an alternating current scheme have shown an increase in the efficiency of the devices.

Erbium doped silicon nanocrystals based light emitting devices have been designed and fabricated. The multilayers have allowed increasing the power efficiency roughly by 1.5 times with respect to the single layer devices. The optimized Si-NCs:Er LEDs have 0.5% of external quantum efficiency at low current densities and show a hundred microwatts per square centimetre of optical power density at the wavelength of 1.54 μm. The value of the external quantum efficiency is one of the highest in the silicon photonics scenario. We have found that the Er^{3+} ions are excited mainly by impact of high energy electrons under direct current excitation. However, a change in Er^{3+} excitation mechanism is observed under a pulsed excitation when sequential injection of electrons and holes into the Si-NCs takes place. This change, which is due to the coupling between Si-NCs and Er^{3+} ions, allows us to drive the Er-doped Si-NCs LEDs with significantly lower voltages than in DC. The optimized active material of Er-doped Si-NCs is a multilayer structure with 2 nm of silicon dioxide and 3 nm of SRO. This active material is to be used in erbium doped silicon nanocrystals based optical resonator structures. Therefore, electrically driven slot waveguide amplifiers have been designed and fabricated. Probe stations were upgraded to include on-wafer electro-optical measurements. Optical tests are performed and high propagation losses are found in all the samples. This results lead to the conclusion that the losses are mainly due to the waveguide itself, and not to the active layer. Electrical tests and opto-electrical measurements show that it is possible to have electroluminescence light and that the losses increase when an injected current is flowing into these devices. The electroluminescence signal is mainly due to the impact excitation of the erbium ions, while, on the contrary, the signal attenuation is due to the free-carrier absorption and charge accumulation. At high voltages, we observed absorption bleaching, which can be optimistically interpreted as due to the positive role played by stimulated emission in the Er^{3+} ions. Finally, electrically driven erbium doped horizontal slot ring-resonators coupled to the slot waveguides have been designed, fabricated and tested for the first time. The Er^{3+} electroluminescence from the top of the ring resonator is observed, but the emission

is very low and the propagation losses are very high. Optical ring resonators show good quality factors, but device fabrication is not uniform and requires additional improvements.

- **Future perspectives**

In this paragraph, I will try to give two ideas of future perspectives and future applications of this kind of devices.

The silicon nanocrystals based light emitting devices have low efficiency and low optical power density. Starting from this consideration, any applications in the lightening is not possible, but they could be used in all those fields in which the efficiency is not the main issue and the key-parameter. A possible application of the silicon nanocrystals based light emitting devices analyzed in this work could take place in the field of the quantum random number generators (QRNG). This target would be achieved from the possibility of counting the number of photons which reach a detector in a precise way even in the case of elevated counting, because this could result in a statistical improvement. Quantum cryptography aims to achieve security from fundamental physical principles, such as the quantum mechanical phenomena of entanglement and Heisenberg's uncertainty principle. In the last few years significant progress has been made in the theoretical understanding of quantum cryptography and its technological feasibility has been demonstrated experimentally. Quantum cryptography is therefore regarded as one of the most promising candidates for a future quantum technology and our LEDs are possible candidates to become quantum random number generators.

An electrically pumped silicon compatible laser is the "holy grail" of the silicon photonics. In my work, I have tried to develop an optical amplifier, by means of electrical pumping. Despite not demonstrating optical amplification, this study shines some light on the path to achieve an all-silicon electrically driven optical amplifier. Unfortunately, some fabrications problem occurred and the fabrication process needs to be optimized. As future perspective on this topic, I believe that silicon nanocrystals sensitized erbium ions could be used as an electrically pumped gain medium in a waveguide or in a ring resonator. The design of this kind of devices could be the same of the one reported in my work, but both the slot waveguide propagation losses have to be reduced and the fabrication problem have to be solved in order to reach a better electrical injection in the silicon quantum dots and make a real working device.

Appendix A: Experimental Setup

Current-Voltage measurements

The current-voltage (I-V) characteristics are recorded with an Agilent Technologies B1500A semiconductor device parameter analyzer. The hold time and the delay time in the I-V sweeps are set to be 1s to balance measurement speed and measurement integrity. The scanning voltage step is 100 mV. A compliance of 100 mA is imposed in order to limit output current and prevent any damages to the device under test. The I-V curves can be collected by scanning the device from accumulation to inversion and then backward from inversion to accumulation, or viceversa. In the thesis, usually the arrows on the I-V curves indicate the scanning of the measurement. In all my work, a negative gate voltage corresponds to forward bias, i.e., the MOS is in accumulation, while a positive gate voltage corresponds to reverse bias, i.e., the silicon substrate is in inversion. Figure A1 shows the experimental setup used for performing the I-V characterization. The measurements were recorded at room temperature into a dark room.

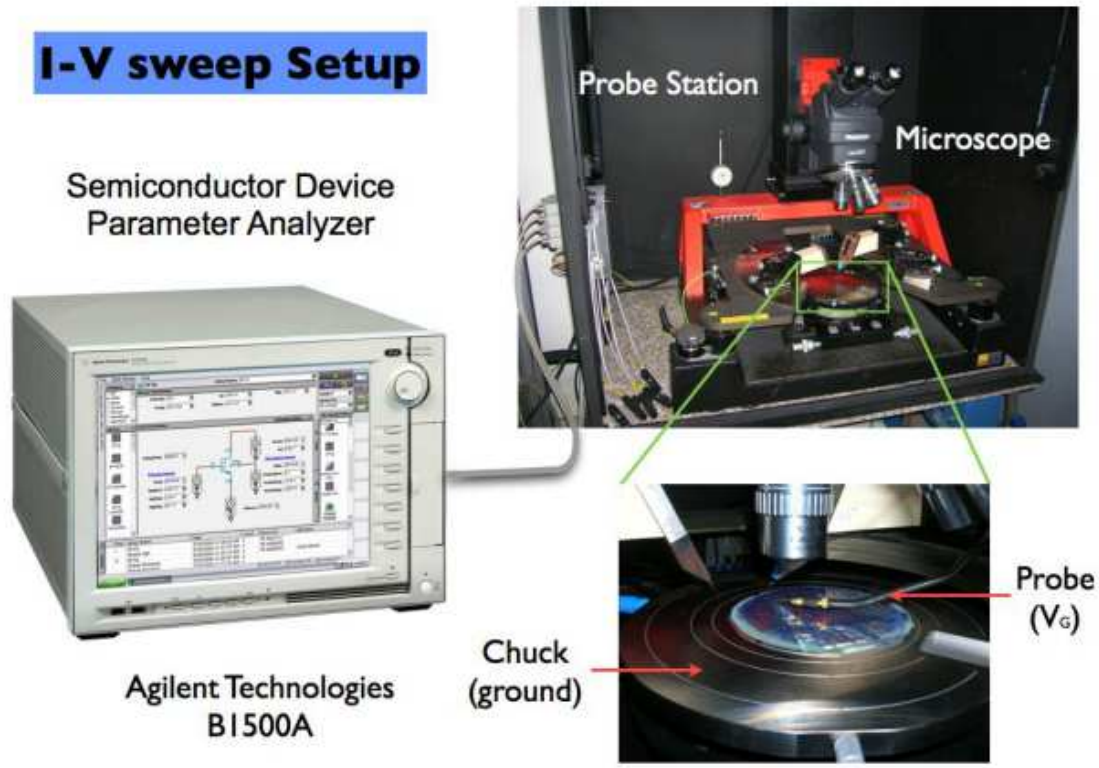


Figure A1. Experimental setup realized for recording the current-voltage measurements.

Capacitance-Voltage measurements

The capacitance-voltage (C-V) characteristics are recorded with an Hewlett Packard 4284A precision LCR meter. The hold time and the delay time in the C-V sweeps are set to be both 0.1 s. The scanning voltage step is 100 mV. A cable length of 2 m long is imposed in order to take into account the parasitic capacitance due to connections. The C-V curves are usually collected by scanning the device from accumulation to inversion and then backward from inversion to accumulation. The open circuit corrections are performed according to the operation manual. The alternating current voltage signal applied to the devices under test, needed to measure the capacitance, is 50 mV. Figure A2 shows the experimental setup used for performing the C-V characterization. The measurements were recorded at room temperature into a dark room, the same of the I-V characterization.

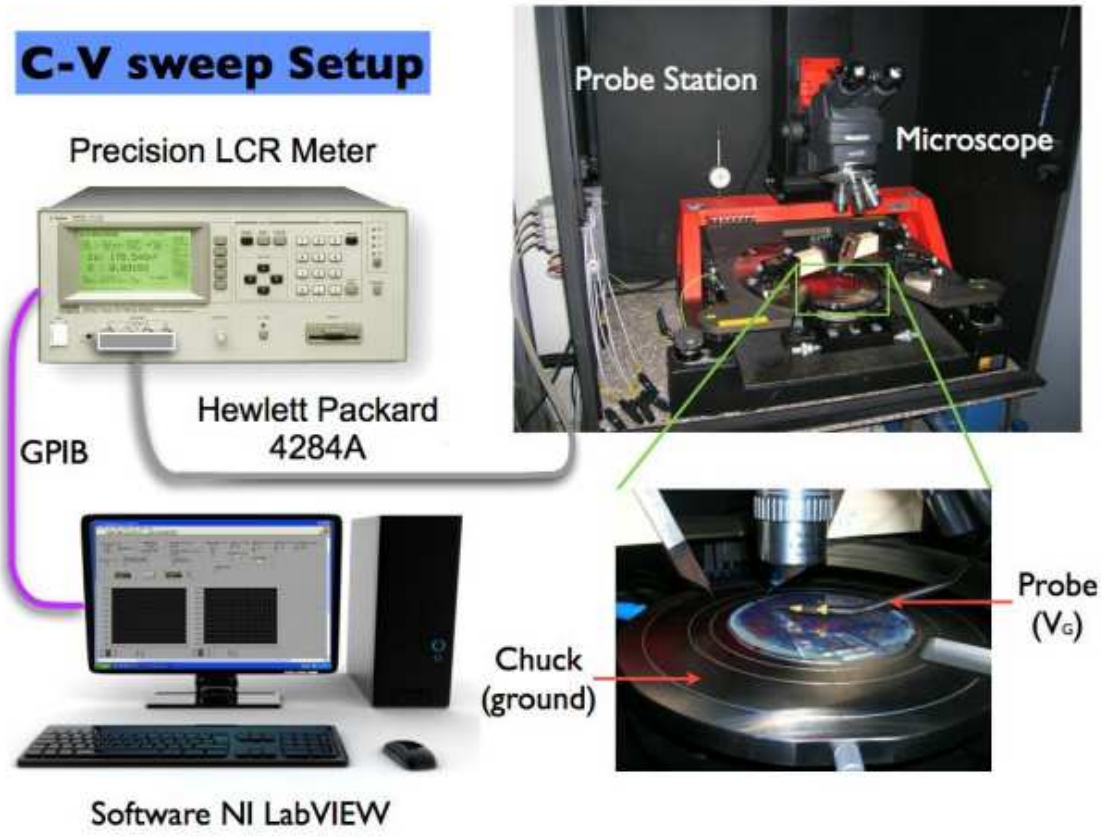


Figure A2. Experimental setup realized for recording the capacitance-voltage measurements.

Electroluminescence spectra measurements

Figure A3 shows the experimental setup used for recording direct current EL spectra. The EL spectra are collected with a fiber bundle and analyzed with a Spectra-Pro

2300i monochromator coupled with nitrogen cooled charge coupled device (CCD) cameras (one in the visible and one in the infrared). The current, which flows through the devices during the measurements, is recorded with an Hewlett Packard 4145A semiconductor parameter analyzer. The measurements were performed at room temperature in a dark room, different from the one presented in the previous paragraphs. A function generator, Tektronix AFG 3252, coupled with a high-voltage amplifier, Falco Systems WMA-300, is used to drive the device in AC regime.

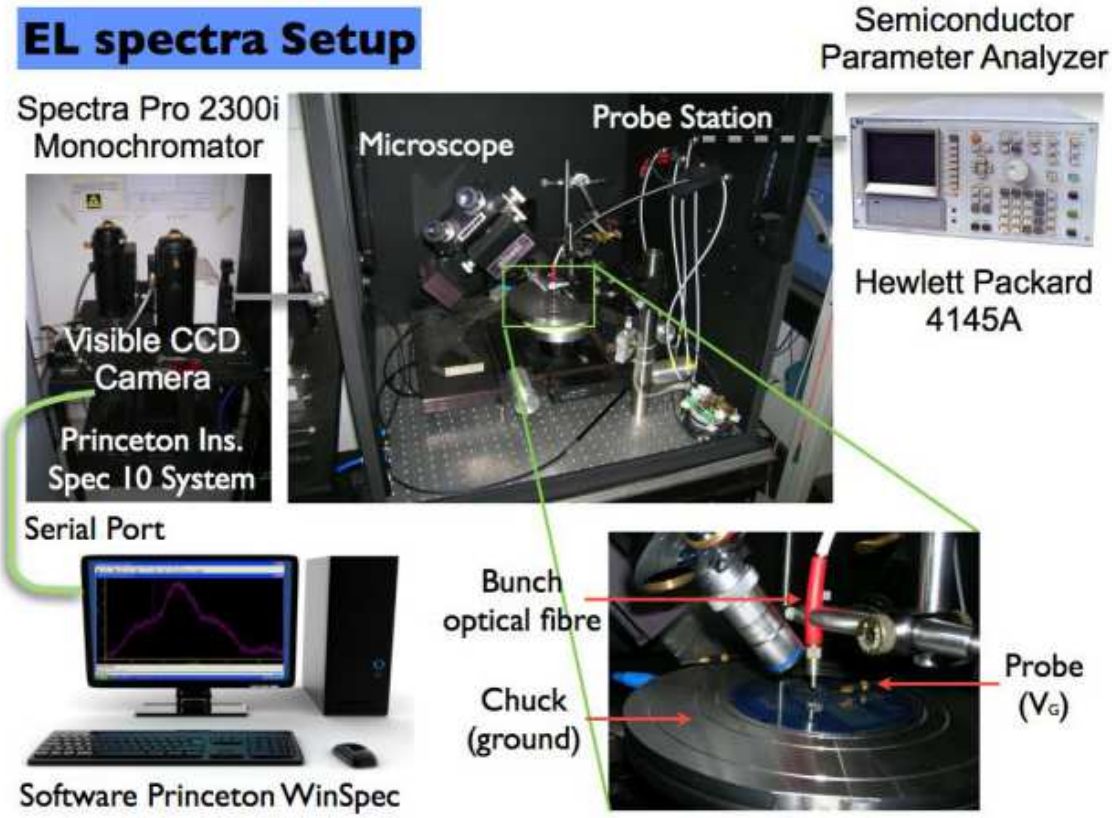


Figure A3. Experimental setup used for recording electroluminescence spectra of the LEDs.

Time-resolved electroluminescence measurements

Figure A4 shows the experimental setup used for collecting time-resolved electroluminescence measurements. EL is collected from the top of the devices using a bunch of optical fibers connected to a single photon counting module PerkinElmer SPCM-AQRH 16. Time-resolved EL signal is recorded with a multichannel scaler Stanford Research Systems SR 430. A Tektronix AFG 3252 function generator is used to apply square wave biases and to send a trigger signal to the scaler itself.

When probing the devices, forward bias is achieved by applying a negative voltage to the gate. The chuck inside the probe station is always referred to ground by the semiconductor parameter analyzer Hewlett Packard 4145A. All measurements were taken at room temperature in a dark room, the same used for the electroluminescence spectra.

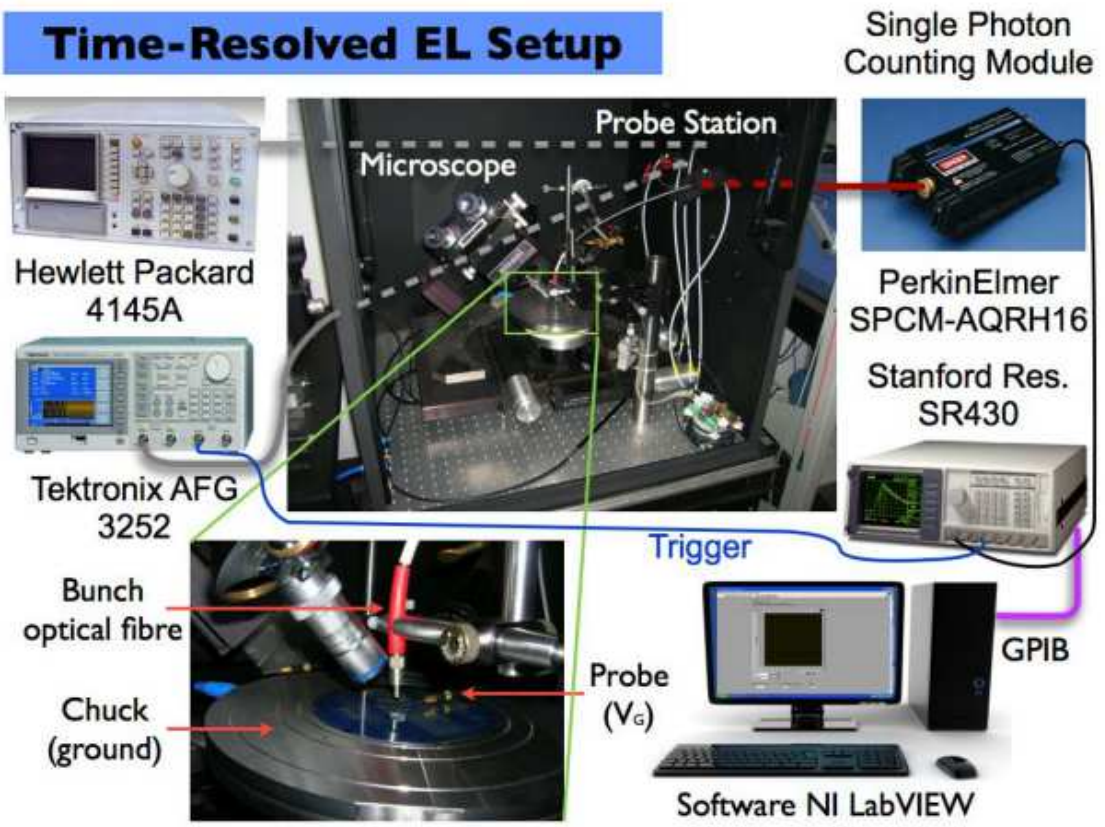


Figure A4. Experimental setup used for studying the time evolution of the electroluminescence when the devices are driven under a pulsed current injection scheme.

Figure A5 shows a photograph of the two different probe stations used for the characterization of the devices. The one reported at the left is the old one, used for the electroluminescence measurements, both the collections of the spectra and the time resolved ones. The one at the right is instead the new one, used for the current-voltage and the capacitance-voltage characteristics. This one has been also adopted with the two fibers supports, in order to do both electrical and optical measurements on the waveguides and on the optical cavities. Figure A6 shows instead a photograph of a zoom of the setup used for the EL measurements. This picture gives an idea of how the sample is contacted with the electrical probes and how the electroluminescence is collected from the device.

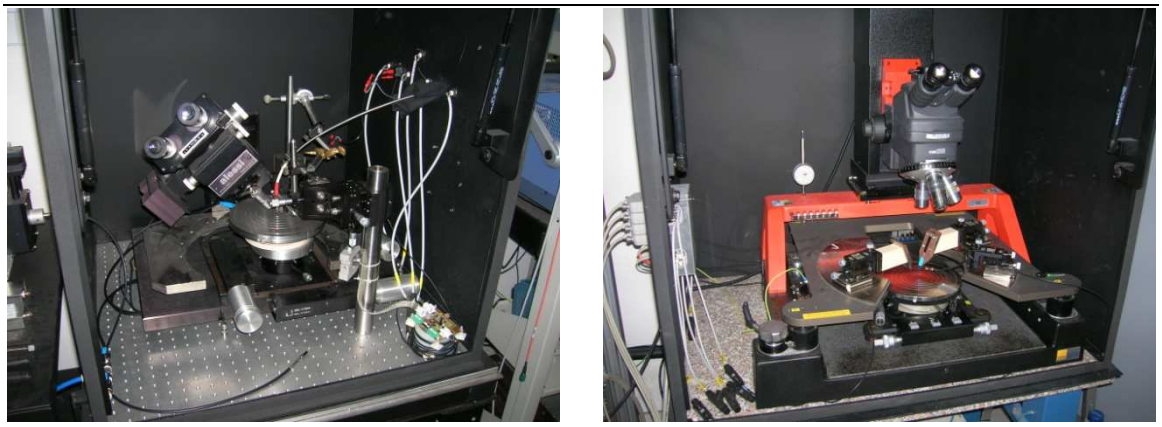


Figure A5. Photographs of the two different probe stations used for the characterization of the devices under study.

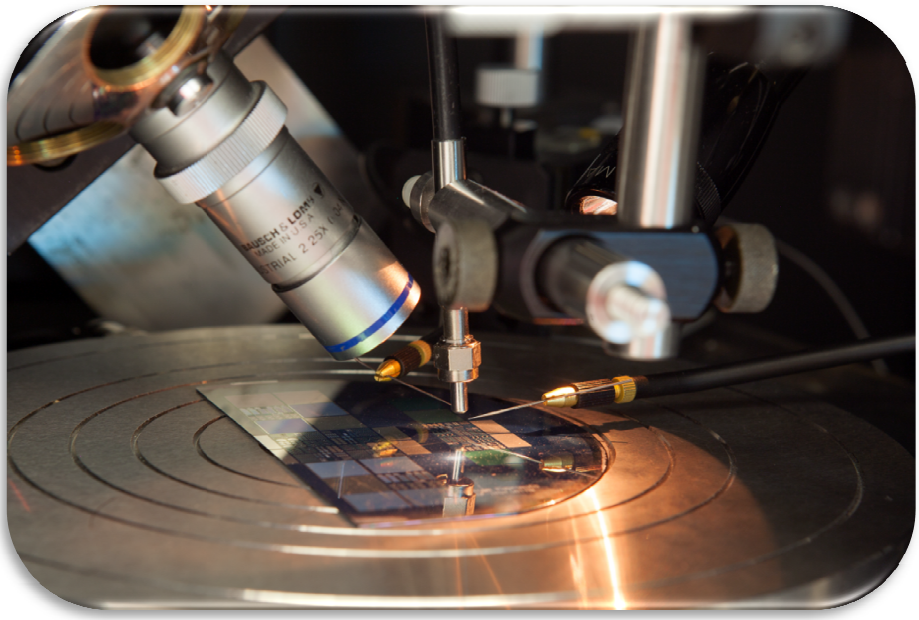


Figure A6. Example of the wafer on the chuck of the probe station, the electrical probe to contact the device under study and the fiber bunble on top in order to collect the electroluminescence signal.

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