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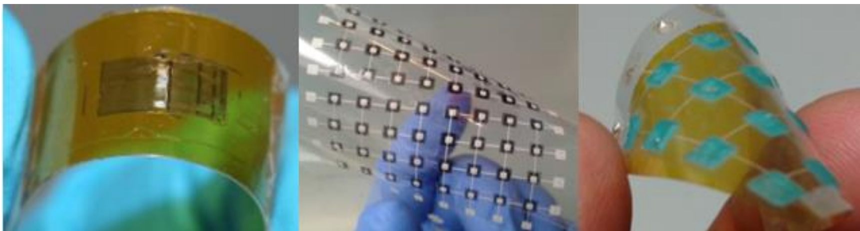
Towards Merging of Microfabrication and Printing of Si µ-Wires for Flexible Electronics

Saleem Khan



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TOWARDS MERGING OF MICROFABRICATION AND PRINTING OF SI µ-WIRES FOR FLEXIBLE ELECTRONICS

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Dedicated to

My Parents, Family and Teachers

Abstract

This PhD thesis focuses on the investigation and development of a feasible technology route for fabricating multifunctional flexible electronic devices through heterogeneous integration of organic/inorganic materials on polymeric substrates. The three types of printing technologies investigated during this research include: (a) Transfer printing of inorganic semiconductors processed through standard microfabrication techniques, (b) Spray coating for deposition of organic dielectrics and metal patterns, and (c) Screen-printing of solution based transducer materials. Fabrication of electronic devices based on transfer printing of high-mobility inorganic semiconductor materials (i.e. Si), aided by high-resolution possible with microfabrication technology, was explored for high performance electronics. A cost-effective processing of printable materials is desired and therefore, through printing technologies, this thesis also explored ways to bring closer the well-established microfabrication and conventional printing tools. Due to commercial interests, the major research focus in flexible electronics thus far has been on applications such as photovoltaics and displays. However, this research is focused on active/passive electronics for sensing applications like electronic skin, which is of significant interest in robotics for safe human-robot interaction and other manipulation and exploration tasks.

Optimization of the Transfer Printing for translating Si microwires from SOI (silicon on insulator) wafers on secondary flexible substrates has been investigated. Processing steps have been improved for fabrication of Si microwires on donor wafers and dry transferring them onto flexible PI (polyimide) and PET (polyethylene terephthalate) substrates. The downscaling of Si in the form of microwires and using them as building block for active devices such as field effect transistors were explored in this thesis. The microwires retain the high carrier mobility, robustness, high performance and excellent stability. Arrays of MISFETs (metal insulator field effect transistors) structures were successfully fabricated and the response variations were compared. The differently doped Si microwires were analyzed in an asymmetric metal semiconductor metal (MSM) structures under planar and bend mode conditions. The optical response as well as the thermoelectric properties of the alternately doped pn-Si microwires were also investigated.

A feasible fabrication route is presented, where combination of transfer printing for Si microwires and development of the subsequent post-processes by additive manufacturing techniques i.e. Screen-printing, Spray coating and Micro-spotting are mainly investigated. The Si microwires are employed as the semiconductor in the MISFET devices whereas screen-printed metal patterns are used for back-gate and deposition of dielectric layer is performed through spray coating. In parallel, screen-printing is also used for development of large area pressure sensor patches using two different materials i.e. P(VDF-TrFE) (Polyvinylidene Fluoride Trifluoroethylene) and nanocomposites of MWCNTs/PDMS (multiwall carbon nanotubes mixed with

poly(dimethylsiloxane) for measuring dynamic and static contact events. Promising results have been achieved by developing a cost-effective way of manufacturing an all Screen-Printed flexible pressure sensors using piezoelectric transducer through P(VDF-TrFE) and piezoresistive based MWCNT/PDMS nanocomposites.

Active electronic circuitry is needed for signal conditioning, amplification or processing of the sensory data on the flexible foils, which is deemed to be developed through Si microwires based technology in the next phase of the project. Ultimate goal of the PhD study was to develop a fabrication platform by combining three different printing technologies for large area sensor patches. Major challenges involved in the development of flexible device designs and printing technologies are highlighted and addressed with dependable solutions. The research concludes with proposing an innovative approach towards heterogeneous integration of large area sensory cells made of organic materials to the active devices based on inorganic semiconductors such as Si microwires. This technological platform for heterogeneous integration of devices made of diverse materials (organic, inorganic etc.) on soft substrates is believed to be a step-change needed to advance flexible electronics towards manufacturing.

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Chapter 1
Introduction and Thesis Background

1.1. Flexible and Printed Electronics

Future electronics will be bendable, flexible and seamlessly printed on large-areas i.e. areas larger than the standard wafer size. The recent significant addition to the field of microelectronics is the fabrication of electronic devices on large areas and nonconventional polymeric substrates that can flex, bend and conform to 3-D surfaces very efficiently [1-5]. Vision foreseen for large area electronics is to revolutionize the existing flat/planar devices through various curvature designs starting from curved, single time bendable, stretchable, foldable and rollable electronics for desired applications [3, 6]. This paradigm shift from micro to macroelectronics will result in many exciting electronic gadgets such as foldable displays, electronic skin, electronic eye imagers, autonomous vehicles with all around sensors, and wearable electronics for early detection and continuous health monitoring – possibly leading to self-health-management [1, 3, 5, 6]. Lightweight, portability, conformable to nonplanar surfaces, large area coverage along with low-cost and high-performance are the distinguishing features of this new technology vis-a-vis state of the art planar electronic components.

Research in this field is broadly directed towards the development of innovative designs and new device structures, rollable plastic substrates, materials processed at lower temperatures (~ 300 ^{o}C) and reliable fabrication technologies. Development of all these streams are vital for the advancement of macroelectronics technology for useful practical applications. All these categories have been explored extensively since the birth of macroelectronics and research development is steadfast (both in academia and industry) worldwide to unveil the potentials of this fast growing and diverse field. The multidisciplinarity of this field is evidenced by development of devices such as, large area printed pressure sensors, radio frequency identification tags (RFID), solar cells, light emitting diodes (LED) and transistors etc. [3, 5, 7-10]. Among different fields desired for flexible electronics, the development of a reliable manufacturing technology where diverse materials (organic/inorganic in solid state as well as solution based) are easily processed and patterned in a cost efficient way on large area polymeric substrates are highly looked-for. Research on the development of flexible electronics is therefore, focused broadly on the fabrication processes pursuing both the matured microfabrication technologies for solid-state electronics as well as solution-based printing technologies [4, 8, 10, 11].

Printing technologies have long been practiced in the printing/press industry for many years by now and the expertise could easily be rendered for manufacturing of flexible devices. Traditional approaches for printing electronics and sensors involve bringing pre-patterned parts of a module in contact with the flexible (or non-flexible) substrates and transferring the functional inks or solutions onto them [4, 10]. Organic materials are considered as the key enabler for printing technologies due to their solution

processability at low temperatures and thus remained the natural choice of research for development of flexible electronics from the very beginning. Organic materials have the advantages of being mechanically flexible after deposition on polymeric substrates as well as the lower principal cost both for materials and for solution processing, which make them the preferred choice for cost-efficient manufacturing [12-14]. The ease to fabricate large area sensors by sandwiching organic materials in parallel plate capacitive structures using screen-printing is ideal for low cost fabrication. Despite all these attractions, organic based active electronic devices show lower performance both in terms of speed and durability compared to conventional inorganic electronics, which remains a major challenge for all-organic based electronic circuits [5, 14, 15]. Devices made of organic semiconductors typically have low charge carrier mobility (~1 with respect to ~1000 $cm^2\ V^{-1}\ s^{-1}$ of single crystal Si), which makes them much slower to respond than crystalline Si built devices [5, 16]. Small molecule crystalline organic materials show moderately better performance but the processing condition i.e. CVD (chemical vapor deposition) hinders their deposition on large areas. Furthermore, poor stability and short life of the organic materials make them a meagre choice for electronic systems requiring better performance and longer shelf life. A large number of applications, especially where faster communication and computation is needed, require high-performance flexible electronics, which is a very challenging task at current stage for organic based semiconductors [17, 18].

1.2. Introducing Monocrystalline Silicon in Flexible Electronics

Silicon as a semiconductor material has been investigated for more than 50 years by now and the manufacturing technologies have already matured for the microelectronics industry. A number of industrial procedures have been developed to obtain bulk Si in its purest form where final product is produced as wafers with variant diameters [19]. Silicon wafers are intrinsically brittle owing to their higher thicknesses usually greater than 100 µm. However, they become mechanically flexible when thinned down below 20 µm [4, 5]. The standardized techniques of microfabrication for electronic devices and microchips are carried out in ultra-clean room environments, where the processing at higher temperatures i.e. ~1000 ^{o}C help in completing the steps such as developing high quality oxide layers and ion implants etc. With the lower thermal budget (< 350 ^{o}C) of polymeric substrates and lack of chemical inertness to most of the chemicals used in photolithography, it is impossible to develop monocrystalline Si and further process it on top of polymeric substrates. Therefore, an alternative technique i.e. Transfer Printing has been developed recently, where single crystal inorganic materials are transferred in solid state from a donor wafer onto a secondary substrate [5, 18]. Donor wafers usually SOI (silicon on insulators) having ultrathin silicon layer (thickness ~ 500 nm – 2.5 µm) are the standard wafers used in microelectronics industry, where all the high temperature processes are performed on the wafer itself and after finishing all the developmental steps, microstructures are transferred to a polymeric substrate. The usual

transfer routes are either through a solution cast, flip-over or a stamp-assisted. For deterministic assembly of the microstructures, stamp assisted transfer is preferred as the finished surfaces of the microstructures are exposed for the post-processing. Silicon microstructures are developed through the standard photolithography technique; variations in the designs are possible during the photomask designs. Hence, shaping Si into many different structures like membranes, wires, spirals and circles etc. is possible. The fabrication route is designed according to the post-processing steps and target applications. All the fabrication steps are finished on the wafer and transferred in the form of membranes onto a secondary substrate when no developmental steps are desired. On the contrary, Si is developed in the form of nano/micro-wires and transferred to secondary flexible substrates. The possibilities of post-processing of Si with diverse materials especially solution processed metals and organic materials provide an exciting opportunity for development of hybrid organic/inorganic devices.

1.3. Motivation and thesis overview

Attaining all the exciting features of flexible electronic circuits by using a single stream of materials (organic or inorganic) for the complete device manufacture is very challenging. As they are often conflicting (Figure 1.1), for example the organic semiconductor based flexible electronic is considered as low-cost solution but the performance of devices from them is modest. On the other hand, conventional Si based electronics is well proven to have high-performance, but the fabrication cost is high. There is therefore a need to explore and develop new technological platform, which benefits from the positives of both of these contrasting technologies. For example, a platform that merges or brings together the active devices made by utilizing

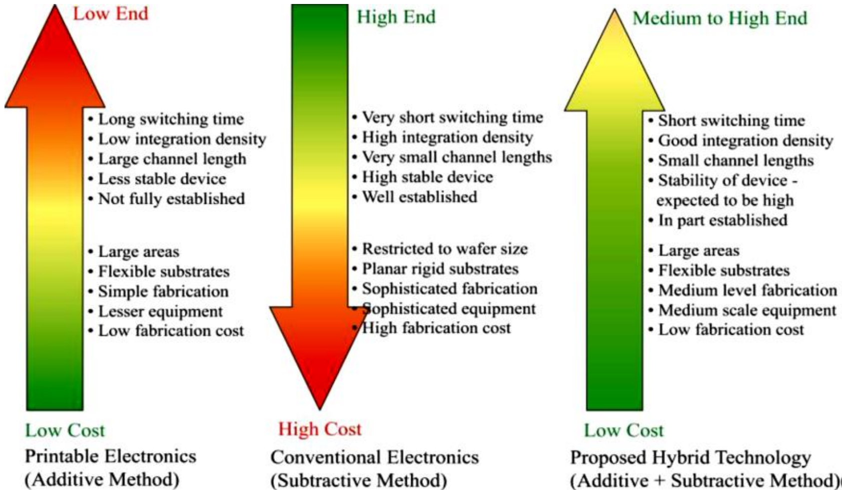

Figure 1.1. Features highlighting the pros and cons of printable and conventional microelectronics for the low, high and medium to high-end devices.

conventional microfabrication with passive structures and devices developed through printing technology. The electronics developed with microfabrication technology will gain in terms the high resolution and possibility to process high-mobility materials, which lead towards high-performance electronics. Incorporation of printing technologies into this approach will result in development of passive structures like interconnects, metal electrodes and coating organic dielectrics. Additionally deposition of transducer materials between two parallel plate electrodes for fabricating sensors and eventually connecting them with the active devices (MISFETs) through extended gate structures will allow the overall cost of the devices and circuits to come down.

This thesis introduces a new technological route where three different printing technologies are merged together to fabricate flexible devices. The three printing technologies i.e. transfer printing; screen-printing and spray coating are utilized to fabricate large area pressure sensors and MISFET (metal insulator field effect transistors) devices. The screen-printing is employed to develop large area pressure sensors by depositing transducer materials such as P(VDF-TrFE) and MWCNT/PDMS nanocomposites. An all screen-printing technology is used to print sensors (4 modules of a 4×4 sensors array, each layer in one print step), where the sensing materials are sandwiched between screen-printed parallel metal (silver (Ag)) plates. Additionally, screen-printing has been used as a rapid patterning tool for the back-gated metal contacts of flexible MISFETs. Transfer printing is used to incorporate Si microwires as the semiconductor layers accompanied by metal patterning and dielectric deposition through screen-printing and spray coating respectively. An enhanced transfer yield more than 95 % of Si microwires is achieved by introducing a new approach of over-etching in the first transfer step and a 100 % yield in the second transfer steps. Spray coating is used to deposit organic dielectrics such as PMMA (poly (methyl methacrylate)) and UV-curable (DuPont) dielectric solutions. These structures are developed, aiming the future scope of this research, where the MISFETs would be coupled through extended gate approach with one of the electrodes of each pressure sensor. Therefore, this technological route is believed to provide an attractive platform for heterogeneous integration of hybrid organic and inorganic based devices on a single foil for large area sensing applications.

This thesis is divided into two major parts. First part of the thesis discusses the potentials of the printing technologies utilized in this thesis and on the development of large area pressure sensors. Focus is more on the experiments of an all screen-printing steps for development of sensors in parallel plate structure. The second part introduces the key developments made towards the Si microwires based devices. All the three printing technologies are involved in the fabrication process of transistor structures on flexible polymeric substrates. For instance, screen-printing is used to print the back-gate followed by transfer printing for Si microwires and spray coating of the thin organic dielectric films. An overview of the thesis and major contents of the chapters are:

Part I.

Part-I of the thesis covers details about the printing technologies and screen-printing of large area pressure sensors, which are supposed to be integrated with the Si microwires, based MISFETs in the form of extended gate structure.

Chapter 2: This chapter highlights the main printing technologies and the printable materials. A detailed overview is presented of the available printing technologies practiced for flexible electronics along with their prominent advantages and disadvantages. Details about the operation mechanism of different printing technologies with special focus on the transfer, spray and screen-printing are highlighted.

Chapter 3: This chapter shows the development of modular expansion of arrays of large area pressure sensors. The two different transducer materials i.e. P(VDF-TrFE) and nanocomposites of MWCNTs/PDMS are used to develop sensors in a parallel plate capacitor structure.

Part II.

Second part (chapters 4-8) of thesis provide details related to Si microwires development and their transfer printing from donor wafer to a secondary substrate. Optimization of the Si microwires transfer and the various processing steps developed to deposit metal contacts and dielectric materials for MISFETs devices fabrication.

Chapter 4: Chapter 4 presents the various techniques to get flexible Silicon. The L-Edit designing steps to develop Si microstructures through standard photolithography and reactive ion etching techniques is described in full detail. Finally, ways to get vertical and planar Si microwires using bulk and SOI wafers are presented followed by discussion on various transfer printing of Si microwires to secondary flexible substrates.

Chapter 5: Chapter 5 discusses the patterning strategies of metal contacts with Si microwires. Two different transfer printing strategies i.e. stamp-assisted and flip-over transfer printed wires are evaluated. The two types of differently doped p and n-Si microwires are evaluated based on current response and junction behaviour. The resistance response in the metal semiconductor metal (MSM) structure is assessed in planar and bend orientations with and without optical illumination.

Chapter 6: Chapter 6 highlights the fabrication procedure and processing steps involved in the development of a MISFET structure based on single Si microwire. Top and back-gated MISFET structures are fabricated utilizing two different dielectric materials.

Chapter 7: Chapter 7 provides details of the comparative study of the MISFETs devices made of single and multiple Si microwires. Top-gated MISFETs are developed by introducing spray coating as the new deposition technique for dielectric and metal layers.

Chapter 8: Chapter 8 provide the conclusion and future scope of the research work achieved within this investigation.

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Chapter 2
Printable Materials and Technologies

Part of this chapter has been published in:

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2.1. Introduction to Printed Electronics

Printed electronics is the new dimension of microelectronics where functional materials is deposited on a non-conventional substrate either from solution or in the solid state. Printed electronics have gained momentous attraction both for low and high-resolution electronic components that are realized on flexible polymeric substrates. The broader fields of research in printed electronics are divide but not limited to development of printable materials (organic/inorganic), stable flexible substrates with higher thermal budget and reliable printing technologies. Significant progress has been made in all the three fields and a continued research is carried out to get the most optimal results for homogeneous or hybrid flexible electronic components. This chapter highlights and review state of the art of printable materials and printing technologies. Being central to the investigations in this thesis, printing technologies remain the focal point of discussion.

Printing technologies are aiding and revolutionizing the burgeoning field of flexible/bendable sensors and electronics by providing cost-effective routes for processing diverse electronic materials at temperatures that are compatible with plastic substrates. Simplified processing steps, reduced materials wastage, low fabrication costs and simple patterning techniques make printing technologies very attractive for the cost-effective manufacturing [1-4]. These features of printed electronics have allowed researchers to explore new avenues for materials processing and to develop sensors and systems on even non-planar surfaces, which otherwise are difficult to realize with the conventional wafer-based fabrication techniques. For instance, the printed electronics on flexible substrates can enable conformable sensitive electronic systems such as electronic skin that can be wrapped around the body of a robot or prosthetic limbs [5-10]. Printed electronics on polymer substrates has also opened new avenues for low-cost fabrication of electronics on areas larger than the standard wafers available commercially. In accordance with the electronics industry roadmap, the research in this field is slowly inching towards a merge of well-established microelectronics and the age-old printing technologies [11]. This is evidenced by development of devices such as, large area printed sensors [12-15], radio frequency identification tags (RFID) [16, 17], solar cells [18], light emitting diodes (LED) [19] and transistors [20] etc.

Traditional approaches for printing electronics and sensors involve bringing pre-patterned parts of a module in contact with the flexible (or non-flexible) substrates and transferring the functional inks or solutions onto them [17, 19, 21-24]. The two major approaches usually followed for development of printing/coating system are contact and non-contact printing, as shown in Figure 2.1 and described later in Section 3. In contact printing process, the patterned structures with inked surfaces are brought in physical contact with the substrate. In a non-contact process, the solution is dispensed through via openings or nozzles and structures are defined by moving the stage (substrate holder) in a pre-programmed pattern. The contact-based printing technologies comprise of gravure printing, gravure-offset printing, flexographic printing and R2R printing. The prominent non-contact printing techniques include screen-printing, slot-die coating and inkjet printing. The non-contact printing techniques have received greater attractions due to their distinct capabilities such as simplicity, affordability, speed, adaptability to the fabrication process, reduced material wastage, high resolution of patterns and easy control by adjusting few process parameters. [2, 3, 25-28]. Recently, the newly emerging polymeric stamp based printing methods such as nanoimprint, micro-contact printing and transfer printing have attracted significant interest, especially for inorganic monocrystalline semiconductors based flexible electronics [18, 27-32]. This chapter brings together various printing techniques and provides a detailed discussion by also involving the key electronic materials. Critical limitations of each technology have been highlighted and potential solutions or alternatives have been explored. More focus is on the transfer, spray and screen printing technologies, as they are selected for developing a printing platform within this research.

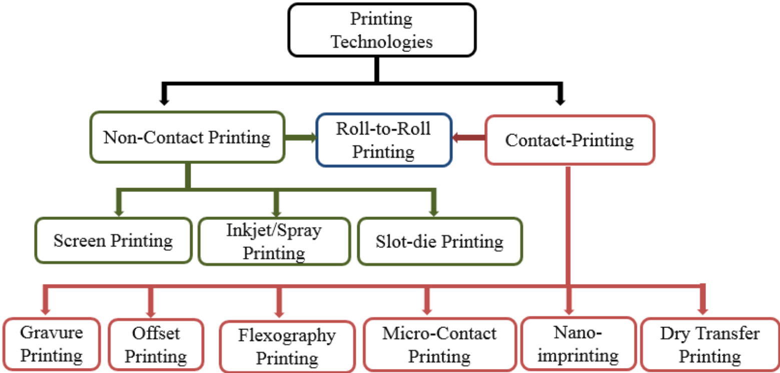

Figure. 2.1. Common printing technologies for solution-processed and solid state materials.

2.2. Printable Materials

Majority of printable materials are in liquid phase, which allow rapid printing on variety of plastic or paper substrates. Selection of these solutions with specific

rheological properties is at the core of developing a reliable printing process. In order to achieve the goal of low-cost and lightweight printed electronics, a large variety of materials (organic and inorganic) have been explored. These materials could be divided into three categories: (a) conductors; (b) semiconductors; and (c) dielectrics [25, 29-32]. Beside these, some composite materials, having dual nature as insulator, ferroelectric, piezoelectric, piezoresistive, and photosensitive properties are also used in thin film printed devices. Hybrid organic/inorganic materials have also been used to compensate for the slow speed organic based electronic devices [28, 31]. Majority of printable materials are in the form of solutions, which require specific properties to allow proper printing on variety of plastic or paper substrates. The following sections discuss the common organic/inorganic materials that are suitable and easily processable through printing technologies.

2.2.1. Conducting Materials

Conducting materials are the main structural blocks of all electronic devices as they form the fundamental part of the device layers or interconnections. Deposition techniques for patterned metal layers and interconnects are now at mature stage with possibility of obtaining structures with controlled thickness and resolution. Various printing technologies require a different set of parameters such as viscosity, surface tension, conductivity and compatibility of the solvents with the underlying materials (in multilayer structures) (Table 2.1) [18]. Properties of these solutions are adjusted according to the desired printing technology by using surfactants and volatile additives. Amongst the list of metals practiced for printed electronics, silver (Ag) based pastes and solutions are the choice of most of the researchers due to its good physical and electrical performance on plastic substrates [25, 27, 29]. Being counted in the category of precious metals, it cannot help to lower the cost of flexible electronic devices, which is the true essence of printing technology. Besides silver solutions, the carbon and copper-based inks are also used. However, oxidation of copper-based inks after printing do not serve the purpose very well [18, 33].

Mimicking metallic conductivity, crystalline organic conductors such as polyacetylene films combined with p-dopants were first reported by Shirakawa et al. Soon after this discovery, the n-type materials were also investigated [34]. Chemical structure of intrinsically conductive polymers can be tailored to get desired electronic and mechanical properties [35]. Majority of the reported organic conductors have compatible work function with p-type semiconductors [30, 35, 36]. Polyacetylene, polypyrrol, polyphenylene, poly (p-phenylene vinylene), polythiophene polyaniline, polyaniline doped with camphor sulfonic acid and PEDOT:PSS (3, 4-polyethylenedioxythiopene-polystyrene sulfonic acid) are some of the most commonly reported hole-injecting polymers used with organic semiconductors. The PEDOT:PSS has been widely studied for transparent conducting polymer anodes as it exhibits a very high conductivity of about 300 S/cm. A detailed description of these materials is given

in [30]. Despite the attractions of low cost and easy solution processing the organic conductors have far less conductivities than conventional metals such as Ag, which has conductivity of ~ 6.30×10^7 S/cm. Another class of conducting polymers developed for printing and flexible electronics is based on nanocomposites (discussed in more detail in chapter 3), made by mixing of metallic nanoparticles with organic elastomers such as (Poly(dimthylsiloxane) PDMS) [37, 38]. Conductivity of such composites is based on the percolation threshold of the fillers. With different ratio of elastomer and nanofillers, the flexible and stretchable conductive sheets and patterns have been investigated in [13-15, 37-41].

2.2.2. Semiconductor Materials

Semiconductor materials are the backbone for developing active flexible electronic and sensing devices. Like conducting materials for printing technologies, the organic/inorganic semiconducting materials are also used for printable sensors and electronics. Inorganic materials have superior properties in terms of performance and stability while solution processable organic semiconductors are attractive due to low cost processing at ambient environment and flexibility. Examples of inorganic semiconductors commonly used for flexible electronics are Si [42-46], oxides of transition metals [47, 48] and chalcogenides [49]. Apart from chemical vapor deposition (CVD) of amorphous silicon for large area flexible electronics, crystalline Si is also used in flexible electronics by employing dry printing technique (central to investigation within this thesis and discussed in more detail in chapters 4-7) [43, 50]. Oxides of transition metals are sometimes used in flexible electronics but through vacuum deposition techniques other than printing. ZnO and GIZO can be solution processed and even printed but sintering temperature of 300–500°C is necessary to achieve optimum mobility [32, 51]. Very few works have been reported on solution processed inorganic semiconductors and their compatibility with the usual printing techniques [25, 32, 52].

From printability viewpoint, the solubility and proper dispersion of organic semiconductors are the important parameters. Commonly used solution processed organic semiconductors, having acceptable charge transport and mobility include regioregular poly(3-hexylthiophene) (P3HT), poly(triarylamine), poly(3,3-didodecyl quaterthiophene) (PQT), poly(2,5-bis(3-tetradecyllthiophen-2-yl) and thieno[3,2-b] thiophene) (PBTTT) [30, 35]. Fullerenes and solution processable derivatives such as phenyl-C61-butyric acid methyl ester (PCBM) blended with P3HT are some of the commonly used electron donor and acceptors in the bulk heterojunction devices [53, 54]. Additionally carbon nanotubes and graphene are also currently under investigation for their high-mobility [55]. Stability and reliability of organic materials for long time processing is very challenging especially the low ionization energies are prone to oxidation, which results in slow responses and degradability of the devices. Further, developing printable n-type organic semiconductor is challenging due to instability,

which is becoming one of the serious obstacles in development of organic CMOS devices [56, 57].

2.2.3. Printable Dielectrics

For applications requiring high capacitance in multi-layered printed structures, thin layers of dielectric materials are essential for proper insulation to prevent leakage currents and sometimes to obtain low voltage operation for field effect devices. A uniform layer of dielectric is needed to promote the activation of the medium caused by electric field or other transduction phenomena. Inorganic materials, such as silica, alumina, and other high permittivity oxides often used in electronics on flexible substrates are usually not printable [2, 3, 25-27, 32]. Low cost organic dielectric materials that are available in large quantities and can be dissolved in various solvents and solution can be printed easily as compared to inorganic counterparts. In most of the printed electronics, semiconductor/dielectric interface is of prime importance for the high performance and stability of the devices. Self-assembled monolayers are sometimes used for modification of the dielectric surface. Some of the commonly used organic dielectric materials in printed electronics are poly (4-vinylphenol) (PVP), poly (methyl methacrylate), Polyethylene Terephthalate, Polyimide, Polyvinyl alcohol and Polystyrene. [2, 3, 25]. Spray coating of the dielectric materials is an interesting and materials efficient technique, which is also employed in this research for deposition of PMMA (discussed in chapter 7). Besides dielectric layer, solution processed organic dielectric materials are also used for final encapsulation of printed devices.

2.3. Printing Technologies

The development of thin film devices either by the use of printing or coating of hybrid organic/inorganic materials is one of the many ways explored to simplify processing steps, facilitate location specific deposition and enhance the production speed. The chemical solution or nanoparticles of functional materials are used in the form of colloidal solution in most of printing technologies summarized in Table 2.1. These solutions are deposited directly on rollable substrates using controlled dispensing processes or coated on substrates using controlled pressures and speeds [28, 52, 58-60]. The key benefit of printing techniques is the reduction in material wastages, as the solution is printed on the defined location in single step and the residual solution is collected back for subsequent use. These dispensing and coating processes have led to promising results especially with organic materials, as organic thin film transistors (TFT), OLEDs, sensors, solar cells, RFID tags, printed batteries and capacitors have been demonstrated, summarized in Table 2.2 [1-3, 25, 26]. An important benefit of printing technologies is that they enable production of large area electronics and sensors by R2R manufacturing in a cost effective way.

Printing technologies are divided into two broad categories, as shown in Figure 2.1. The contact and non-contact based patterning discussed in this section follow the classification given in Figure 2.1 and the state of the art, the pros/cons, prospects and the challenges of these printing techniques are discussed subsequently.

2.3.1. Contact-based Printing

Contact based printing technologies are those processes, where the functional materials are transferred on the target substrate through a physical contact of the transfer media. Materials are picked through patterned structures and printed on the desired substrate. Contact based printing is broadly divided into two major streams depending on the phase of the functional material. The first one includes the printing mechanism by which material in the form of chemical inks or colloidal solutions is used to pattern. While the second one employs the mechanism, in which solid-state materials especially inorganic semiconductors are printed on secondary substrates through transfer printing techniques.

The prominent techniques used in contact-based printing of solution-based materials include gravure printing, gravure offset printing, flexographic printing, microcontact printing and nano-imprint lithography. Gravure printing utilizes direct transfer of functional inks through physical contact of the engraved structures with the substrate [3, 27, 61, 62]. It is capable of producing high quality patterns in a cost-effective manner typical of a R2R process. The gravure printing tools consist of a large cylinder

Table 2.1

Comparison of various printing technologies [4]

Parameter	Gravure	Offset	Flexographic	Slot-die	Screen	Inkjet	Microcontact & Nanoimprint	Transfer
Print Resolution (μm)	50-200	20-50	30-80	200	30-100	15-100	1-20	4-50
Print Thickness (μm)	0.02-12	0.6-2	0.17-8	0.15-60	3-30	0.01-0.5	0.18-0.7	0.23-2.5
Printing Speed (m/min)	8-100	0.6-15	5-180	0.6-5	0.6-100	0.02-5	0.006-0.6	NA
Req. Solution Viscosity (Pa. S)	0.01-1.1	5 – 2	0.010-0.500	0.002-5	0.500–5	0.001-0.10	~ 0.10	NA
Solution Surface Tension (mN/m)	41- 44		13.9 -23	65-70	38-47	15-25	22-80	NA
Material Wastage	Yes	Yes	Yes	Yes	Yes	No	Yes	No
Controlled Environment	Yes	Yes	Yes	No	No	No	No	Yes
Experimental Approach	Contact	Contact	Contact	Contact-less	Contact	Contact-less	Contact	Contact
Process Mode (sample pattern line)	Multi-steps	Multi-Steps	Multi-steps	Single-Step	Multi-Steps	Single-Step	Multi-steps	Multi-Steps
R2R Compatibility	Yes	Yes	Yes	Yes	Yes	Inter-mediate	Yes	No
Hard Mask Requirement for each Printing Step	No	No	No	No	Yes	No	No	Yes
Printing area	Large	Large	Large	Large	Medium	Large	Medium	Medium
References	[5, 27, 30, 61, 63, 77]	[27, 30, 78-80]	[27, 30, 63] [9, 68, 81, 82]	[83-87]	[27, 30, 88-91]	[27, 31, 70, 92, 93][74][35, 69, 94]	[4, 8, 95-101]	[33, 49, 102-106]

electroplated with copper and engraved with micro cells. Ink is transferred through capillary action onto a rollable substrate when it comes in between the engraved and impression cylinders. In gravure offset printing, an extra elastic blanket is used, which picks up the ink from grooves of the cylinder and transfers it to the targeted surface [3, 63]. Dependence on the printing speed and blanket's thickness are more dominant parameters due to the minimal contact time between ink and the blanket [61, 64, 65]. Flexographic printing is used for high-speed runs of printed electronics and is more attractive than gravure and offset for high-resolution patterns [3]. A wide variety of ink can be printed with a rubber or polymer plate having raised patterns that are developed by photolithography and are attached to a cylinder. On contact with the inked areas of the annilox cylinder, these raised patterns on plate cylinder serve to print on the substrate running between print/plate and impression cylinders. These technologies have long been used in the text printing/press and the optimized processing could easily be implemented for printing electronic structures on flexible substrates. The roll-to-roll (R2R) capabilities of these technologies have fascinated the rapid fabrication of electronic devices at depreciated manufacturing costs. The manufacture process is very simple and varies slightly for each based on different features such as high resolution, low principal costs and reliability of the system for printable materials.

The other prominent contact based printing for patterning solutions of functional materials is through a soft polymeric stamp. The patterned structures are replicated on a mouldable polymer (usually PDMS) from a master mold. The master mold is developed through micromachining for low resolution and photolithography for high-resolution structures. The technique usually termed, as soft lithography is a low cost technique from processing point of view, as the principal cost in only involved in developing a single master mold. The noticeable techniques developed for this approach include micro-contact printing (μCP) and nano-imprint lithography (NIL). μCP is an effective technique for preparation of substrates and patterning a wide range of materials, which are sensitive to light, and etchants. A conformal contact of patterned elastomeric stamp with target surface is the key requirement for successful transfer of structures. Microcontact printing has the ability to produce multiple copies of 2-dimensional patterns by using patterned stamp developed through master mold [24, 66-68]. Poly (dimthylsiloxane) (PDMS) is the frequently used elastomer due to its extraordinary properties as compared to other elastomers [24, 68-70]. NIL on the other hand, is used to pattern materials by mechanical and physical deformation of wet layer using hard or soft mold followed by different temperature processes. The system consist of a mold with nano-scale patterned structures on the surface that is pressed into a solution cast on a substrate at a controlled temperature and pressure [71]. The two most crucial processing steps that influence the pattern quality and throughput are resist filling and demold characteristics. A controlled pressure is needed not to destroy the imprint patterns [21]. Diverse NIL approaches are developed i.e. thermal, photo, ultraviolet (UV), step-and-flash and roller nanoimprinting [71-74].

2.3.2. Transfer Printing

Transfer printing is one of the most attractive techniques in contact based printing processes recently developed. As against patterning solution based functional materials, transfer-printing technique is used for processing materials in their solid state. Transfer printing involves the translation of inorganic elemental or compound semiconductor microstructures from standard donor wafers onto a secondary substrate. This is one of the focal printing technologies selected within this research for development of electronic devices on flexible substrate. Details about the development and processing steps of the printing technique are provided in a much more comprehensive way in chapters 4-7. This technique is adopted to develop fast flexible electronics, through translating silicon microwires onto secondary substrates and embedding them in solution based materials for getting resistor, metal semiconductor metal (MSM) and metal insulator field effect transistors MISFET structures. This technique has gained significant interest in the research community and the process has already been optimized for development of a variety of devices and circuits. Conventional photolithography technique is used to get micro and nanowires of Si on the wafers itself and then transferring them onto flexible substrates through flip-over (Figure 2.2) or a

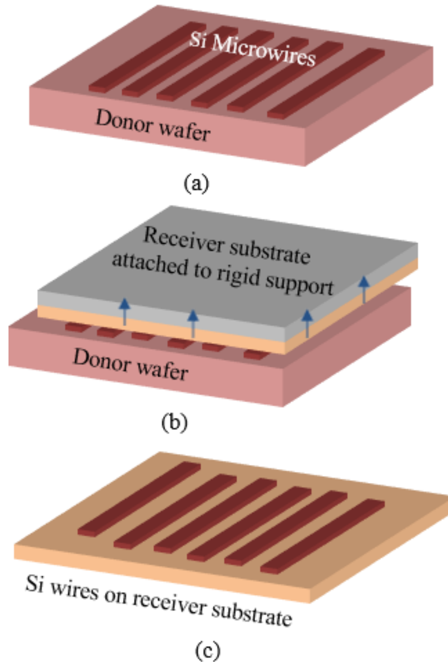

Figure 2.2. Schematics of flip-over transfer printing (a) Si microwires on donor wafer, (b) conformal contact of receiver substrate with an adhesive side facing Si microwires (c). Si microwires transfer to receiver substrate after peel-off.

stamp-assisted transfer (Figure 2.3) approaches [75-79]. Very well developed manufacturing and processing technologies for electronic grade silicon constituting high levels of purity, surface smoothness, control over crystallinity, doping concentration and type, and the resulting high carrier mobilities make it a distinguished candidate in the current scenario of large area electronics as well.

The two techniques used for transfer printing i.e. flip-over and stamp-assisted vary in the number of processing steps and approach to translate microstructures from donor wafer. Flip-over technique is a single step process, where the adhesive side of the target substrate is brought in conformal contact to the donor wafer and retracted back immediately as shown in Figure 2.2. This is a very robust technique of transferring microwires but at the cost of losing the top finished surface of the Si device layer. Additionally, it is impossible to pre-pattern or pre-process the substrate due to the degradation of the adhesive receiving layer. The post-processing of microwires is also challenging as the commonly used scotch tape adhesive, which affects the attachability of the microwires to flexible substrates upon treatment with chemicals. Stamp-assisted transfer printing is an attractive alternative used for deterministic assembly of Si microwires with top surface available for post-processing on a pre-processed substrate. A conformable PDMS stamp is used to pick up the freestanding microstructured silicon

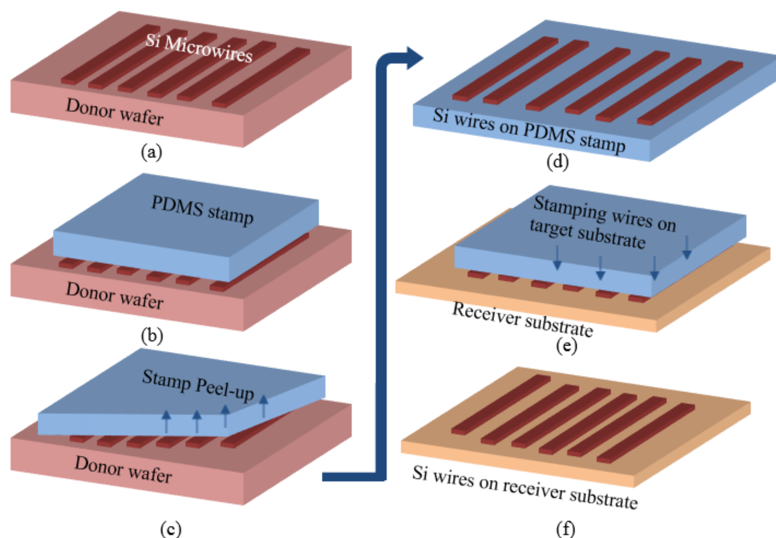

Figure 2.3. Schematic of the process flow of stamp-assisted transfer printing and fabrication steps for silicon microstructures. PDMS is used as transfer element: (a) lithographic patterning and etching using DRIE on wafers; (b) chemical etching of SiO2 under the microstructures; (c) bonding of carrier substrate i.e., PDMS with microstructures; (d) peeling off PDMS with microstructures; (e) microstructures transferred to PDMS; (f) stamping PDMS with microstructures on final receiver substrate i.e., polyimide; (g) peeling off PDMS, leaving behind microstructures on polyimide; (h) microstructures finally transferred to the receiver substrate.

from top of Si wafers after etching and transferred with controlled orientation to flexible substrate. Figure 2.3 shows the processing steps involved in realizing Si microwires and their transfer to secondary substrate. The PDMS stamp is peeled back retrieving the Si ribbons with fast speed enhancing the kinetic control of adhesion [80]. Rate dependent adhesion and printing of the solid structures with high peel velocity (typically 10 cm/sec) and low stamping velocity (~1 mm/sec) respectively has been investigated [81]. The mechanics of kinetic dependence of switching of adhesion has its origin in the viscoelastic response of the elastomeric stamp. Adhesiveless stamping like this is very valuable for wafer-based microstructures printing, to operate it from moderate to high temperatures [75]. Nanostructures through bottom-up approach are also being explored. The main challenges in the bottom-up approach of fabricating microstructures relate to control of dimensions, uniformity, the doping levels, crystallographic orientation and purity of the material. Also for scalable integration over large areas, producing well-arranged arrays of these structures are challenging [82]. Besides deploying nano/microstructures onto secondary substrate by the usual dry transfer printing through PDMS stamp, solution based printing by casting the microstructures in a solution are also practiced. Although manufacturability of wet transfer (through fluid) of structures is unclear as the doping levels and uniform surfaces are not well-recognized [83].

Based on the active area needed and subsequent alignment defines the methodology for either using strips or membranes of Si in the transfer printing process for flexible electronic devices. Although both the approaches have pros and cons in relation to alignment and ease in undercutting of the structures due to the exposed area for etchants both for Si and buried oxide (BOX). The backside surface quality is acceptable in the flipped transferred NMs but the non-uniformity of the doping profile on the backside is the main limitation. Solid source diffusion has the issues of large feature sizes and driving the dopants in larger depth in NMs increasing sheet resistance. Instead ion implantation is employed which gives good results [76]. Simple integrated circuits like NMOSFET, CMOS inverters, sensors, three and five stage ring oscillators and differential amplifiers are reported to be developed on a flexible polyimide substrate using transfer printing of Si micro ribbons [77, 78, 84, 85]. Thermoelectric energy harvesters by transfer printing of arrays of alternately doped Si wires have also been reported in literature [79]. Flexible TFT with 1.5μm channel length was developed on plastic substrate showing very high frequency ranges in GHz. Radio frequency (RF) characterization under bending conditions showed slight performance enhancement with larger bending strains [86, 87]. Device performance can further be enhanced by using strained silicon channel [88]. A single-pole through switch containing two PIN diodes were realized and transferred to polymer substrate, by doing selective doping of 200-nm thick and 30um wide SiNM on SOI wafer.

The rigid microstructures on flexible electronics experience tensile and compressive strains during bend into convex and concave shapes. The employment of these structures onto flexible substrates strongly depends on the failure mechanisms like interfacial slippage and delamination. The dimensions and mechanical properties of

micro/nanoscale semiconductor wires, ribbons, bars, or membranes determine their bending mechanics. A practical design rule might be that the silicon strain must remain below 0.1%, which leads to a degree of bendability of r~2.5 cm for polymer substrate, which is still sufficient for many devices and applications [31, 89, 90]. Skinniness size of the Si nano membranes (SiNM) permit the planar-type structure to have very high level of mechanical bendability [91]. Rigorous necessities of active circuitry for large-area RF systems that could operate in L-band and even higher are required for flexible electronics applications [92]. Successful development of technology protocol for transferring Si based structures can complement the slow speeds of organic materials, which could balance the total cost of manufacture of flexible devices. Challenges of misalignment of neighbouring strips movement during undercutting, registration of pre-doped regions, gate dielectric materials at low temperatures and surface related issues for the stamps are very critical to be controlled [81]. Development of the Si microwires designs and the optimized approach for transferring Si microwires form donor (SOI) wafer to secondary flexible substrates are explored in full detail in chapters 4-7. The successful fabrication by embedding of Si microwires in diverse organic and metallic materials for realizing MISFET structures are presented in more detail.

2.3.3. Non-Contact Printing

Non-contact printing technologies are completely solution-based processes in which the functional materials are patterned or coated in a single deposition step. Non-contact printing, as evident form the name itself are the printing technique which do not require physical contact of a pre-patterned inked structures to the target polymeric substrates. The solution is deposited through a screen mask or nozzle, which are connected to a continuous delivery of solution. Non-contact based printing has been emerged as the revolution in the field of printed flexible electronics as these enable the fabrication of multi-layered 3D structures. The efficient use of solutions by using very small quantity of materials and collection of the residual inks for subsequent uses make these processes more simple and cost-efficient. Several non-contact printing techniques have been developed such as inkjet printing; spray coating, slot-die coating and screen-printing. Screen-printing and inkjet/spray coating techniques are potentially explored within this thesis for deposition of diverse metallic and organic based solutions. Especially screen-printing has been utilized both for patterning metal contact for back-gates MISFETs as well as for printing large area pressure sensors based on two different transducer materials. This section include overview and state of the art accompanied by operation mechanism and potentials of these various non-contact based printing techniques.

2.3.4. Screen Printing

Screen-printing is the most popular and matured technology for printed electronics as it has been practiced in electronics industry for long time to print metal interconnects on

printed circuit boards. It is faster and more versatile in comparison to other printing tools, as it adds simplicity, affordability, speed and adaptability to the fabrication process. The results from screen-printing can be reproduced by repeating a few steps and an optimum operating envelope can be developed quickly [3, 25, 53, 59, 93, 94]. Two different assemblies of screen printers i.e. flatbed and rotary are used for R2R manufacturing described in Figure 2.4(a-b) respectively [3]. Screen printer has simple setup comprising of screen, squeegee, press bed, and substrate, as shown in Figure 2.4. In flatbed, the ink poured on the screen is squeegeed to move across the screen resulting in its transfer through the stencil openings to the substrate beneath it. For optimization of the materials and processing steps, flat bed screen-printing is a powerful tool for small laboratory systems. Flatbed screens can be substituted by rotary screen for continuous processing in which the web of the screen is folded while the squeegee and ink are placed inside the tube.

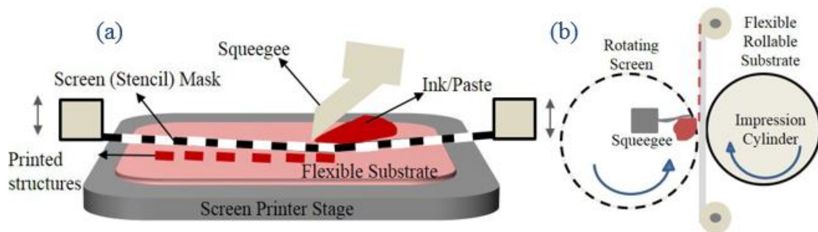

Figure 2.4. (a) Flatbed screen printing with planar substrates for solution dispensing, (b) Rotary screen printer with moving substrate (web) between cylindrical mask and impression cylinder.

Relatively high speeds can be achieved by rotary screen as compared to flatbed, but the screens for rotary setup are expensive and very difficult to clean [3, 61]. Although a very simple process, the print quality and characteristics are affected by various factors such as solution viscosity, printing speed, angle and geometry of the squeegee, snap off between screen and substrate, mesh size and material [59, 95, 96]. The paste viscosity and surface tension of the substrate are important for complete dispensing of the paste through the screen mask. Screen printing technique is usually compatible with the high-viscosity inks as the lower viscosity inks will simply run through the mesh rather than dispensing out of the mesh [28, 97]. Without giving any consideration to proper tuning of the ink properties and mesh count, the nominal values of 50-100µm are common print resolutions and wet thicknesses of a few microns. The possibility of printing relatively thick layers could enable printing of low-resistance structures, also with conducting polymers, by compensating the high resistivity with a thicker layer [25].

In addition, a compromise between surface energies of substrates and surface energies of the inks is important for high-resolution line widths [97-99]. The reduced surface energies of the substrates reduce the wettability of the solution, which results in improved line resolution. If the critical surface tension of a substrate is lower than the surface energies of inks, good resolution can be achieved even with low viscosity inks.

Although high viscous inks are required to minimize ink flow on the substrate, the low viscosity is desirable to dispense the solution through the mesh to realize structures with fine edges and resolution. In this scenario, the low viscosity inks are preferred as the wettability of the substrate can be controlled by adjusting the surface energies of the substrate. The low viscosity inks possess high degree of flowability, which reduces the chances of mask blockage, and leads to even edges of printed lines and, smooth surface of the printing films [97, 99]. Material, strength and number of meshes in screen also play a major role in high-resolution patterning, as screen is developed by using different sizes of mesh openings and several materials ranging from polyester to stainless steel. The technological development in the screen mesh is made by modifying the silk strength by using materials such as nylon, polyester and stainless steel. The increase in the strength of the mesh wire material used in the screen mask and the mesh count result in improved printing quality. For printing stability during mass production, a screen made of stainless steel mesh with three times more in strength than conventional stainless steel mesh has also been developed [95, 100].

The feasibility of screen-printing for flexible electronics has been demonstrated through a number of printed sensors, electronics devices and circuits. For example, all screen printed TFTs have been demonstrated in [93, 101, 102]. Screen-printing was claimed to be used for the first time to develop OLEDs by investigation the process and solution parameters i.e. viscosity of the solution and mesh count of the screen [95]. Multilayer high-density flexible electronic circuits, connected through micro via holes

Table 2.2

Comparison of electrical characterization results of sample devices developed with different printing technologies and materials. [4]

Printing Technology	Material (Organic/Inorganic)	Mobility (cm^2/V.Sec)	On/Off ratio	Thr. Vol. (V)	Reference
Flexography	P(NDI2OD-T2) (Organic)	0.1 - 0.3	10^5–10^6	10.20	[68]
Flexography	GSID 104031-1 (Organic)	1.8-4.1×10^{-3}	N/A	6	[63]
Flexography	6,13-bis triisopropylsilylethynyl) (Organic)	2.0-5.8 ×10^{-3}	N/A	5.1	[63]
Gravure	SW-CNTs (Organic)	0.04-0.17	10^3-10^5	-4.5	[61]
Gravure	P(NDI2OD-T2) (Organic)	0.1 - .2	10^5-10^6	5	[68]
Gravure	SW-CNTs (Organic)	0.07-.15	10^3-10^4	-20	[68]
Inkjet	TIPS–Pentacene (Organic)	0.15-.53	10^6	2	[69]
Inkjet	P(NDI2OD-T2) (Organic)	~ 0.1	~10^5	~ 10	[68]
Inkjet	C60, fullerene (Organic)	2.2-2.4	10^7-10^8	5	[70]
Inkjet	P3HT/PS (Organic)	0.02	10^6	>30	[71]
Nanoimprint Lithography	Poly(3-Hexylthiophene) P3HT (Organic)	0.86 - 0.98	7.02 × 10^3	15.7	[72]
Screen	Dinaphtho-Thieno-Thiophene (DNTT) (Organic)	0.33	10^4	N/A	[73]
Transfer	µs-Si (Inorganic)	105	10^2	~1.5	[74]
Transfer	Poly-Si (Inorganic)	30	N/A	10	[75]
Transfer	Single-Si (Inorganic)	230	>10^5	~1	[76]
Transfer	Single-Si (Inorganic)	300	N/A	N/A	[75]

with embedded passive and optical devices, have been realized by using advanced screen printing processes [59]. Screen-printing is also used for patterning to develop shadow masks for fabrication of organic TFT. Screen printed electrical interconnects for temperature sensor on PET substrate are reported in [99]. The large area flexible pressure sensors are fabricated by utilizing two polyimide films as top and bottom films and connecting the electronic circuits through micro via holes. An all screen printed pressure sensors developed also in this research and explained in more detail in chapter 3, by using piezoelectric Poly(vinyledene-fluoride-trifluoroethylene) (PVDF-TrFE) and piezoresistive multi wall carbon nanotubes (CNT) in Poly(dimethylsiloxane) (MWCNT/PDMS) nanocomposite materials [13-15]. All structures of metal plates, interconnects and sensitive materials are deposited by using screen-printing technology. Entire structural features of a humidity sensor including the interconnect patterns and protective polymer layers are also screen-printed [94, 96, 103]. Screen printing of cobalt hydroxide has been reported for obtaining supercapacitors [104]. The simulated R2R process is used for monitoring the structural properties of moving screen-printed interdigitated electrodes recently [105].

Unlike many other manufacturing techniques, the screen-printing does not require high capital investment. Accompanied by some supplemental methods such as inkjet technology, vapor deposition and laser processing, screen-printing is employed in most of the production lines of printed electronics. Using the supplemental technologies often results in cost reduction [100, 106]. Despite these attractions, screen-printing also poses a few challenges for developing all layers of a flexible device. These include high wet thickness of the film, exposure of the ink to atmosphere and the dry out of the ink on the mask that deteriorates the mask designs of the screen [53]. However, the advantages such as high definition and high precision of multilayer structures add to the figure of merits of the screen printing techniques as compared to other deposition techniques for large-scale production.

2.3.5. Inkjet Printing and Spray Coating

Inkjet printing is the rapidly emerging technique for direct patterning of solution based materials deposition. Materials in the form of colloidal or chemical solution are

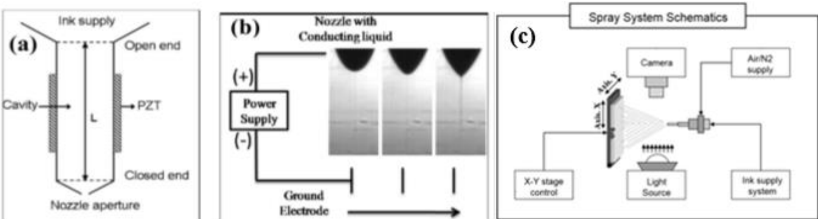

Figure 2.5. (a) Schematic of the piezoelectric inkjet head, with PZT actuator [1]. (b) Schematic description of Electrohydrodynamic inkjet system. Electric field is generated between nozzle and counter electrode [15]. (c) Description of Electrospray system with complete setup [19, 21].

deposited through a micrometre sized inkjet nozzle head. A number of mechanisms for actuation of inkjet nozzle head have been developed. Among these, the most prominent techniques are thermal, piezoelectric and electrohydrodynamic inkjet systems. Droplets (often called Drop-on-Demand (DoD)) of very small dimensions are ejected at the corresponding pulse generated by either thermal or piezoelectric actuators used in the inkjet nozzle head [107-110]. The Figure 2.5 (a-b) shows the mechanism of droplets actuation through piezoelectric and electrohydrodynamic setups. In electrohydrodynamic printing, solution is ejected by generating a high electric field between the nozzle and a counter electrode. A stable cone jet is the primary requirement of electrohydrodynamic inkjet system. The type of applied voltage defines the mode of ink ejection from the nozzle. DC voltage results in an intact jet while AC voltage at different frequencies and functions define the drop-on-demand mode of the system. An intact jet can be utilized for continuous patterning of solution as well as drop-on-demand similar to thermal and piezoelectric nozzle heads [111].

Another interesting feature of electrohydrodynamic printing is the spray coating of

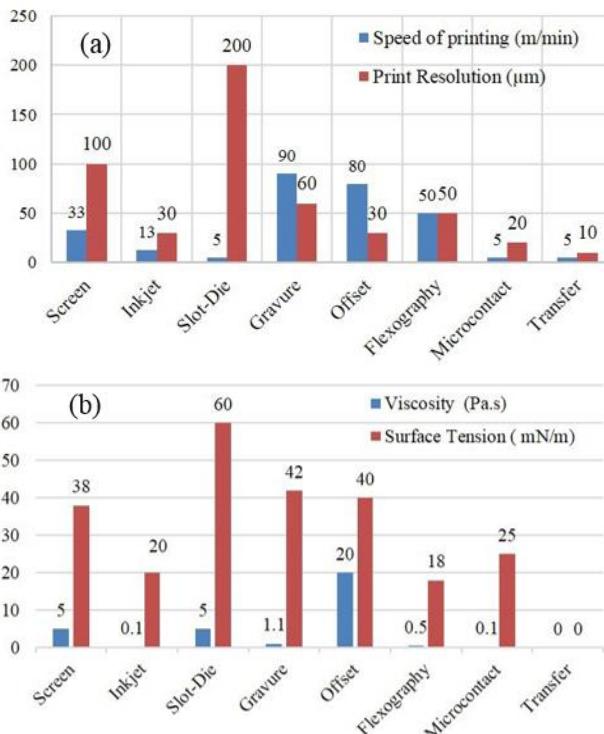

Figure 2.6. Graph showing maximum values reported for Speed of printing and Print Resolution based on the data from Table II. Graph showing maximum values reported for viscosity and surface tension required for printing techniques based on the data from Table 2.2.

colloidal solutions shown in Figure 2.5 (c). Thickness in the range of nanometres can easily be achieved just by increasing the electric field value along with the distance between nozzle and substrate. A very fine layer of conductor, semiconductor and insulator can easily be deposited by adjusting the conductivity and viscosity of the solutions to obtain a stable cone jet. This technique has been successfully utilized in fabrication of a range of electronic devices and in biological systems [52, 112-114]. Besides electrospray deposition, some researchers are also exploring "Aerospray" for thin film deposition and patterning of electronic materials [115, 116]. Inkjet printing has been used to fabricate TFT consisting of ZnO and PVP as the active device region and gate dielectric respectively [117]. A high performance n-channel transistor with uniform amorphous C60 Fullerene is developed by using inkjet printing and vacuum drying process [58]. Complementary circuits composed of pentacene and a xylene carboxylic diimide derivative of p and n-channel TFTs are also fabricated on flexible foils. Staggered configuration of TFTs is followed for development of a flexible CMOS device, by printing both the n and p-type organic materials separately using inkjet technology. The misalignment between energy levels due to the wide band gap of organic materials results in large barriers for charge injection, causing in reduced performance of the circuit [118]. Resistors, capacitors and inductors are developed using inkjet printing on polyimide substrate with various functional inks [60]. Inkjet in comparison to flexography, spin coated and gravure printing generally results in rougher and far less uniform morphologies with only partial uniform coverage of the channel region [119]. Chemical stability, solubility in common solvents, inexpensive and low temperature processing are some of the key requirements of inkjet printable

Table 2.3

Summary of Non-contact printing technique and challenges [4]

Print Type	Mechanism and Features	Challenges
Screen	1. Most mature conventional printing technique. 2. Controlled deposition with fast speeds and versatile. 3. Desired pattern defined by open area of mesh. 4. Paste, printing process, substrate. 5. Squeegee, pressure and screens.	1. Drying of solvents in mask and deteriorated printed patterns. 2. High-resolution uniform line patterns not possible <30 µm. 3. High viscosity required to prevent spreading and bleed out. 4. Dry out of the ink on the mask when kept for long time. 5. Large wet thickness of printed films and high surface roughness.
Inkjet	1. Low viscosity needed as compared to other techniques. 2. Ejection of droplets by using different actuation phenomena. 3. Thermal, Piezoelectric, and Electrostatic driven printer. 4. Position specific deposition of droplets. 5. Low material wastage.	1. Periodic bulging of lines with high contact angle in droplets. 2. Coffee-ring effect due to unequal distribution of dried solute. 3. Slow speed, multinozzle in parallel, misfiring, clogging. 4. Pixilation-related issues due to drop-on-demand. 5. Chaotic droplets at high frequencies and splashes with printed lines.
Slot-Die	1. Uniform film thickness can be determined by controlling the feed rate and coating speed. 2. The first step establishes steady and uniform coating flow. 3. Second step adjusts gap between slot die and moving web. 4. Defect-free in long-time steady operation after adjustments. 5. Prewetting on die surface, fluid viscosity, slot gap, coating gap, and die lip length.	1. Operating window of operation is bound by a minimum and a maximum coating speed for uniform coatings. 2. Various coating defects, such as dripping, air entrainment, ribbing, etc. are observed outside the region. 3. Wastage of solution and unnecessary edge effects due to inefficient transient operation. 4. Proper control of start-up and shut-down periods are important.

Table 2.4

Summary of contact-based printing technologies and challenges. [4]

Print Type	Mechanism and Features	Challenges	References
Gravure	1. Ink pick-up by the engraved cells of the cylinder. 2. Substrate properties of interest - smoothness, compressibility porosity, ink receptivity and wettability. 3. Ink properties of interest - ink chemistry, viscosity, solvent evaporation rate and drying. 4. Doctor blade, angle and impression pressure, printing speed and uniformity of the gravure cylinder diameter.	1. Cylinder life and higher cost. 2. Proper ratio of cell spacing to cell width. 3. Consistent straight printed lines with fine edges. 4. Defects related challenges due to contact printing techniques 5. Pick out effect due to direction of trenches to printing patterns 6. Enhancement of reliability for printed electronics. 7. Large degree of control for size and shape of conductive lines.	[3, 5, 27, 29, 30, 61, 63, 74, 118]
Offset	1. Elastic blanket roll picks up the ink from the grooves of the gravure plate and transfers it to the target surface. 2. The goal of the set process is 100% transference. 3. Enables the printing of ink onto hard surfaces. 4. Main process parameters are roll speed and pressure.	1. Width of the printed line increases with solvent absorption. 2. Lifespan of blanket expires quickly with absorbing solvent. 3. Viscosity thickening decreases blanket's absorbing power. 4. Spreading of line during set process. 5. High rolling resistance due to the fast rolling speed. 6. Wave like pattern's edge with the vertical direction.	[3, 12, 27, 30, 74, 98, 110, 111, 116-118]
Flexographic	1. Patterns are raised on low-cost flexible plate (attached to a cylinder) using photolithography. 2. High flexibility and low pressure imposed on substrate allows using this process for fragile and stiff substrates. 3. Better pattern quality and integrity in both vertical and horizontal compared to gravure.	1. Divergence from nominal specified values with squeezing. 2. Marbling effect, a typical printing problem. 3. Alignment of multi layers transfer appears cumbersome. 4. Tensile stresses occur with solvent evaporation o temperature. 5. Surface roughness of printed patterns approximately 6-8μm. 6. Layer cracks and non-uniform films.	[3, 9, 11, 27, 30, 63, 78, 98, 119-121]
Micro-Contact	1. Masters developed by photolithography and CNC. 2. Stamp is "inked" and put in contact with the substrate surface and transfer occurs at point of contact. 3. Straightforward method for the preparation of micro and nanostructured surfaces. 4. Mostly employed by the biological sciences	1. Peeling stamp from master with nano-structures corrugations. 2. Hydrophobicity of PDMS is a problem with polar inks. 3. Swelling of the stamp during inking increase the pattern sizes. 4. Diffusion of imprinted molecules on patterned surface. 5. Pattern reproduction challenge due to forces exerted or stamp. 6. Pairing, buckling or roof collapse of structures during contact.	[4, 8, 123-125, 128, 130, 135, 136]
Nano-Imprint	1. A hard mold developed by Photolithography that contains nanoscale surface-relief features. 2. Master pressed into a polymeric material cast at a controlled temperature and pressure. 3. Creating a thickness contrast in the polymeric material.	1. Damage to the fragile nanostructures when removing. 2. Coefficient of thermal expansion of master and polymer 3. Defect density control is the stringent requirement.. 4. More time required per replication for heating and cooling. 5. Vertical and lateral collapse of the replica features. 6. Poor fidelity of replication of nanostructures less than 50 nm	[4, 8, 123-125, 128, 133-136]
Transfer	1. Wires and membranes realized on SOI or bulk wafers using standard photolithography. 2. Transferring the structures using PDMS stamp onto the flexible substrates. 3. Transferring and printing through solution casting. 4. Photolithography + Micro Contact printing.	1. Misalignment of neighboring strips during undercutting. 2. Registration of pre-doped regions of transferred nanomembranes. 3. Active area needed for device & using strip or mesh NM. 4. Undercutting of strips and meshes based on exposed area. 5. Gate dielectric at low temperatures needs to be explored. 6. Stamp related issues as described in micro-contact printing. 7. Surface manipulation of the stamp for efficient transfer. 8. Backside surface quality of flipped transferred structures. 9. Doping profiles of flipped & non-flipped structures.	[33, 137-140, 142-148, 150, 151]

materials alongside excellent charge transport in ambient conditions.

Development of colloidal solution for proper ejection of droplets on a targeted area by keeping an acceptable quality of the printed circuits is challenging due to the influence of evaporation rate of the solvents and orientation of the active particles. Slow speed due to limited number of nozzles and possible clogging renders to the complexities of the inkjet system. Low throughput due to slow speed of inkjet printing process is a challenge for becoming an industrial production technique for printed electronics instead of its very promising results on laboratory scale. Low pattern resolution in the range of 20-50 µm and more, adds to the issues of inkjet system due to the spreading of solution on target substrate and chaotic behaviour of droplets during the time of flight. Necessary modifications to the viscosity, concentration and solvent system are needed for proper ejection of the droplets without blocking the nozzle. Spreading of droplets, bulging out of the ink after sintering due to hydrophobic substrates, shape, thickness and morphology of the dried droplets has to be controlled [28, 61]. Different techniques for controlling wetting/dewetting of printed patterns on flexible substrates are already under investigation and techniques like modifying surface properties of substrates by plasma treatment [120], localized micro-plasma treatment [121], tailoring adhesion and cohesion of ink particles within and with substrates [122], and adding gelating polymers [123] have been developed.

Significant progress has been made in design, technical and process capabilities of printing technologies in recent years. Much more work needs to be done before the field is ready to be scaled up for R2R process technology [106, 124]. Organization of the different film forming techniques according to the distinct categories of coating and printing is not straightforward. It is critical to develop a mechanics model to eliminate the gap between the conceptual design, materials and the process parameters [125]. One of the main challenges is how to model the effects of material, structure, and process together and optimize them to make reliable multi-layered flexible sensors and devices with acceptable performance. Some of the other challenges are those that relate to the cost and performance of flexible circuits, panel size, process throughput, substrate distortion, barrier layer technology and yield of the process on which R2R technology is based [3, 106, 126-128]. Despite the vigorous attractions of large area flexible sensors and electronics, this new technology must overcome significant technical and process challenges in order to gain ground for practical high volume applications [106, 128].

Figure 2.6 (a) & (b) summarize the common features of various printing technologies. Figure 2.6 (a) shows the comparison of printing speeds and capability of print resolution that could be achieved by each printing technology. Whereas Figure 2.6 (b) shows the common material’s properties, i.e. viscosity and surface tension of the solutions used in printing technologies. Table 2.3 and Table 2.4 summarizes qualitatively the mechanism, process requirements, materials and critical limitations of non-contact and contact printing technologies reported in literature. Main features of all the printing technologies are highlighted to explore the possibilities of merging different techniques to develop a common manufacturing platform where limitations of one

technology can be overcome by using another. Attractive features of high-resolution patterning and deposition of diverse materials by nanoimprint techniques can be harnessed by integrating them with the fast printing and coating tools for advancement of a R2R manufacturing system. Similarly, the development of soft polymeric stamps can provide a route to common platform for developing an optimized transfer printing protocol with photolithography, which could finally be implemented in fast R2R manufacturing track to achieve the real goal of low cost large area flexible sensors and electronics.

2.4. Conclusion

Printed sensors and electronics have attracted greater interest as printing enables low cost fabrication. The increased number of research articles and demonstration of printed sensors and electronics in a number of applications reflects the keen interest of the researchers in their quest to fulfil the promise of large area electronics on flexible substrates through cost-effective printing technologies. In this paper, we have presented a comprehensive overview of various technologies that have been employed so far for the printed devices such as TFTs, LEDs, sensors, displays, solar cells, RFID tags, printed batteries, energy harvesters and capacitors. Material solutions with adjusted rheological properties and optimum processing parameters are the major paradigms for current research on printed electronics. Most of the existing printing technologies use solution based organic materials, which often result in transistors with modest performance, which is suitable for low end applications such as RFID and displays. The performance of printed devices is also affected by the resolution limits of current printing technologies, which is much poorer than possible with current micro/nanofabrication. Fast communication and computations in emerging areas such as internet of things (IoT) will require cost-effective electronics with high-performance.

Recent progresses with printing of high-mobility materials holds a great promise for the high-performance printed electronic systems. Advances in dry transfer printing of inorganic materials could complement the organic materials based solutions. A possible approach is to employ stamp printing techniques for high-mobility semiconductor material (both solution and solid state) deposition and exploiting conventional printing technique for interconnects and metallization. However, due to resolution limits of current printing tools the full potential of printing has not been realized. Printing of high-mobility materials with resolutions comparable with the current micro/nanofabrication tools will be a significant step towards cost-effective high-performance electronic systems. The hetero-integration, involving devices based on both organic and inorganic materials, is another interesting area that could lead to stable electronic systems with good mechanical and electrical properties. Following the trends of paper printing industry, the manufacturing cost of plastic electronics is expected to reduce [106, 129, 130] by the fast speed printing of electronic components at defined locations [27]. The cost-effectiveness of printing technologies and employing them for

flexible electronics will enable new classes of applications, and dramatically change the electronics industry landscape. Printed electronics and sensing will also have a major societal and economic impact with skilled labour from print industry gradually developing printed electronics.

The printed devices and circuits demonstrated in labs often use standalone printing technologies. For large-scale production, there is a need to scale or merge these printing technologies on R2R production lines without sacrificing the chemical, physical or electrical characteristics of the device. The large area electronics through R2R production lines is foreseen to play a major role in the cost-effective manufacturing of nonconventional electronic devices and systems. Various mechanisms and challenges summarized in Table 2.3 and 2.4 for each of the printing technology highlight the possible alternatives for developing a universal printing platform where limitations of one can be overcome by another while maintaining the optimum process parameters and solution properties. Development of an efficient platform by assembling different coating, printing and patterning tools to develop a very robust process protocol will result in high throughput and low cost devices. This thesis therefore, brings together development of process protocols by combining the three potential printing technologies for fabrication of flexible devices.

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Chapter 3
Screen Printing of Sensor Materials

Part of this chapter has been published in:

Saleem Khan, Leandro Lorenzelli and Ravinder Dahiya, "**Flexible Pressure Sensors based on Screen Printed P(VDF-TrFE) and P(VDF-TrFE)/MWCNTs**" *IEEE Sensors J. vol. 15, no. 6, 3146-3155. 2015.*

Saleem Khan, Wenting Dang, Leandro Lorenzelli, and Ravinder Dahiya. "**Flexible Pressure Sensors Based on Screen-Printed P (VDF-TrFE) and P (VDF-TrFE)/MWCNTs**" *IEEE Transactions Semiconductor Manufacturing, 28, no. 4 (2015): 486-493.*

The first part of the thesis presents the advancement towards the rapid manufacturing of pressure/tactile sensors on polymeric substrates using solution based organic transducer materials. This chapter covers the development of sensors separately on large area, which highlights and compares two different types of screen printed flexible and conformable pressure sensors arrays. In both variants, the flexible pressure sensors are in the form of segmental arrays of parallel plate structure - sandwiching the piezoelectric polymer Polyvinylidene Fluoride Trifluoroethylene (P(VDF-TrFE)) between two printed metal layers of silver (Ag) in one case and the piezoresistive (Multiwall Carbon Nanotube (MWCNT) mixed with Poly(dimethylsiloxane (PDMS)) layer in the other. Each sensor module consists of 4×4 sensors array with 1×1 mm^2 sensitive area of each sensor. The screen-printed piezoelectric sensors array exploit the change in polarization level of P(VDF-TrFE) to detect dynamic tactile parameter such as contact force. Similarly, the piezoresistive sensors array exploits the change in resistance of the bulk printed layer of MWCNT/PDMS composite. The two variants are compared on the basis of fabrication by printing on plastic substrate, ease of processing and handling of the materials, compatibility of the dissimilar materials in multilayers structure, adhesion and finally based on the response to the normal compressive forces. The foldable pressure sensors arrays are completely realized using screen-printing technology and are targeted towards realizing low-cost electronic skin.

3.1. Motivation for Large Area Sensors

Printed electronics and sensors over large areas and diverse substrates is growing rapidly due to attractive features such as low-cost processing and possibility of depositing diverse materials over nonplanar surfaces. The rapid growth of the field is in line with the electronics roadmap, which indicates the merge of the well-established microelectronics technology with the age-old printing tools to realize electronic systems with simplified processing steps, reduced materials wastage, high throughput, low fabrication cost and single patterned deposition processes [1, 2].

Amongst various active and passive flexible electronic devices developed so far, the research on electronic or tactile skin for robotics has gained significant interest due to the future needs in applications such as prosthetic devices, safe human-robot interaction

and multitasks for handling delicate structures [3]. As robot technology advances, the significance of tactile sensors increases as it enables robots to conduct practical tasks such as grasping and handling delicate objects [3-7]. Tactile sensors over large areas such as entire body of a humanoid robot or of an industrial manipulator will open new research area in robotic whereby whole body contacts could be exploited to carry out such as lifting a large box or lifting an elderly – as humans do. The ultra-flexible and lightweight electronic or tactile skin with capability to measure the contact parameters such as pressure, temperature and proximity or soft touch is the key enabler for above tasks and applications.

Typical manipulation tasks such as grasping, picking and placing an object from one place to another are divided amongst various action phases [8]. To successfully carry out such manipulation tasks humans require dynamic tactile feedback (e.g. from fast adapting receptors in the skin) at transition of action phases and static or quasi-static tactile feedback (e.g. from slow adapting receptors in the skin) during the course of an action phase. The implication of these studies in humans on robotics is that the tactile skin should comprise of sensors or transducers capable of detecting both the static and dynamic contact events [4]. This is also the motivation behind investigating both the piezoelectric and piezoresistive sensors in this work. Whereas the former detects the dynamic events, the latter is capable of measuring static or quasi-static contacts. Considering human touch sensing as reference, the tactile sensors should be able to detect dynamic contact forces up to 1 kHz.

On practical side, the cost-effectiveness of electronic or tactile skin, especially of the large area skin, plays a major role in its effective use in robotics. For this reason, the printing technologies are attractive and an all screen-printing technique is the possible alternative available [9-13]. The possibility of fast production of sensors over large areas makes screen-printing attractive for manufacturing. Screen printing method has been used in this work to develop the piezoelectric and piezoresistive tactile sensors. In particular, the focus of investigations in this chapter is on the manufacturing processes, number of steps involved in the final module development, ease of handling of materials, compatibility of dissimilar materials in multilayer structures, adhesion to polymer substrate, overall assembly of the sensor modules and finally on the basis of sensor response to normal compressive forces.

3.2. State of the Art

3.2.1. Piezoelectric and Piezoresistive Tactile Sensors

Over the years, wide varieties of tactile sensing structures have been demonstrated using various transduction methods such as capacitive, ultrasonic, piezoresistive, and piezoelectric etc. [14-16]. Piezoelectric materials are unique as they allow measuring dynamic events such as slippage and have wider applicability in sensors, actuators and energy harvesters [17-20]. Amongst various piezoelectric materials, the Polyvinylidene fluoride (PVDF) and its copolymer Trifluoroethylene (TrFE) have been widely

investigated due to their mechanical flexibility and stable piezo, pyro and ferroelectric properties. Attractive features of P(VDF-TrFE) are the high sensitivity, wide frequency response, flexibility, cost effectiveness, and ease of fabrication [5, 16, 20, 21].

Piezoresistance is another interesting phenomenon that has been exploited to develop pressure sensors (e.g. for grip) for measuring static contact events. Their advantages include simple low-cost electronics [4, 22, 23]. Several materials and mechanisms explored to exploit piezoresistance for sensor include change in resistance of metallic strain gauges or change in mobility of solid-state semiconductor devices [24-26]. Often these materials and structures have low gauges factors and to overcome this obstacle, the conductive polymer composites have been explored by researchers to develop piezoresistive devices. MWCNT in PDMS (polydimethylsiloxane) matrix results in a material, which possesses a number of exciting properties that can successfully be harnessed in sensors and actuators [27-33].

3.2.2. Printing of sensors

For deployment of sensor arrays on large surfaces, it is necessary to micro-pattern the transducer material in an efficient and cost-effective way. Different fabrication technologies have been reported to realize P(VDF-TrFE) and MWCNT/PDMS based sensors. Spin coating, thermally drawn functional fibers, micro-machined mold transfer, single and multilayer inkjet printers have been employed for deposition of these solutions for sensors [6, 20, 21, 29, 30, 34-38]. The frequently used techniques such as spin coater and inkjet for patterning large areas devices have limitations of process speed and overlay registration accuracy in multi-layered structures. Although, inkjet printing has high lateral resolution, patterning of large areas (> 2 mm^2) require repeated deposition of droplets, which often results in a nonuniform layer thickness and edges. In addition, patterning of P(VDF-TrFE) after spin coating whole layer on wafer requires photolithography, which leads to more complexity of the manufacturing process [20]. The cost-effectiveness and faster fabrication of sensors over large areas make screen-printing very attractive and therefore [11, 12], an all screen-printed structure is the main focus of our current study. Using the similar technology for all the layers will help in minimizing process time and improve manufacturability. Besides this, the use of printing technologies will lead to reduce material waste and high-speed manufacturing.

3.3. Materials Synthesis and Scheme of the Sensors

3.3.1. PVDF-TrFE Solution Preparation

The materials used for developing piezoelectric modules consist of P(VDF-TrFE) as the transducer medium. PVDF is a well-known polymer used in piezoelectric based sensors due to excellent features especially for dynamic responses of compressive forces as shown in Figure 3.1 (a & b), which can be successfully harnessed for tactile sensing in robotic skin for slip detection and control. Usually mechanical stretching is required to induce piezoelectric properties into PVDF, which is incompatible with microfabrication process. On the other hand, P(VDF-TrFE) has the tendency to

crystallize directly in the polar β-phase without any requirements of mechanical stretching [4, 39]. Molecular proportion x (0.6 < x < 0.85) of the vinyledene fluoride in P(VDF-TrFE) define the crystal structure and optimal piezoelectricity of the polymers [5, 20]. Compositions around 70/30 %wt. exhibit good ferroelectric response.

P(VDF-TrFE) have good solubility in Dimethylformamide (DMF) and Methyl Ethyl Ketone (MEK), which are most appropriate for screen-printing. Solutions with different weight ratios of P(VDF-TrFE) and MEK were investigated for optimum parameters of dispensing through stencil mask of a screen-printing. Pallets of 70/30 wt. %. P(VDF-TrFE) were dissolved in Methyl Ethyl Ketone (MEK) at 15% weight to get the solution compatible with screen-printing experiments [11]. After mechanical stirring, the mixture was kept at 90 °C for 6 hours and stirred continuously. This resulted in P(VDF-TrFE) pallets were completely dissolved in MEK and solution was used with screen-printing without any further treatments.

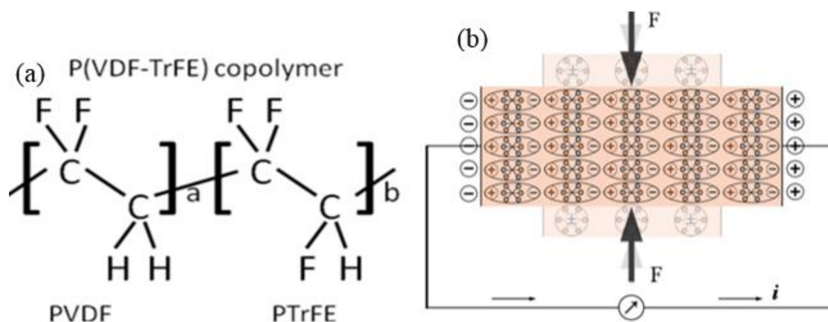


Figure 3.1. (a) Bonding structure of PVDF and TrFE (b). Working of a piezoelectric sensor. The charge is generated s when piezoelectric material is subjected to external compressive force [4].

3.3.2. Percolation and Nanocomposite Preparation

Addition of highly conductive nanofillers in a dielectric material results in a conductive or semi-conductive polymer. Percolation describes the mechanism of incorporation of highly conductive nanofillers in an insulating polymer, which results in alteration of its mechanical and electrical behaviour. Percolation mechanism is based on the orientation of the nanofillers to form conductive channels through either physical contact or tunnelling when dispersed in polymer matrix. Figure 3.2 (a & b) show schematics of percolation mechanism where different concentrations of nanofillers are shown. The actuation in these nanocomposites layers is governed by the distribution, geometry and interconnection paths of nanotubes in the polymer matrix, which vary upon application of force. This leads to a change in bulk resistance of the composite layer. Percolation threshold is the critical concentration of conductive fillers at which the sufficient continuous conductive network is established and dielectric base polymer

becomes conductive as shown in Figure 3.2 (a). A low percolation threshold is desired to retain the static as well as dynamic mechanical, physical and electrical properties of nanocomposites. The shape and size of the nanofillers affect both electrical and mechanical properties of the nanocomposites. The aspect ratio of the nanofillers is the critical parameter influencing the percolation threshold. Uniform dispersion of nanofillers is of prime importance and contributes mainly to the performance of sensors and devices. Compared to metallic nanoparticles fillers, multiwall carbon nanotubes are extensively investigated in recent years. Due to the high aspect ratio of MWNTs, low percolation threshold is achieved, which helps in retaining the soft behaviour of elastomeric structures [27-33].

Development of piezoresistive sensors array consisted of multiwall carbon nanotube (MWCNT) mixed with Poly(dimethyl-siloxane) (PDMS) matrix. Incorporating the MWCNTs in PDMS results in a material with a number of exciting properties for sensors and actuators especially for grip purposes in tactile sensors of robotic skin. The actuation mechanism is based on the geometry and interconnection paths of nanotubes developed in the polymer matrix, which vary upon application of force. This leads to a change in resistance of the bulk composite layer [28, 29, 38]. These nanocomposite materials have similar characteristics to some inorganic semiconductors while maintaining typical polymer properties of flexibility, easy processing and synthesis. A low percolation threshold is desired to retain the static as well as dynamic mechanical, physical and electrical properties of MWCNT/PDMS nanocomposites. Uniform dispersion of nanofillers is of prime importance and contributes mainly to performance of the sensors [31].

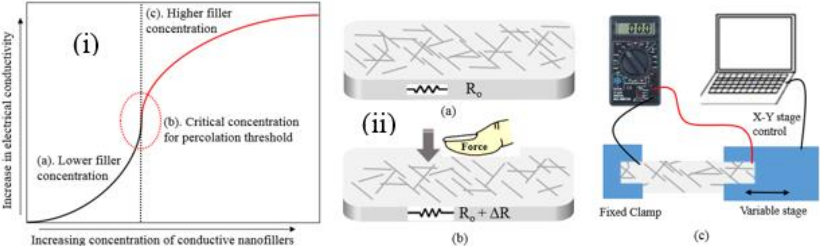


Figure 3.2. (i) Electrical conductivity of conductive composites as a function of filler fraction, where "a, b, c, d" denote the typical network of conductive fillers within the polymeric matrix. (ii) Schematic of the actuation mechanism of nanocomposite-based sensors (a) Sensor without pressure applied, (b). Normal compressive force (c) System setup for resistance measurement.

Although these polymer nanocomposites have the challenges of non-linearity, hysteresis and temperature drifts, they are effective for large strains, simple and cost-effective to fabricate. These advantages make them a better choice of sensing elements for applications requiring complaint materials such as electronic skin, electronic textiles and other large deformation measurements. For this reason, the work presented here employs MWCNTs in PDMS matrix for piezoresistive sensor arrays. MWCNTs purchased from Sigma Aldrich have > 95 % carbon, with nanotubes having outer diameters of 6-9 nm, length 5μm and ~2.5g/mL density at room temperature. In order to check the screen printability of the MWCNT/PDMS composite solution, four different solution samples, having 1%, 3% 5% and 6% as weight ratios, were prepared. To enhance the dispersion of nanofillers, MWCNTs were first mixed in chloroform by using mechanical stirrer and kept in ultrasonic bath at frequency 40 kHz for 30 minutes. Sequence of the synthesis steps for nanocomposite processing is shown in Figure 3.3 (a-e). After uniform dispersion of nanotubes in the chloroform, PDMS (Dow Corning Sylgard 184) was mixed with the solution followed by mechanical stirring for 10 minutes. Composite solution was kept again in ultrasonic bath at 40 kHz for 3 hours. Cross-linking agent was added in 10:1 into the composite and degassed completely in a vacuum desiccator. Similar steps were followed for developing all the three solution samples [12]. After degassing steps, nanocomposites were immediately screen printed on pre-printed electrodes.

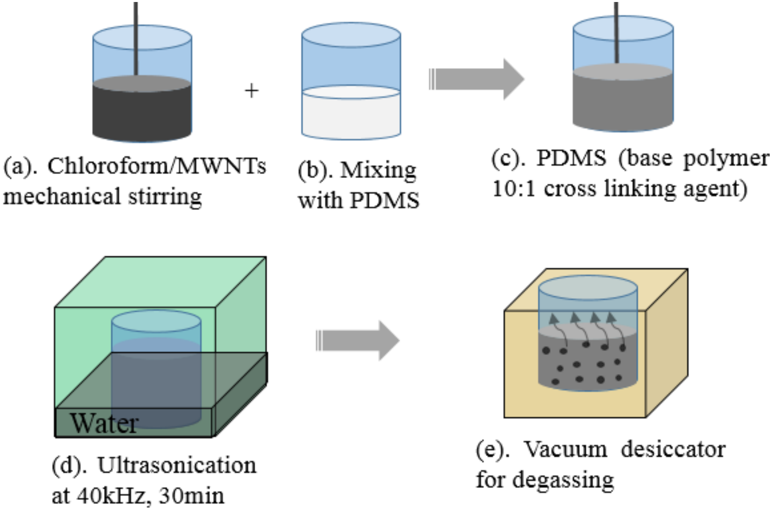


Figure 3.3. Synthesis and manufacturing procedure of the PDMS/CNT nanocomposites by adding a dispersant solution before casting the final solution for patterning.

3.3.3. Schematic of the Sensor Module

The scheme of each of the four sensor modules developed by using above synthesized materials is shown in Figure 3.4. Stencil mask has been developed in such a way that four modules (each with 4x4 tactile sensors) can be printed on a single substrate in one go. A parallel plate structure is developed in which the transducer material is sandwiched between metallic layers. For metallic plates and interconnect lines as well, silver (Ag) based paste (purchased from DuPont (5028)) is used. Rheological properties of the Ag paste are already adjusted to be used with screen printing tools. UV-curable dielectric (DuPont-5018) paste is used as received from supplier for the force concentrator structures. Details of the screen printing steps are discussed in the following sections.

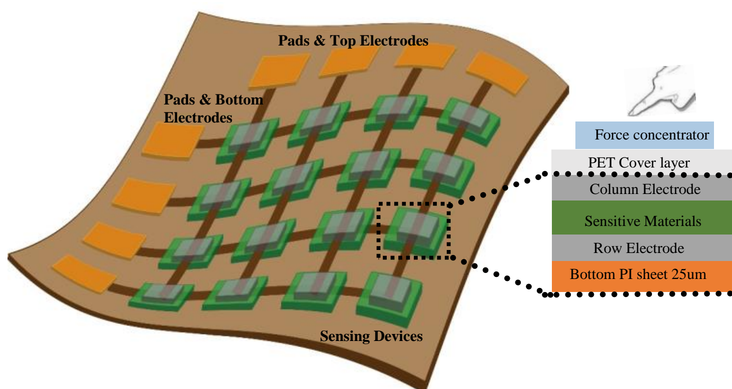


Figure 3.4. Schematic diagram of a single module of sensors array and cross sectional view of the proposed printed layers.

3.4. *Screen Printing Experiments*

3.4.1. Screen Printing of Metallic Patterns and P(VDF-TrFE)

Different fabrication technologies have been reported to realize P(VDF-TrFE) based sensors. Spin coating, thermally drawn functional fibers, micro-machined mold transfer, single and multiplayer inkjet printers have been employed for developing P(VDF-TrFE) based sensors [6, 20, 21, 34-37]. The frequently used techniques such as spin coater and inkjet for patterning PVDF have limitations of process speed and overlay registration accuracy in multilayer structures. In addition, patterning of PVDF after spin coating whole layer on wafer requires photolithography, which leads to more complexity of the manufacturing process. Screen-printing is considered preferable alternative technology for patterning. For realizing the parallel plate capacitive structures the silver (Ag), based paste is used for top and bottom electrodes. Paste viscosity is in the range of 15-30 Pa.s. Conductive tracks for bottom electrodes are divided into 4 modules, each containing

4×4 array of transducer components (Figure 3.5). Capacitive area is 1×1mm^2, which are connected through printed interconnected lines of 100 µm wide. Distance between consecutive sensors is 5.6 mm in order to reduce crosstalk between neighbouring sensors. The pads for readout signals, 2×2 mm^2 area, are coupled with printing bottom electrodes. After completing the first step of Ag printing, samples are sintered at 120 °C for 1 hour. A separate stencil mask with 3×3 mm^2 opening area, overlapping on each side of the bottom electrode is used for printing piezoelectric material i.e. P(VDF-TrFE) on bottom electrode. Both stencil masks are designed in such a way that the overlay registration accuracy can closely be maintained. Screen-printing parameters i.e. squeegee height, pressure on the stencil, squeegee speed, snap-off and offset for the screen stage are critical to monitor. Height for first forward squeegee is kept at 46.15mm while the following squeegee is kept at 42.90 mm from the stencil mask. Pressure and speeds for both the squeegees are kept at 0.5 kg and 10 mm/sec respectively. Screen height from stage is kept at 5 mm while keeping the snap off at 1 mm. Deposited layers are sintered in vacuum at 130 °C for 4 hours to remove the solvents and enhance recrystallization of P(VDF-TrFE). The top electrodes are patterned on separate PET substrate by using the first stencil mask but with 90° degree orientation to obtain sensors in the row-column fashion. The scheme of the stencil masks used for printing various sensor structures i.e. metallic patterns, transducer and dielectric for top force concentrator are shown in Figure 3.5(a).

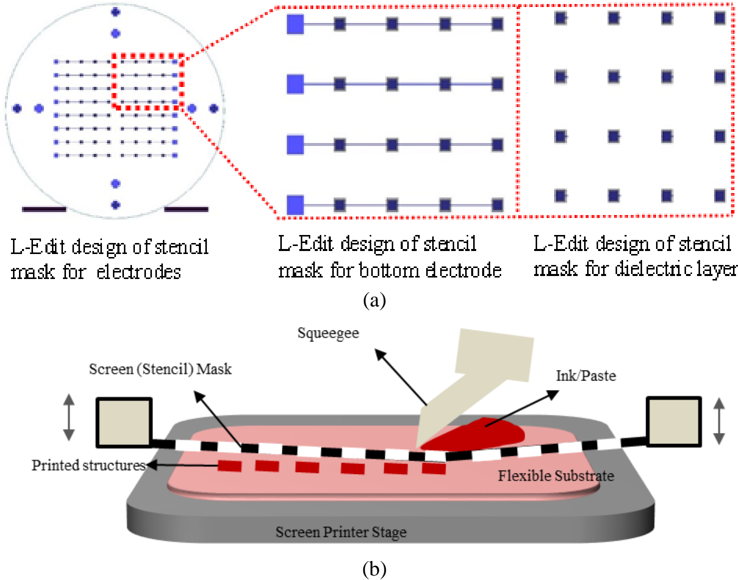


Figure 3.5. (a) L-Edit design of stencil masks for metallic, transducer and force concentrator structures (b) Schematic of flatbed screen-printing system setup

Screen-printing (schematics shown in Figure 3.5 (b)) is more robust and it is easy to control the layer thickness by varying process parameters like pressure and speed of the printing squeegee if solution properties have reached its optimal requirements. The small fraction of solution printed only at the opening of the stencil plays an important role in reducing material cost by minimizing wastage, and reusability of the solution makes the printing system very robust for subsequent uses. However, the residual solution collected by the second squeegee is not completely the same as before and some part of the material is wasted in this process as well. This problem is mainly due to the selection of solvent specifically in case of P(VDF-TrFE) when dissolved in MEK. This problem is foreseen to overcome by investigating an appropriate solvent that is also compatible with screen-printing. Uniformity of the layer is maintained in screen-printing and the solution is deposited at desired areas of interest, i.e. on top of bottom metal layers with 100% overlay registration.

3.4.2. Screen Printing of MWCNT/PDMS

The similar structure of parallel plates and experimental setup is followed to realize the piezoresistive sensors array. The MWCNT/PDMS nanocomposites layer is sandwiched between the two printed silver metal electrodes as discussed in previous section. Attractive feature of this approach is that the processing steps are performed by using a single printing technology i.e. screen-printing. Solutions of MWCNT/PDMS composites were printed on bottom electrode aligned by adjusting screen printing stage parameters. In case of MWCNT/PDMS the three solutions, with 1, 3 and 5% wt. prepared as reported in Sec. 3.3.2, were used for analysis of optimal dispensing out of the solution. Different printing speeds are applied because of different concentration of the three solutions. Speed of the forward squeegee was kept higher i.e. 15 mm/sec in case of 1% solution and was decreased to 10 mm/sec and 6 mm/sec for 3% and 5% respectively. The experimental parameters such as squeegee pressure snap-off from stage and speed are summarized in Table 3.1. High speed of the squeegee is observed to overcome the problem of bleed out of lower concentration solutions from the stencil mask, which also helps in keeping the desired patterns on the substrate after printing. This is the reason to keep the amount of dispensed material as minimum as possible. While at higher concentrations, speed is reduced to increase the dispense time at the stencil openings. These parameters were adjusted after doing a number of experiments with the prepared nanocomposite solutions.

Table 3.1. Screen Printing Parameters

Material		Pressure(kg)	Snap-off (mm)	Speed (mm/sec)
PVDF-TrFE		0.5	1	10
MWCNT/PDMS	1%	0.45	1.2	15
	3%	0.5	1	10
	5%	0.5	1	6

A hard mask is prepared for the deposition of the nanocomposite solutions. Figure 3.6 (a) show images of 3D printer and masks prepared by using it whereas Figure 3.6 (b) depicts an image of the manual screen-printing for higher concentration solutions. Shadow masks are made of plastic sheets, which are layered by gluing separate sheets of plastic to each other containing the desired structures. This is a full-automated way of producing these masks using a 3D printer (SD300). Such type of masks are more useful for composite solutions with high concentrations (i.e. > 5 wt. %), where uniformity of layers are needed to be maintained after printing. In contrast to these masks, standard meshed screens dedicated for screen printers alter the uniformity of the final deposited solution on substrate. This is due to the residual and agglomeration of the nanotubes on the screen meshes.

Deposited layers were sintered in vacuum at 80 ^{o}C for 5 hours and kept overnight. After complete polymerization, counter electrode was printed on top of composite material using the same stencil but with 90° orientation. Top and bottom electrodes are in good alignment and no short-circuiting was detected after checking all the devices.

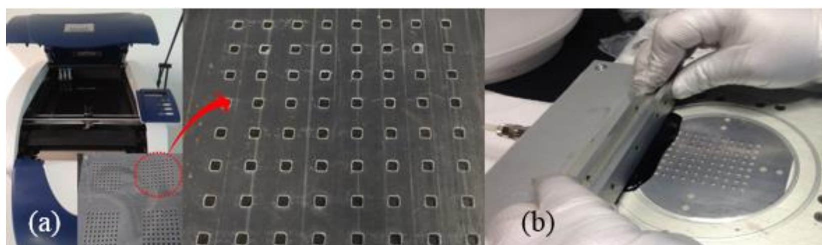


Figure 3.6. (a). 3D-Printer with the final developed shadow mask for deposition of nanocomposite solutions. (b). Manual screen-printing by using squeegee to print nanocomposite solutions on top of pre-printed silver tracks

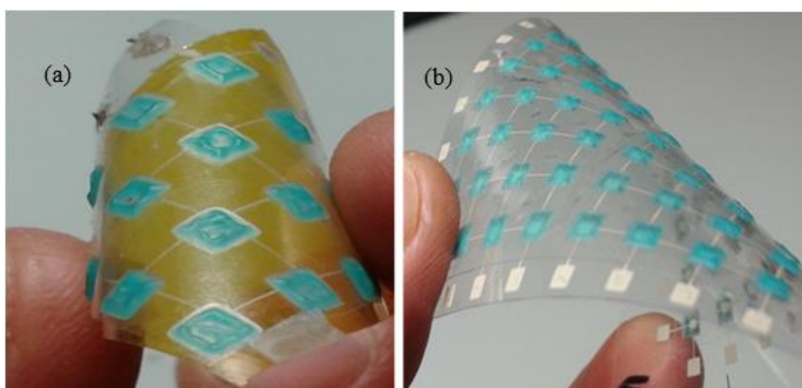


Figure 3.7. Final assembled screen-printed sensor cells with force concentrated structures (a) Sensors based on P(VDF-TrFE) on polyimide (PI) substrate (b) Screen printed MWCNT/PDMS sensors on PET substrate

Force concentrator structures (3×3 mm^2) were printed on a separate substrate and laminated on the bottom substrate, which also served as an encapsulant from any environmental affects to the sensors. Force concentrators were printed using UV-curable dielectric ink supplied by DuPont. Figure 3.7 (a&b) shows the final assembled array of sensor devices with force concentrator structures based on printing MWCNT/PDMS composites.

3.5. Results and Discussion

Screen-printed conductive patterns and sensitive materials were characterized to investigate different physical and electrical parameters required for reliable printed flexible sensor modules. In case of conductive patterns, the thickness of printed layers is of prime importance for enhanced electrical conductivity. Screen-printing deposits thick layers in a single deposition step as compared to other patterning tools by maintaining the overlay registration accuracy and uniform pattern edges, which is suitable for the proposed printed capacitive structures. Profilometer for thickness measurement, adhesion to the polymer substrate under different humidity and temperature conditions, print efficiency and sheet resistance are some of the prime characteristics of printed patterns. Adhesion of the subsequent printed materials on the sintered Ag patterns was checked in planar as well as in bent orientation of the substrate at 15 mm radius. Finally, sensors are characterized by applying normal compressive forces at different frequencies. Results based on physical characteristics and responses with both materials are investigated and discussed in the following sub-sections.

3.5.1. Sheet Resistance of the conductive patterns

Sheet resistance of the conductive patterns has been measured in planar and bent mode to check any change in conductivity. Four-point collinear probe setup was developed by using high impedance Keithley 7410 voltmeter for current and voltage analysis (equipment and results shown in Figure 3.8). Resistance is measured in one complete row of printed electrodes having four plates connected inline. In the collinear configuration, the outer two probes placed at the centres of printed plates were used to source the current while the inner two probes placed on the central two plates were used to determine the voltage drop across the whole line. The sheet resistance value given by the supplier for the printed silver paste is about 12Ω/sq. for the layer with thickness about 25µm. The sheet resistance measured in our samples (layer thickness of about 8µm) is 14.15 Ω/sq. in the planar mode, which is in the close range of expected sheet resistance of silver paste after sintering. The sheet resistances of the same printed lines were checked at bent orientation of the substrate. In bent orientation with radius of 15mm round, the sheet resistance was observed to be little higher i.e. about 17.54 Ω/sq. This could be due to the variation in layer thickness and possible microcracks during the

bend mode conditions. Nonetheless, the resistances in both the planar and bend orientations are acceptable for our application in the pressure sensors.

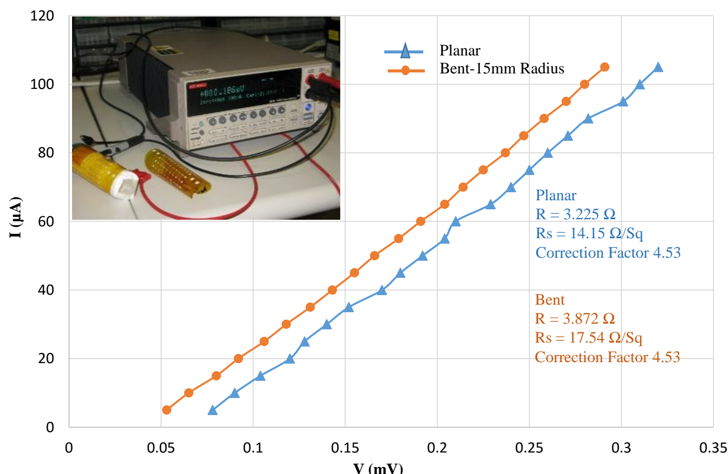


Figure 3.8. Sheet resistance of screen-printed Silver (Ag) patterns in planar and bent orientation (radius 15 mm) on PI substrate.

3.5.2. Microscopic and mechanical profilometer analysis

Mechanical profilometer and scanning electron microscope (SEM) were used to analyze the thickness of conductive patterns as well as the deposited P(VDF-TrFE) and MWCNT/PDMS layers. Samples were analyzed after complete sintering in a vacuum environment. Figure 3.9 shows SEM image of P(VDF-TrFE) layer deposited on top electrode respectively. The porous structure observed in P(VDF-TrFE) layer indicates complete evaporation of solvent leaving behind pinholes. The printed layer of P(VDF-TrFE) in which the pinholes left after evaporation of the solution are evident from Figure 3.9. The Ag paste printed for top electrodes pass through these pinholes of the P(VDF-TrFE) layer, which eventually results in short circuiting of the two printed metal plates. This was confirmed by a trial experiment by printing Ag paste on top of P(VDF-TrFE), which resulted in short circuiting after sintering. This is one of the reasons for printing top electrode on a separate PET substrate instead directly on P(VDF-TrFE) due to the penetration of Ag paste through these pinholes.

Mechanical profilometer is used to check the thickness of all layers i.e. conductive patterns, P(VDF-TrEF) and MWCNT/PDMS layers. Metallic patterns observed at different positions of the substrate were found to have thickness about 8 μm. Screen printed P(VDF-TrFE) was found to have thickness about 3 μm less than the MWCNT/PDMS samples which were around 10-15 μm thick. Minimum thickness was obtained with the 1% solution, while layer with 5% solution is about 15 μm, which is due to the increased concentration of MWCNTs. Figure 3.10 shows the optical micrographs of the printed MWCNT layers in which agglomeration of MWCNT in the PDMS matrix occurs at random locations. Agglomeration of MWCNTs are more evident in solutions with increased concentrations of the filler materials that ultimately affects the reliability of the sensor response and consistency.

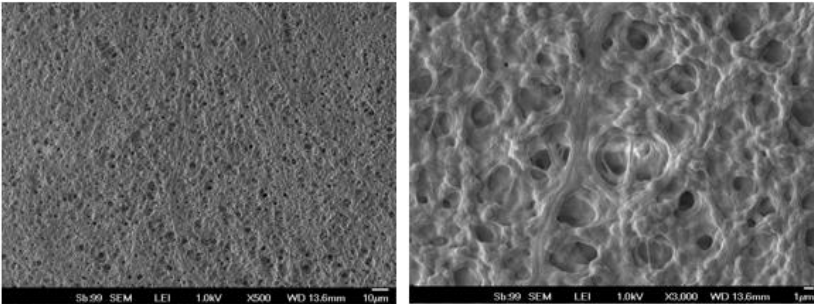


Figure 3.9. Scanning Electron Microscope images showing optical micrographs of porous structure of screen-printed P(VDF-TrFE) on top of Ag patterns.

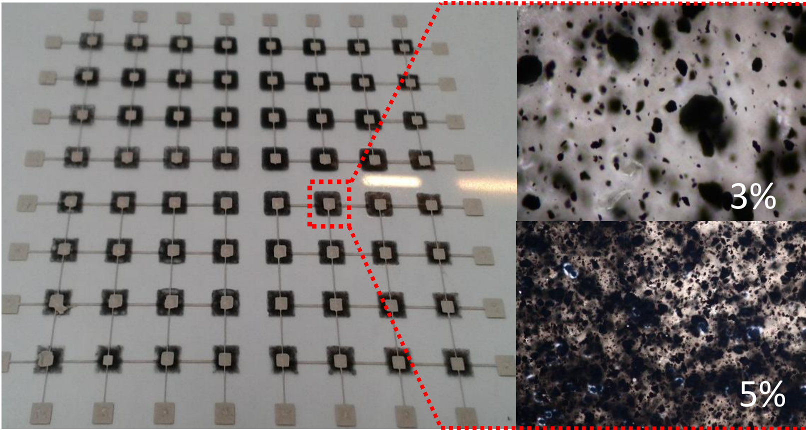


Figure 3.10. Optical micrographs of screen-printed Ag (for metal and interconnect lines) and sandwiched MWCNT/PDMS. Optical microscopic images of 3 and 5% wt. shows the MWCNTs distribution in the PDMS matrix.

3.5.3. Adhesion loss test of printed layers

It is important to determine the adhesion of printed features on polymeric substrate under different environmental conditions, especially the temperature and humidity as they have direct bearing on the reliability of sensors. Adhesion of screen-printed P(VDF-TrFE), MWCNT/PDMS, silver patterns and dielectric ink (for force concentrator structures) were checked under different temperature and humidity conditions. Tape test was performed for checking adhesion loss or complete delamination of the printed layers from flexible substrate. Adhesion of these layers was investigated under two orientation schemes, first with samples on a planar surface and second, with substrates wrapped around a cylinder of 15 mm radius. Three different temperature and humidity conditions were developed for both the schemes. In first set of experiments, samples were tested at room temperature and humidity of 16g/cm^3. In the second set of experiments, samples were placed in a humidity chamber with absolute humidity at 40 g/cm^3 and temperature at 40°C. The samples were kept in humidity chamber for 15 minutes and then taken out for adhesion test immediately. In the third setup, the humidity level was raised to 80 g/cm^3 and temperature to 80 ^{o}C. Adhesion tape was applied on the samples immediately after withdrawal from the chamber for second and third set of experiments. At room temperature and 16 g/cm3 of humidity, no delamination of interconnect wires or force concentrator structures were observed. Only two interconnect lines at the centres (12 % of the total interconnects length) were peeled off at 40 ^{o}C and absolute humidity of 40 g/cm^3. For 80 ^{o}C and 80g/cm^3 of the temperature and humidity, three interconnect lines of (18 % of the total interconnects) were observed to be delaminated.

Similar results of delamination of interconnect lines were observed in bent orientation at 15 mm of radius, at the same conditions of humidity and temperature. Force concentrator structures were observed to have very good adhesion to the substrate and all the structures remained fixed. Adhesion loss test for printed structures of P(VDF-TrFE) was also performed according to the developed conditions mentioned above. Upon testing at room temperature, there is no peel-off of any structure from the substrate. However, at higher values of humidity and temperature in second and third set of experiments, all the layers of screen-printed P(VDF-TrFE) were peeled off. The same results were experienced for bent samples as well. The porous structures of P(VDF-TrFE) layer is playing critical role in absorbing the humidity, which ultimately weakens the materials/substrate interface strength and deteriorates all the structures developed on top of it. The poor adhesion of P(VDF-TrFE) with polymer substrate at increased temperature and humidity values make it less attractive on an electronic skin, which is required to read stimulus accurately at varied working environment. Possible solution to the humidity problem is to use an encapsulation layer. The PET substrate used for top electrodes and force concentrator structures is selected to serve this purpose in our proposed scheme.

Plasma oxidation of polymer substrate was performed before printing bottom electrodes for modification of the surface to promote the adhesion of transducer materials with substrate. The plasma oxidation makes the polymer surface hydrophilic and improves the adhesion. As the total coverage area of the transducer material (3×3 mm^2) is greater than bottom electrode (1×1 mm^2), materials make strong bond around the electrodes after sintering. Polymer nanocomposites i.e. MWCNT/PDMS are soft material owing to the intrinsic properties of base polymer matrix. When microstructures of these composites are printed onto the plasma-oxidized substrate, the interface is tightly secured by strong bonding. Tape test was performed for checking adhesion loss of Ag tracks printed on top of MWCNT/PDMS nanocomposite. Adhesion of Ag is also found to be dependent on filler concentration. For 1% MWCNT/PDMS, about 70% of the Ag tracks were delaminated by peeling-off the adhesive tape. Adhesion became stronger for MWCNT/PDMS samples with higher concentrations, (i.e. with 3% and 5%

Table. 3.2. Adhesion loss test for the printed structures

Printed Layer	Temp, °C	Absolute humidity, g/cm^3	Observation delamination
Interconnect Lines	25	16	Negative
	40	40	Two lines (12% of the total length) delaminated.
	80	80	Three Lines (18% of the total length) delaminated.
Dielectric (Force Concentrators)	25	16	Negative
	40	40	Negative
	80	80	Negative
P(VDF-TrFE)	25	16	Negative
	40	40	Complete delamination
	80	80	Complete delamination
MWCNT/PDMS	25	16	Negative
	40	40	Negative
	80	80	Negative

filler concentrations), as about 50% and 10% of the Ag layers were delaminated respectively. This might be due to strong interaction of Ag paste on molecular level with MWCNTs in the PDMS matrix. Alternate to P(VDF-TrFE), MWCNT/PDMS showed very good adhesive properties at all the developed conditions of temperature and humidity. Surface properties of substrates for both the materials were modified by exposing it to plasma oxidation before doing printing experiments due to which

adhesion of MWCNT/PDMS improved further, while no improvement in P(VDF-TrFE) was observed. Table. 3.2 summarises all the adhesion loss test for the printed structures.

3.5.4. Capacitance-Voltage (C-V) and Piezoelectric response of P(VDF-TrFE)

Polarization or poling of P(VDF-TrFE) is required to introduce the piezoelectric behaviour. P(VDF-TrFE) is normally polarized by applying high voltage across the film. The strength of this voltage is typically 80 V/μm for P(VDF-TrFE) films [20]. This is one extra (and major) step towards achieving precise piezoelectric response. Higher voltage and increased charge induction to thin layers at raised temperatures often results in sparking and eventually destroy the structures. On the other hand, no modification or changes into the printed layers of MWCNT/PDMS are needed. The transduction paths developed by MWCNTs in PDMS bulk remain fixed after polymerization, which ultimately contribute to the change in resistivity. To polarize screen-printed P(VDF-TrFE), the sensor arrays were put on a hot plate at 80 ^{o}C and voltage increased at a rate of 60 V/μm across the metal layers on the pads. For screen-printed layers of P(VDF-TrFE) with thickness of 3 μm, the maximum potential of 180V was reached in 6 incremental steps of 30V each. Electric field was applied for 10 minutes at each incremental step. Between two successive voltage application steps, the metal plates of P(VDF-TrFE) samples were short-circuited for about 5 minutes to mitigate the electric breakdown.

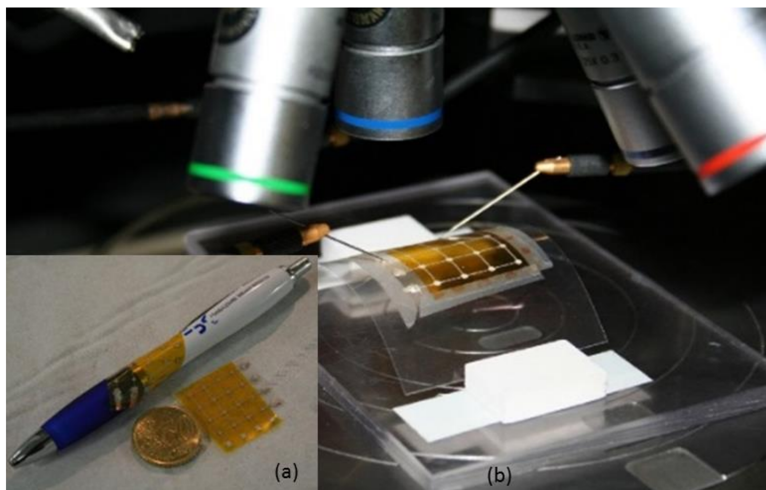


Figure 3.11. (a) Final assembled sensor modules in planar and bent orientations. (b) C-V measurement setup of sensors in bent orientation.

C-V measurements at varying frequencies were made before and after polarization. For C-V measurements, Agilent 4284A, precision LCR meter was used controlled by a program developed in LabVIEW. Figure 3.11 shows arrangement of probes with sensor module in bent mode. The frequency used for experiment was increased in 30 steps ranging between 100Hz and 1MHz and peak oscillating voltage was kept at 10mV and hold time of 1 sec. Average values of capacitance at all these frequencies before and after polarization are obtained and are 0.695 pF and 0.962 pF for unpoled and polarized

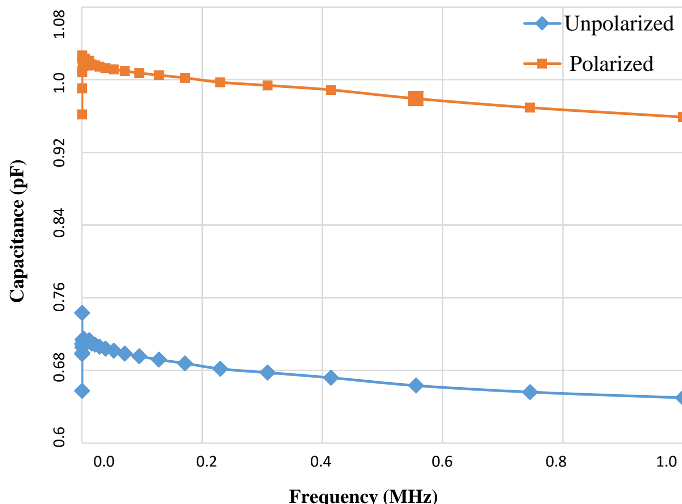
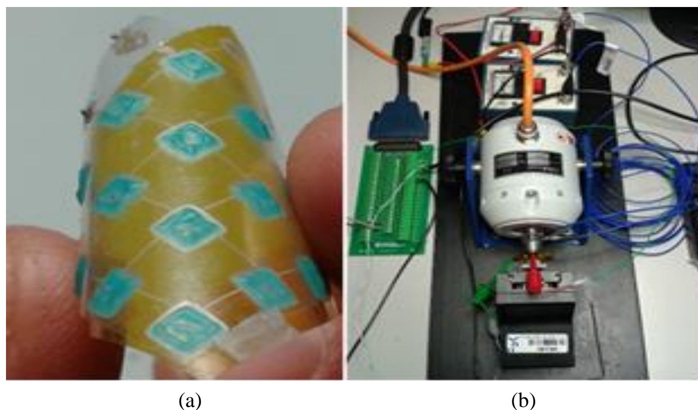


Figure 3.12. Capacitance vs. frequency measurement of unpolarized and polarized P(VDF-TrFE) with peak oscillating voltage 10mV and a hold time of 1sec.



(a) (b)

Figure 3.13. Experimental setup of measuring piezoelectric response of P(VDF-TrFE). (a) Sensor module with force concentrator structures. (b) TIRA shaker and signal conditioning setup for dynamic force measurement.

samples respectively shown in Figure 3.12. Change in capacitance value is observed in the polarized samples and an increase in capacitance of 0.267 pF is recorded. This difference is consistent among various capacitive devices both polarized and nonpolarized. This change may be due to polarized charges injected during poling. The general frequency response of the device is in the acceptable ranges as discussed in literature for applications to flexible pressure sensors.

Piezoelectric properties of the discrete devices were investigated at different frequencies and force values. Sensors were tested at 10Hz, 50Hz and 200Hz while forces varied from 0.5–3.0 N for each corresponding frequency. Equipment used for testing the sensor devices consist of TIRA shaker, signal conditioning circuits and an amplifier shown in Figure 3.13. All the major equipment for analysis and measurement of the output values is controlled by a program developed in LabVIEW. Upper limit of the dynamic force applied by shaker is 18 N with frequency ranging from 2 Hz–1 kHz. A load cell (PCB piezotronics) with sensitivity of 112.41 mV/kN and measurement range of 0.00448 kN is mounted on the shaker tip, which can move in z-direction, is used to measure and control the applied force on the sensor.

The force concentrators covering the whole effective area of the sensor is aligned according to the load cell tip in x, y and z directions. Sensors were characterized at constant frequency and increasing the applied force. At frequencies below 50 Hz, sensor response is about ~0.05V/N. For frequencies greater than 100Hz, the response of the sensor increases approximately in linear fashion. This increase in response can be observed in Figure. 3.14 at 3N, which shows an increase of almost 0.07V for 200Hz and

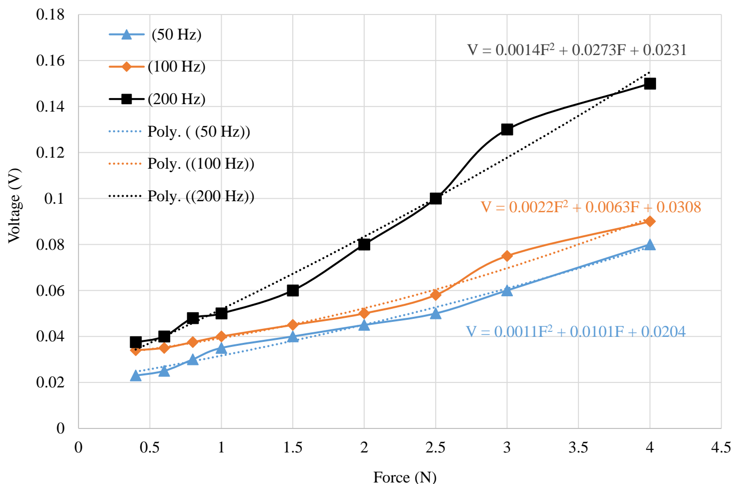


Figure 3.14. Response of P(VDF-TrFE) at varying forces and frequencies. Sensor is characterized at three different frequencies i.e. 50, 100 and 200 Hz at each force value. Response of the sensor increases with increasing frequency while trend of graph lines is polynomial of second degree.

0.02V for 100Hz at the same applied force. Response of the individual sensors at different value of frequencies and varying force is given in Figure 3.14.

3.5.5. Piezoresistance response of printed MWCNT/PDMS

The piezoresistance in MWCNT/PDMS nanocomposites is introduced by generation of distributed conductive paths within the bulk. The resistance of the sensors presented here can be tuned with filler concentration as shown Figure 3.15. This change in the initial resistance values for bulk piezoresistive composites at different filler concentration is mainly due to different number of interconnection paths and random distribution of MWCNT within the polymer matrix. Filler concentration is not only the major parameter for resistance change but is also critical for printing process. Solution becomes dense with increased amount of fillers and beyond a certain limit; it becomes difficult to screen print uniformly. Thus, an optimum range of filler concentration is required for controlled patterning and readable resistive response. At low concentrations ~1%, the initial resistance is very large restricting resistance change within close limits. In addition, the solution is less viscous and flows out after printing which deteriorates the shape of the patterned structures. The isolation of individual sensing devices is not maintained and very irregular layer of MWCNT/PDMS is achieved. Avoiding such condition requires increase in the filler concentration. This also improves both physical and electrical properties of the device. With increased concentration, operating range of the device is extended due to an increase in the offset value of initial resistance. The operating envelope (0-10N for MWCNT/PDMS in current research) of the transducer material becomes responsive to an increased range of forces. Comparing the three nanocomposite solutions, 3 % wt. is found to be the optimum concentration by analysing the piezoresistance response values in Figure 3.16 and also from screen-

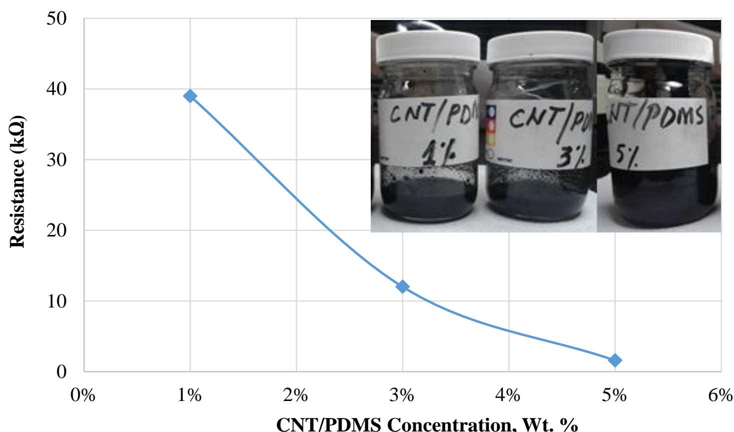


Figure. 3.15. Change is the resistance of polymerized composite samples with varying MWCNT concentration in PDMS.

printing experiments.

The response of MWCNT/PDMS composites is obtained by applying compressive forces on the sensor device. The observed change in the resistance of sensors is due to (a) micro-nanoscale changes in the carbon nanotubes as a result of mechanical deformation, and (b) the formation of conductive paths within the matrix. Prepared samples were put on a rigid surface and force was applied on top of force concentrator structures that are aligned with the sensory cells. Piezoresistive behaviour was confirmed by the observed change in resistance with respect to applied force. As shown in Figure 3.16, the resistance increases with increasing forces. The amount of change in the resistance values is observed to be higher for sample with less concentration of MWCNTs in PDMS. That could be due to immediate breakdown of the conduction paths established in the polymer matrix. The MWCNT/PDMS samples with 1% and 3% wt. concentrations show an approximate linear response (Figure 3.16) which is often desired in pressure sensors. In case of 5%, wt. an abrupt non-uniform change in resistance occurs above forces of around 6.0 N. This range is much higher than the force (0.01-1N) experienced by humans in daily tasks [14].

The sensors were also evaluated for cyclic force to check their restoration behaviour to the initial resistances. Restoration of the resistance values for 3% wt. after removing the applied stress was much faster than the samples with 1% and 5% wt. concentrations. For 3% wt., the restoration time is of the order of few seconds, while for other two concentrations it took few minutes to restore the initial value. The trend of increase in resistance values is not uniform, which might be due to non-uniform dispersion and random conductive paths made by aggregates of nanotubes within the polymer matrix.

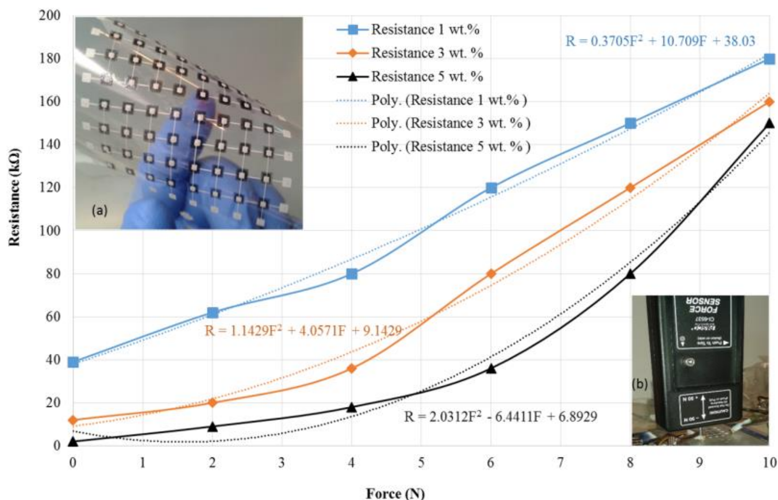


Figure 3.16. Resistance change with normal compressive force showing trend line of a polynomial of degree two, (a). Screen-printed (MWCNT/PDMS 3% wt.) modules. (b) Setup of force sensors for characterizing final assembled device with force concentrator structures.

Agglomeration of MWCNTs at various locations of the layers was observed after printing as shown in the optical micrographs in Figure 3.10. The agglomeration of MWCNTs occurred only in 3% and 5% wt. solutions. Agglomeration of nanotubes is more evident in less concentrated solution as compared to higher concentrations. Fluctuation in resistance values in bulk sample was observed at normal conditions without applying any stress or strain, which is possible due to the fast shifting of different conductive paths generated in the bulk MWCNT/PDMS composite (especially in higher concentrations and agglomerated sites). These fluctuations in resistance were observed even under compressive force on the devices.

Increase in resistance for all the three concentrations is detected when the substrates are wrapped in convex shape around a cylinder (15mm radius). This increase is caused by the bending induced strain. The conductive paths established during the normal position are enlarged which results in an increased resistance. Alternatively, decrease in resistance is recorded when the substrates are bent in concave shape. In this case, the conductive paths are pushed more closer, which results in increase in conductivity of the composite. This is interesting for robotic skin when mounted especially at joints, where contraction and relaxation during the movement can be monitored and controlled by using such type of strain sensors.

3.6. Conclusion

Arrays of all screen printed flexible pressure sensors presented here were obtained by sandwiching P(VDF-TrFE) and MWCNT/PDMS separately between two patterned silver layers. A total of 64 sensors have been fabricated in one flow by screen printing technique. Screen-printing is attractive for printed multi-layered electronic devices by using materials, which do not have any compatibility issues if printed layer by layer. Investigative study based on ease of processing, robustness, time saving, material efficiency and compatibility of layer-by-layer structures has been performed. Based on the physical characteristics of the printed layers, MWCNT/PDMS (3% wt.) nanocomposite show uniform patterned deposition and reusability of the solution for subsequent use. Based on the screen-printing experiments 3 wt. percentage solution of MWCNT/PDMS was observed to be close to the viscosity ranges required for screen-printing. In addition, the agglomeration in 3% wt. is less as compared to higher concentrations, which leads to approximately linear response and less fluctuations in resistance values of the sensors. There is no issue of porosity in MWCNT/PDMS layer as observed in P(VDF-TrFE) which help in reducing the extra processing process steps required for top electrode on a separate substrate. Also contact resistance in P(VDF-TrFE) with top electrode is expected to be higher as both the layers are not in intimate contact which is assumed to be one of the major drawbacks of P(VDF-TrFE) layers. Adhesion loss tests performed at different humidity conditions show delamination of P(VDF-TrFE) layer and poor adhesion to plastic substrates at raised temperatures as opposed to MWCNT/PDMS layers. Encapsulant in the form of PET substrate having

top electrode and force concentrator structures are used for covering P(VDF-TrFE) in order to avoid such conditions.

Maximum sensors response at optimum operating values for P(VDF-TrFE) and MWCNT/PDMS are 0.05 V/N and 20 kΩ/N respectively, which shows piezoresistive material to have broad range of response at static forces. The response of P(VDF-TrFE) devices is almost near to ideal linear response required for tactile sensing. An additional step of polarization is required to induce charges in P(VDF-TrFE) layer, which will enhance the sensor response. Albeit poor physical characteristics of screen-printed layers, P(VDF-TrFE) is ideal for dynamic forces at wide range of frequencies, which is useful in slip detection for tactile sensors on robotic skin. Although conductive polymer composites have the disadvantages of non-linearity, hysteresis and temperature drifts, they are simple, cost-effective to fabricate and effective for large strains.

Further investigation is needed to finding threshold for optimum concentration, enhancing dispersion and reducing agglomeration of MWCNT. The pressure-mapping device could be enabled for local differences of pressure by utilizing the patterning capability of composite materials. Further investigation of compatible solvents for P(VDF-TrFE), which have low evaporation rate during the printing process and matching-well with the viscosity requirements of the system will be explored. Characterizing whole array of devices and analysis of interference or cross talk will be investigated in future work. Whole package of screen printed foldable pressure sensor is targeted for development of low cost electronic skin applications. Successful patterning of P(VDF-TrFE) and MWCNT/PDMS nanocomposites in single step with reduced uniform thickness and the piezo-responses obtained, show that these sensors could find an attractive field of applications in not only electronic skin but in almost every enabling technology of large area electronic transducer system which needs light weight sensing devices attached conformably onto the surface.

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Chapter 4
Microfabrication of Si Microstructures

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Silicon (Si) is the second largest available material in earth's crust in different forms of silica (SiO_2) and silicates and is extracted from silica-rich sands through different processes. The generic processes for the purification of electronic grade Si and the manufacture of crystalline Si in variant wafer dimensions are very well established. The common industrial method used to get electronic grade Si in the form of single crystal is the Czochralski (CZ) method. In CZ process, a seed crystal attached to a rod is dipped and pulled back from molten Si, with a specific circular speed to control the Si orientation and ingot diameter [1-4]. The Si ingots are sliced into wafers usually through a wire-saw followed by subsequent steps of edge profiling, grinding, polishing and cleaning etc. Si has proved to be the dominantly used semiconductor materials in the microelectronics industry. It remained the attractive choice of research for more than 50 years and processing techniques to get Si in different crystalline structure have already matured. The high performance electronic components require a highly monocrystalline Si with negligible lattice defects [2, 3]. Additionally, high quality materials developed or implanted within the lattice are carried out at higher temperatures i.e. 1300 ^{o}C to activate the surfaces. State of the art planar electronics, where devices are fabricated on Si wafers are compatible with sustaining these much higher temperatures. However, getting Si on flexible polymeric substrates is challenging with the state of the art microfabrication procedures. Therefore, new techniques, where the single crystal Si in desired microstructures are transfer printed on secondary (polymeric) substrates after finishing all the high temperature steps on the wafer itself. This chapter highlights the state of the art microfabrication techniques for obtaining Si in various microstructures, thinning techniques to make Si flexible followed by transfer printing techniques to flexible substrates.

4.1. Microfabrication routes of Si

Microfabrication brought the revolution in miniaturization of structures and is still rapidly developing for MEMS (microelectromechanical), optical, fluidics and microanalysis systems. However, the basis of microfabrication and the fast development of the technology lies in the microelectronics technology especially for processing Silicon [5]. The Silicon crystal structure is regular, extensively studied and well understood and to a large extent, the properties are controllable for desired electronic applications. The extraordinary developments in microfabrication technology for Si in the last few decades provided the opportunities to explore the potentials of Si for a wide

range of devices. Tuning the intrinsic electronic properties of the Si and possibility to microfabricate electronic structures are increasingly central to modern science and technology. The opportunities in the advancement in technology is driven by the ease to fabricate microstructures in variant dimensions or to reconstitute the established structures in further downscale versions [5]. The block diagram in Figure 4.1 shows the prominent standard steps involved in the development of a typical microelectronic device using inorganic materials.

The whole process of microfabrication is dependent on a standard technique called photolithography. Lithography refers to process invented by Aloys Snefelder in 1796 and it refers to the writing on stones (Greek words lithos for stones and graphein for to write). Lithography can be used to print text or artwork onto paper or other suitable material [6]. Lithography has laid a strong foundation for today's microelectroelectronics technology in the shape of photolithography. In photolithography, a structure is patterned on a target substrate using a photosensitive polymer (usually called photoresist) and exposing to light through a patterned mask. The photomask consists of an opaque patterns (chrome or iron oxide) on an optically transparent support i.e. quartz. Two types i.e. negative and positive photoresists are practiced in the electronics industry and the photomask are designed accordingly to the type of materials used. The photoresist exposed to UV light becomes either more (positive resist) or less (negative resist) soluble in a developing solution. In either case, the pattern on the photomask is transferred into the film of photoresist [5]. After soft and hard bake steps, the patterns from the photoresist are transferred onto the target substrate by performing further development steps. The development steps involves solution processing of the photoresist to remove the unwanted (exposed or non-exposed) part of the photoresist. A typical electronic device consist of multi-layered structures and the combination of multiple photomasks with accurate alignment are at the heart of this development.

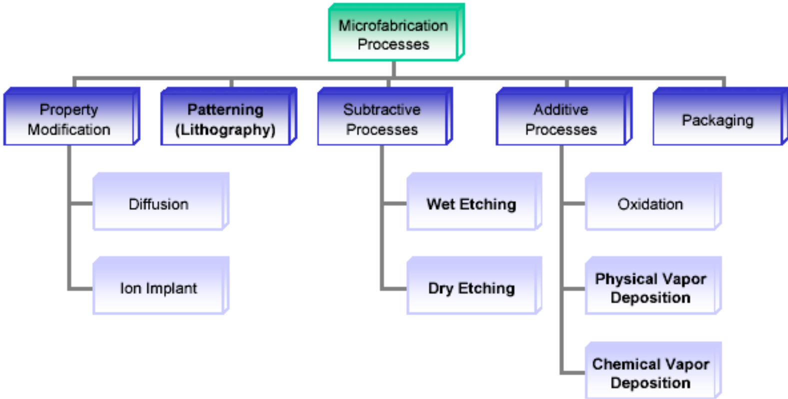


Figure 4.1. Microfabrication processing steps for microelectronics manufacturing.

Details of the intrinsic steps involved pattern transfer in the standard photolithography are described in the schematics of Figure 4.2. Here, negative photoresist has been selected for replicating the photomask patterns on an oxidized Si wafer. Initially the wafer is cleaned properly to remove any contaminants and then negative photoresist is spin coating on top of oxide layer of Si as shown in Figure 4.2 (a). The photoresists used in photolithography are usually sensitive to Ultraviolet (UV) light, as is the case in this example. The photoresist is exposed to UV light and rinsed in a developing solution, which removes the unexposed photoresist and leaves behind the exposed part to pattern the desired structures of the photomask in the subsequent developments as shown in Figure 4.2 (c & d). Now the pattern area is open for subtractive process of etching away the oxide layer and as a result, the Single crystal Si is exposed for desired processing. Patterned wafer is kept in HF solution, which etches away the oxide layer with a faster rate than the photoresist or the underlying Si shown in Figure 4.2 (e). The oxidized Si wafer with etched windows in the oxide (Figure 4.2 (f)) now awaits further processing. All the processing steps and chemical used in photolithography are matured enough and currently features as small as few nanometres are possible to be developed. This rapid advancement is not only not only for the two-dimensional structures, but technology for the high aspect ratio features desired for applications such as lab on a chip and or microelectromechanical systems have also been commercialized.

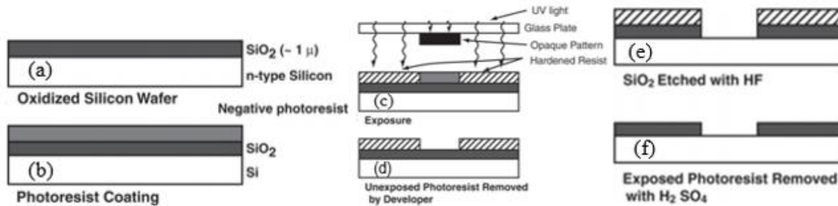


Figure. 4.2. Standard photolithography steps for transferring patterns form photomask on a desired substrates. (a) An oxidized Si wafer (b) photoresist coating, (c) exposure, (d) development, (e) oxide etching, and (f) resist stripping and oxide etching.

4.2. Flexible Substrates

It is the flexibility of polymer substrates, which is providing grounds for low cost high-speed manufacturing of flexible devices over large areas using various printing technologies in a R2R production line. To replace planar rigid substrates like bulk Si, the flexible substrates are required to possess properties such as dimensional stability, thermal stability, low coefficient of thermal expansion (CTE), excellent solvent resistance and good barrier properties for moisture and gases. There are three types of substrates that could be employed for flexible electronic devices: thin glass, metal foils and plastics [7-9]. Thin glass is bendable but the intrinsic brittle property limits its utility in flexible electronics. Metal foils on the other hand can sustain very high

temperatures and provide a window for inorganic materials to be deposited on it but the surface roughness and high cost of the materials hinder its use for flexible electronics.

Plastic materials are the potential candidates for applications requiring high degree of bendability, transparency and emissive properties. Plastic materials provide a reasonable trade-off between physical, chemical, mechanical and optical performance as described in Table 4.1. In addition, the central idea of the low cost flexible electronics (e.g. R2R manufacturing) is feasible with plastic substrates. The main issue in use of plastic substrates is the lower glass transition temperatures (Tg) (Figure. 4.3), which limits its utility to organic materials. Polymer substrates are divided into three main groups [7, 8] i.e. semi-crystalline, amorphous and solution cast amorphous. Semi-crystalline polymers used in flexible electronics include polyethylene terephthalate (PET), heat stabilized PET, polyethylene napthalate (PEN), and heat stabilized PEN and polyetheretherketone (PEEK). Amorphous polymer substrates include polycarbonate (PC) and Polyethersulphone (PES), which are non-crystalline thermoplastics that can be melt-extruded or solvent casted [10]. Some of the amorphous group that cannot be melt processed include such as modified polycarbonate (PC), Polyethersulphone (PES), polyarylate (PAR), polycyclic olefin (PCO) or polynorbonene (PNB) and polyimide (PI). These substrate materials are discussed in detail in [7, 8, 11].

The semi-crystalline polymer substrates with Tg higher than 140°C (e.g. heat stabilized PET and PEN) generally tend to have high melting points, which allows the polymers to be melt processed without significant degradation [8]. The effect of thermal stress and mismatch between the CTE of substrates and the deposited material are

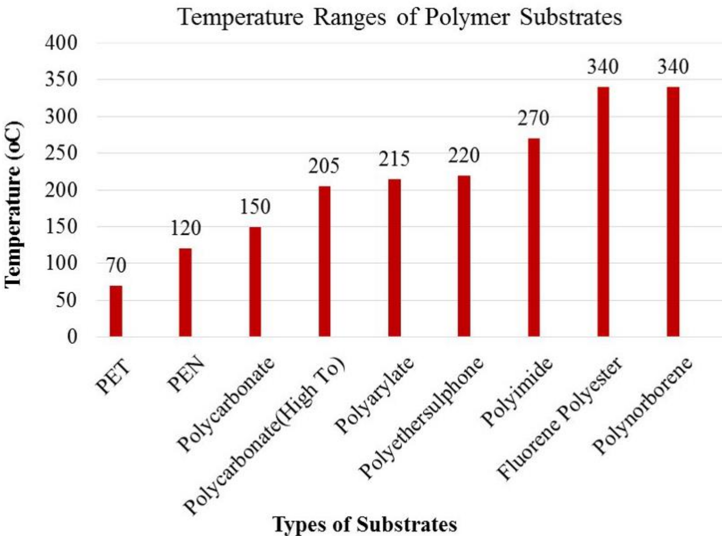


Figure 4.3. Glass transition temperatures of commonly used plastic substrates in printed electronics.

critical for efficient performance of the electronic devices. This means if material with different CTE (e.g. amorphous polymers have CTE 50ppm/°C below Tg) deposited on top of these substrates can expand 3 times, above the Tg value of the substrates, ultimately causing undesirable mismatch in the fabricated structures vis-à-vis original layout [8, 12]. Applications such as RFID, sensors, active matrix backplane, OTFTs and OLEDs etc. also affect the choice of substrate. For display applications, optical clarity is important where a total light transmission (TLT) of > 85% over a wavelength range of 400-800nm are required [8, 11, 13]. This is only required for light emission through substrates in bottom-emission and electrophoretic displays. To overcome the challenge of humidity absorption, a thin barrier coating of transparent oxides is applied on the surfaces of polymer substrates, especially for sensors used in food and medical packaging. In nutshell, to replace planar substrates, the polymer substrates should mimic their properties such as dimensional stability, thermal stability, low CTE, excellent resistance and good barrier properties for moisture, air and gases [7-9].

Table 4.1

Comparison of Polymer substrates [4]

Property	PET	PAcr	PEN	PC	PS	PI
Tg (°C)	70	105	120	145	203	270
Upper Tm (°C)	115	175	268	115-160	180-220	250-320
CTE (ppm/°C)	33	70	20	75	54	8-20
% Transparency	90	>90	88	92	89	35-60
Water Absorption (%)	0.6	0.2	0.4	0.25	1.4	2-3
Y. Modulus ($10^9 N/m^2$Gpa)	2-2.7	2.4-3.4	0.1-0.5	2.6	-	2.5
Solvent Resistance	Good	Good	Good	Poor	Poor	Good
Surface Roughness	Poor	Fair	Poor	Good	Good	Good
Dimensional Stability	Good	Good	Good	Fair	Fair	Fair

4.3. Towards Flexible Silicon

There has been a growing interest in realizing electronic components on nonconventional polymeric substrates (Figure 4.3) to obtain flexible, foldable and stretchable electronic systems for applications requiring ultra-high bending such as implantable electronics, displays and robotic skins etc. [14, 15]. Tremendous progress has been made in the field of flexible electronics in the last decade focusing mainly on the materials development and cost effective manufacturing of the innovative electronic structures. Materials still remain the more challenging part and different types of materials have been investigated especially solution based organic materials [16]. The

attractive properties of organic materials suit well the requirements of the flexible electronics especially the mechanical flexibility and solution processability for low fabrication costs [17, 18]. Despite the attractions and suitability for integration to flexible substrates, organic materials are faced with many challenges of high-speed performance for fast switching transistors or by the requirements of high drive currents for the backplane transistors array of an active matrix display [19]. The charge carrier mobility is extremely low i.e. ~1 cm^2/V.sec for organic semiconductors compared to their inorganic counterparts especially Si which have very high carrier mobility i.e. ~ 1000 cm^2/V.sec [19, 20]. Additionally, the short lifetime, nonstability in variant conditions and fast electrical and physical degradation of the thin layers make it more challenging for use in reliable flexible electronic components [21]. The organic semiconductor-based analogue and digital electronics is not sufficient to meet many challenges, especially those related to high performance requirements of active circuits for large area pressure sensors. They are severely unstable to design analogue circuit and sensor blocks such as comparators, amplifiers and ADCs [22, 23].

To overcome the abovementioned challenges, new forms of high mobility material such as single crystal Si nanowires and ultra-thin chips have been investigated recently [22, 24, 25]. The Si nano/microscale structures based devices are emerging rapidly and have gained significant interest during the last decade. Similarly, ultra-thin flexible chips are also promising as they enable compact electronics and are bendable [23]. Si chips are traditionally built on wafers whose thicknesses are in the range of 100 micrometres. These wafers are intrinsically brittle, thus limiting their use in the development of flexible electronics. Flexibility can be induced into Si wafer if it is thinned below 50 μm, in the range of 20–50 μm. In addition, at 10 μm range, the Si exhibits a transparent nature, therefore enabling its usage in displays applications [22]. These ultra-thin flexible Si chips can be transferred onto a polymeric foil to form system in foil (SiF) devices for different electronic applications [23]. Thinning of Si chips are generally achieved either by physical or chemical methods as shown in Figure 4.4 (a & b). Among the physical methods, back grinding of wafer is the most popular method for thinning of wafer using a grinder wheel [26]. Traditionally, the removal rate

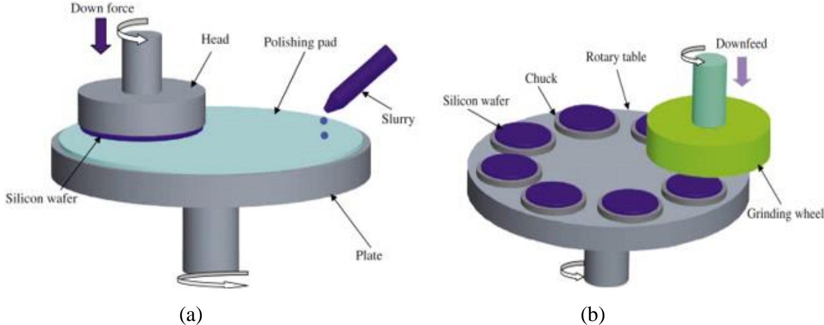


Figure 4.4. Schematics of chemical mechanical polishing, (b). Blanchard-type wafer grinding [26]

for back grinding ranges from 0.1−100 μm/min [27, 28]. The back grinding of the sample causes sub surface damage and crack at the edges. The thinned wafers are transferred using a carrier wafer, following which the thin membrane is eventually removed [26]. In addition, thin Si-based devices and nanomembranes can also be achieved by chemical etching of Si wafer. Chemical etching of Si can be achieved either via both dry and wet etching process. The thinned Si is removed from wafers by etching the underlying layer. Some of the widely used wet etchants of Si are ethylenediamine pyrocatechol (EDP), potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH). Wet etching of samples lead to undercutting [29], which could be evaded by using dry etching process. Common dry etching techniques include: (1) Plasma systems; (2) Ion etching; (3) Reactive ion etching. Some of the new techniques include Dicing Before Grinding (DBG), [30] thinning of wafer by a combination of selective wet etching and back grinding process. The devices are fabricated on top of epitaxial grown Si. Other available techniques for thinning of chip includes Chip film, Hyperion and Taiko [22, 31, 32]. Despite the progress and achievements of the ultra-thin Si chips in improvement of the bendable electronics, the conventional BSIM (Berkeley Short-channel IGFET Model) [33] models fail to predict the behaviour of such devices since they are appropriate for rigid and planar structures. These models need to characterise and capture the effects related to uniaxial, biaxial and shear stress, which is important from circuit design aspect as well as various bendable electronics applications [33].

Si device layer of the SOI (silicon on insulator) wafers is another way for obtaining thin Si chips, where the devices are fabricated using standard semiconductor fabrication process on the active layer of mono-crystalline silicon with predefined thickness over the buried oxide. Thin chips can be obtained from SOI wafer by two ways: (1) By creating deep trenches from front side to the buried oxide level and then etching it away lifting of the top layer as membrane, or (2) The backside bulk wafer may be removed by etching it in selective etchant like TMAH with oxide as the etch stop layer [34]. Near optimum results can be achieved using SOI wafers. Before etching step, the circuits realized on the top of the wafer have to be supported and protected. However, SOI wafers are of much higher cost and can be used only for high-end applications. [35].

4.4. Si Micro/nanowires

4.4.1. Top-down and Bottom-up approaches

Nanowires (NWs) of inorganic materials are attractive choice for realizing electronics on flexible polymeric substrate for diverse applications [36, 37]. Semiconducting nanowires possess interesting electrical, optical, mechanical and electrochemical properties [37]. Device prototypes in the areas of nano-electronics, sensors, optoelectronics and photovoltaics have been demonstrated by utilizing these properties [38-41]. Two distinct fabrication routes such as bottom-up and top-down for obtaining Si microstructures in the shape of nano/microwires have been developed as shown in Figure 4.5 (a-d) [38, 42]. In the bottom-up fabrication techniques the nanostructures are developed by placing atoms or molecules one at a time along a preferred direction

(usually vertically for wires configurations). Such processes are time consuming and so self-assembly, techniques are employed where the atoms arrange themselves as required. Additionally the poor control over geometry, uniformity, doping level and above all deterministic transfer to secondary or flexible substrates make the bottom-up approach further challenging [23, 38]. Alternatively, top-down fabrication can be likened to sculpting from a block of stone. Parts of the unwanted materials are gradually eroded until the desired shape and dimensions are achieved. The nanotechnology techniques vary for obtaining nanowires and the fabrication routes are optimized both by combination of standard lithography and etching techniques [37]. Depending upon the level of resolution required for features in the final product, etching of the base material can be done chemically using acids or mechanically with the help of ultraviolet light, x-rays or electron beams. The top-down approach is considered to be the most efficient for obtaining wires of varying dimensions from few nanometres to hundreds of nanometre size. Technology is available for developing both planar and vertical wires in

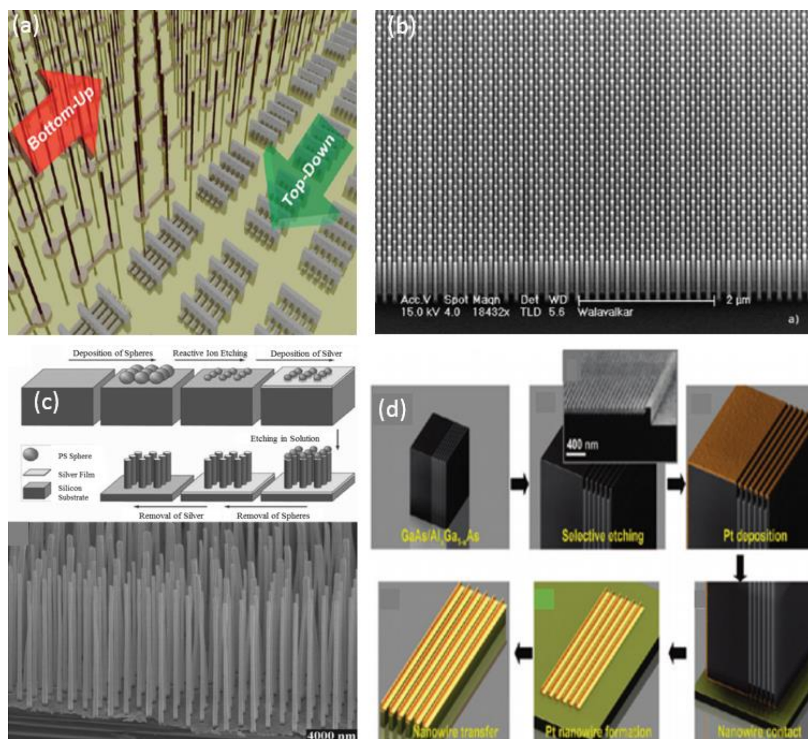


Figure 4.5. (a). Outlook of top-down and bottom-up approaches, (b). SEM image of an array of 50 nm diameter Si nanowires etched into a Si wafer. A sputtered Al_2O_3 hard mask, patterned by EBL (c). Schematic of NSL process for the fabrication of vertical Si nanowire arrays via metal assisted etching (MAE) (d). Schematic of the SNAP process for production of aligned nanowires [41].

bulk by using standard Si wafers. Top-down approach allows the development of nano/microwires through systematic and controlled processing conditions, which helps in minimizing geometric variations (i.e. thickness, width and length of wires) and maintain the preferred crystallinity and doping profiles of the wires. It is less time-consuming and cost effective as compared to the bottom-up approach [25, 37, 43].

4.4.2. Vertically aligned micro/nanowires development

Extensive research has been carried out in both the areas of novel bottom-up and top-down synthesis routes for the synthesizing single crystalline Si nanowires with structural and atomic level composition control [43]. For example, catalyst particle assisted vapour-liquid-solid (VLS) mechanism is successful for the synthesis of elementary to ternary semiconducting nanowire hetero-structures. High carrier mobility and mechanical flexibility of the NWs makes them suitable for flexible electronics applications as shown in Figure 4.6 [37]. Ge/Si core-shell NW based pressure sensors over polyimide substrates have been demonstrated as an artificial e-skin [44] by Ali Javey and co-workers. Vertically grown Ge/Si NW arrays have been transferred horizontally over polyimide material by dry contact printing process. NW FETs were fabricated over flexible polyimide substrate with a pressure sensitive rubber on the top of the device stack. The structure has been demonstrated over an area of 7x7 cm^2 with a spatial resolution of ~0.4 x 0.4 cm^2 was attained with arrays of nano-wire taxel

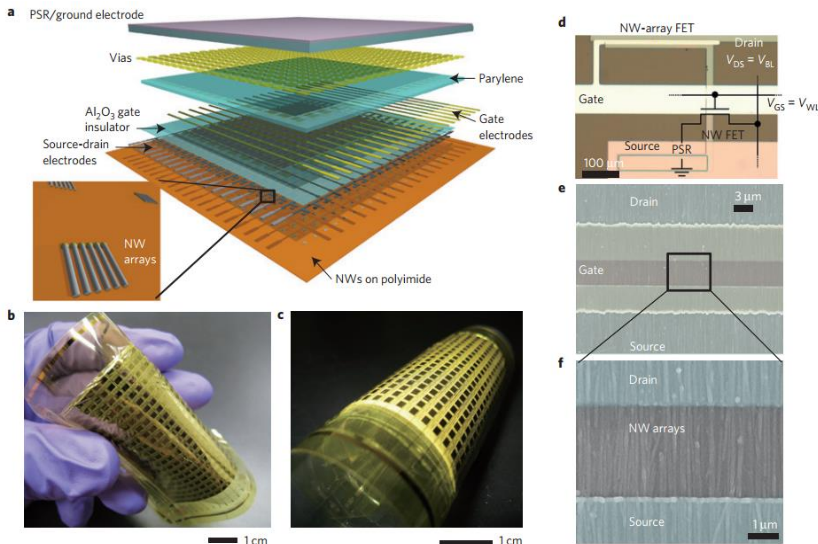


Figure 4.6. Nanowire-based macroscale flexible devices, (a). Schematic of the passive and active layers of NW e-skin. (b) & (c). Optical photographs of a fully fabricated e-skin device. (d). Optical-microscope image of a single sensor pixel in the array. (e) & (f). Scanning electron micrographs of a NW-array FET [43].

elements. This depicts a proof-of-concept of application of nanowires to fabricate macroscale tactile skin for robotics and prosthetics [45]. The device circuitry operates at less than 5 V with response time of less than 100 ms. The circuit conductance has been tested up to 2000 bending cycles to evaluate the flexibility and mechanical robustness of the nanowires. Stable performance has been observed up to the bending radius of 2.5 mm, which has been attributed to the nano-sized wires as device components. Besides development of elemental Si nanowires, research is also carried out in development of compound semiconductors for a range of applications. In compound semiconductors, zinc oxide nanowires have shown to be the tactile sensing elements based on piezotronic transduction mechanism [46]. As-grown vertical ZnO nanowires have been used for the fabrication of large area self-powered tactile imaging circuits. This brings an opportunity to directly integrate material synthesis, device fabrication and mechanical actuation. As against conventional vertical wrap gated FETs [47], ZnO piezotronic transistor consisting of metal-semiconductor-metal junctions which utilizes polarization of immobile ions for device operation has been demonstrated. The conductivity in the NW channel is modulated by the externally applied stress over the metal surfaces. Hence, the transport characteristics are affected by externally applied strain, which effects the polarization in the nanowire.

Besides tactile sensing applications, additional sensing/functional capabilities such as temperature sensing, chemical sensors, gas sensors, texture recognition, distributed heating and circuits for signal conditioning are also central to the scope of nanowires development. The reliable sensing and electronics need to be developed with these new approaches to make it perform in par/more competitive to the state of art electronic components. This is very well possible using silicon nanowire based approach in tandem with various devices and sensors realized with inorganic nanowires. Silicon nano-ribbons based transduction mechanisms have been demonstrated to sense light and temperature [48]. A six inch wafer scale vertically developed silicon microwire arrays as shown in Figure 4.7 have demonstrated tremendous progress towards low-cost, high-efficiency photovoltaics and photo electrochemical fuel generation [49, 50]. The high-

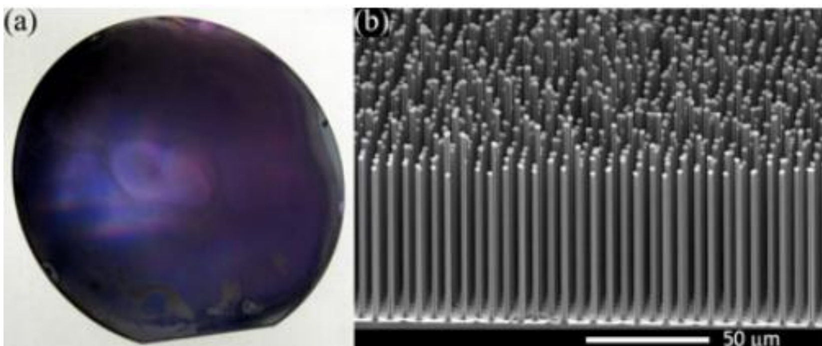


Figure 4.7. Photograph of a six-inch wafer covered in Si microwires (left) and SEM image of these wires (right). The wafer was cleaved to enable imaging of wires near its center [49].

aspect ratio and radial junctions of the vertical Si microwire arrays absorb nearly all the incident solar, light that enables the minority carrier collection in the radial directions. Optimal techniques have been developed and progress made towards a full six-inch wafer-scale growth of Si microwire arrays for photovoltaics and solar fuel generation [50]. Embedding these microwires in a polymer and removing afterwards from the mother wafers to be deployed on flexible polymeric substrates [41, 49, 50]. However, utilization of the full potential of the elementary and compound semiconductor NWs is delayed by transfer related issues [51] to secondary polymeric substrates. Current transfer printing processes need to be scaled up for large area and deterministic printing. Developments of new manufacture friendly transfer process certainly help to benefit more from semiconducting nanowires.

4.4.3. Planar Si Microwires Fabrication

Another class of Si microwires, fabricated in planar mode through standard photolithography techniques such as reactive ion etching have attracted significant interest in recent years. Different application areas have been explored ranging from solar cells, electrochemical fuel cell, artificial photosynthesis and pressure sensors on flexible substrates [52-54]. Among these developed technologies and structures, incorporating Si based microstructures with diverse materials have greater potential to be implemented for measuring variety of physical parameters like strain, pressure and temperature. Using solution based materials such as poly(vinyledene-trifluoroethylene) (P(VDF-TrFE)) with single crystal Si is one such example, where it has already been exploited as a pressure sensor in the shape of a POSFET device [55]. However, these type of devices are realized on a rigid silicon wafer and the need for application of such structures on non-planar flexible substrates is primarily required for development of conformable electronics. To address this issue and realize flexible electronics on polymeric substrates where single crystal Si microstructures and solution processed transducer materials are stacked on top of it are recently developed [56, 57]. One such model where fabrication and characterization of a Si-based flexible triboelectric active sensor array for self-powered static and dynamic pressure detection and tactile imaging with batch microfabrication process is presented [58].

The challenges for flexible systems are addressed through monolithic integration of nano-membranes fabricated with top-down approach for stretchable electronics on a polymeric substrate [59]. The electronic components developed by using Si nanomembranes have shown very promising results. However, due to the limitations of physical and mechanical properties like brittleness of Si, a small dislocation or cavity in the material crystal structure can propagate the cracks abruptly for large area membranes. Delamination of Si nanomembranes from the polymeric stamp under their own weight can propagate even further these cracks and affect the transfer yield. Therefore, an alternative technique for reducing the sizes and changing the shape from Si nanomembranes to micro/nanowires would assist in overcoming these issues. The

high-mobility inorganic semiconductors with controlled thicknesses and uniform widths in the range of a few micrometres are promising solutions for high performance flexible electronics and systems. Silicon micro/nanowires exhibit high carrier mobility, high performance and excellent stability in flexible and foldable electronics applications.

The procedure for development starts with designing, developing and transferring of silicon micro/nanowires in planar mode from a standard bulk silicon or silicon on insulator (SOI) wafers to a secondary polymeric substrate. Various sensors have been reported by using this technology in which Si microstructures are translated to polymeric substrates, where all the high temperature processes are performed on the donor wafer and are transferred afterwards. A top down approach is practiced to develop Si micro/nanowires using standard photolithography and etching techniques. Si microwires are developed by deep reactive ion etching in which wires with desired widths are developed with specific trenches in between consecutive wires. The capability to develop deep trenches in SOI wafers to maintain the high resolution of the shadowed material with minimum variations in the designed dimensions are the attractive features of deep reactive ion etching (DRIE). To maintain the performance of the finally assembled microwires based devices in close ranges, uniformity of the wires structures is of great importance [60]. In DRIE process, the etching of Si through high-density plasma can be achieved by two different approach. In the standard approach, all the gases are fed in one cycle where etching and passivation of the sidewall are performed at the same time while the etching and passivation gases are flowed

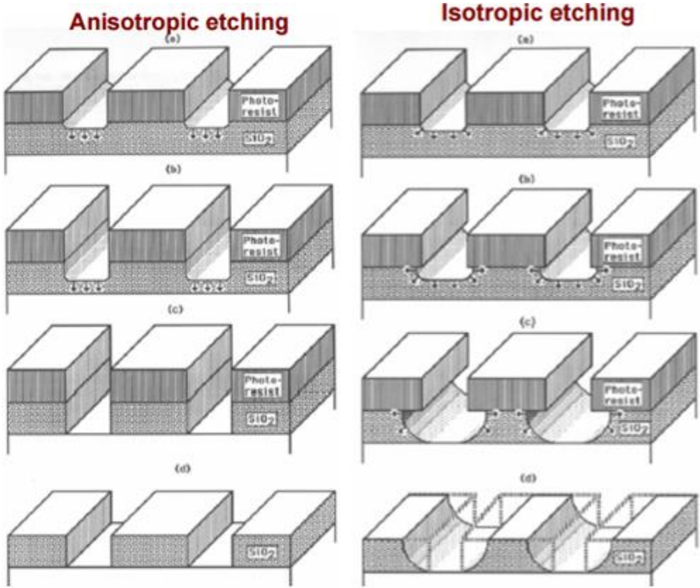


Figure 4.8. Etching protocol for getting an-isotropic and isotropic structures. Development of such structures depends on the requirements of final applications.

independently in an alternative way of time-multiplexing technique. Anisotropic etching as shown in Figure. 4.8 guarantees the uniform edges and thickness of the Si microwires.

4.5. Design of the Si Microwires

The photomask for fabrication of Si microwires is developed by using L-Edit (Layout Editor from Tanner, Electronic Design and Automation). This is a computer aided drawing tool used to design the two-dimensional wires by introducing opaque or clear area in the mask for trenches. Trench is the area where the Si device layer of the SOI wafer is removed anisotropically using DRIE processes. Wires with different combinations of lengths and widths are fabricated in order to investigate and optimize the transfer of the microwires. The active area of contact between the polymeric stamp and Si microwire is of prime importance affecting significantly both the transfer steps from SOI to stamp and from stamp to secondary substrate. Figure. 4.9 (a) shows microwire designs on wafer scale with varying lengths and widths. Length of the wire is also important to be explored as the wires often break or delaminates owing to their longer lengths and not enacting with the stamp. Therefore, for these investigations, wires of varying widths and trenches such as 4, 6, 8, 10, 20 and 50 µm were fabricated with lengths of 30, 50, 100, 150, 200, 1000 and 5000 µm. In the photomask, 10 instances of arrays of each wires combination were designed where each instance

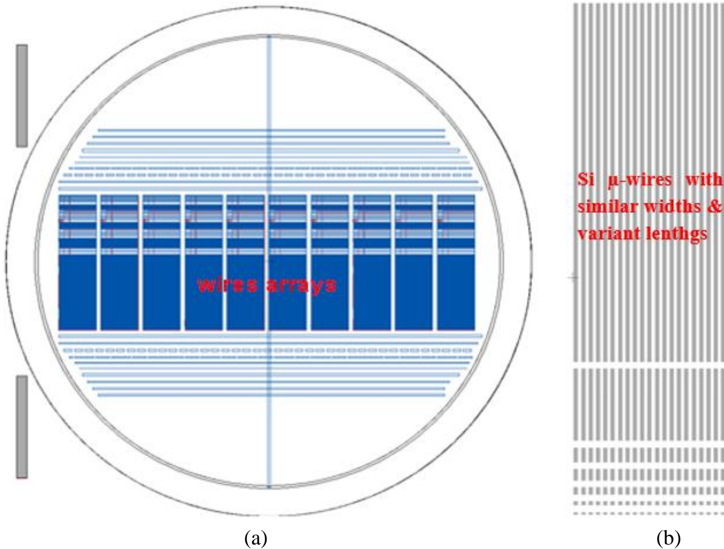
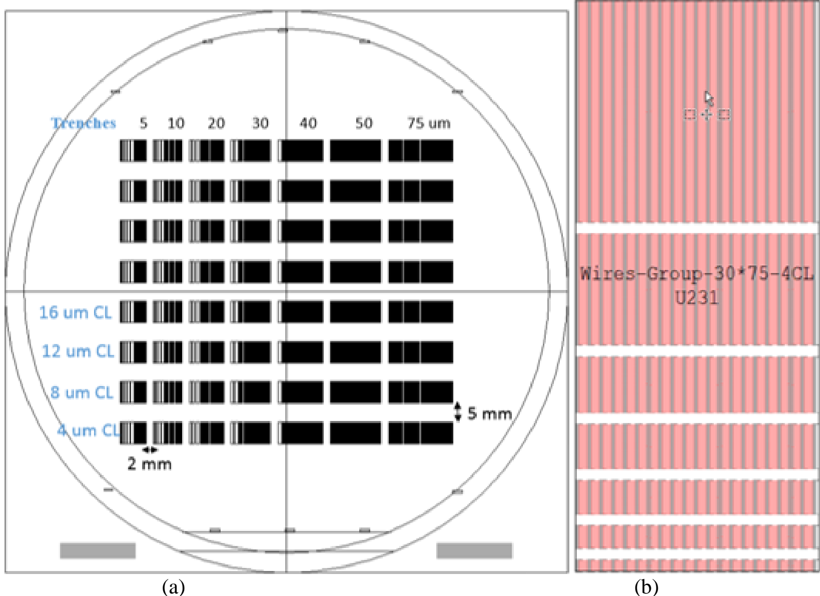


Figure. 4.9. (a). 10 instances of arrays, each including: 20 wires per each dimension, For all combination of: Length (30, 50, 100, 150, 200, 1000, 5000µm) Wire width (4, 6, 8, 10, 20, 50) µm and Trench width (4, 8, 10, 20, 50) µm; (b). Example of array with variable length x fixed wire width x fixed trench width.

consisted of 20 wires each. Figure 4.9 (b) shows one such example of wires combination showing different lengths but similar width and trenches. Wires developed in this mask were completed without any further modification of the doping concentration through implant or diffusion processes.

To further enhance the wires design based on the experimental observation of the above-mentioned mask, a modified version of mask was prepared where stress intensifiers at the tethered positions were introduced to promote the detachment of the wires from the donor wafer during first transfer step. Additionally, to further enhance the metal contacts and promote the metal-Si contact with less schottky barriers, microwires were heavily doped at the edges by leaving an undoped region in the centre. This undoped region is left as channel area to simplify the design process of metal insulator field effect transistors. The less doped area will act as the active channel for the MISFET devices minimizing the tolerances occurring due to variations in the post-processing of metallization. In the new design, the wires dimensions are changed from the previous mask. Here the maximum lengths have been reduced to 2 mm for two reasons. First is to avoid the breaking of long wires observed in the experiments performed for the transfer printing and secondly to maximize the wafer utilization by reducing the unwanted long wires. Further, the widths have also been modified in the



(a) (b)

Figure. 4.10. (a). Two instances of arrays, each including: 10 wires per each dimension, each module all the wires combination with similar trench as well as length (200, 300, 400, 500, 1000, 2000) µm, Wire width (5, 10, 20, 30, 40, 50, 75) µm and Trench width (5, 10, 20, 30, 40, 50, 75) µm; (b). Example of array with variable length x fixed wire width 30 µm fixed trench width of 75 µm with channel area of 4 µm.

new design; here the wires have varying widths of 5, 10, 20, 30, 40, 50 and 75 µm. Figure 3.10 shows wafer scale design of wires in the second mask where the widths and lengths of the wires have been modified from the previous mask.

The smaller dimension wires i.e. 4, 6, 8 and 10 µm are challenging to be picked up from the donor wafer in the first transfer steps and also deterministic printing on the target substrate with 100 % transfer yield. Therefore, all the new wires dimension have been modified based on the experiences observed during the experiments performed with the firstly designed mask. Two instances of all the wires' groupings have been designed where each instance contain 7 arrays of all combination of the wires. Each module of wires combinations are designed with similar trench widths and channel area of the undoped region as shown in Figure 4.11. Details of the wires physical and electrical performances are discussed in more detail in the forthcoming chapters.

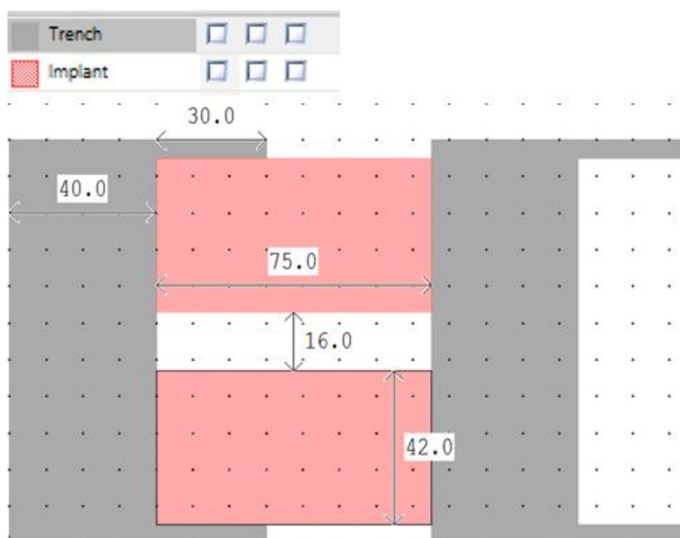


Figure. 4.11. Example of a single wire with 40 um trench, 75 µm width and 16 µm channel area. Anchored area (stress intensifier) is also kept at 30 µm connected to the trench junction.

The development of Si microwires starts by selecting a P-doped SOI wafer having resistivity ~15 Ω. cm. The photolithography starts with standard cleaning process of RCA and then coating with positive photoresist to define the alignment marks followed by a development stage. The alignment markers are plasma etched and the photoresist is removed in ashing and wet resist removal steps. After the alignment markers are developed, another step of positive photoresist coating is performed for the ion implantation. The implant area is developed and the photoresist is hard baked. Phosphorous is implanted in the open areas at a concentration of 1015 (standard). After implantation step, the photoresist is ashed and removed through wet etching. The wafer is heated to around 925 ^{o}C to drive in the phosphorous for uniform diffusion. A pre-

litho clean is performed before defining the trench areas. A positive photoresist is coated to define the trench structures and the developed afterwards. Deep Reactive Ion Etching (DRIE Alcatel) is performed to etch anisotropically the 500 nm Si device layer. After ashing and wet-etching, the photoresist is removed and cleaned finally by standard procedures. The various Silicon microwires developed are shown in Figure 4.12 (a-c), where proper control over thickness and dimensions are shown clearly.

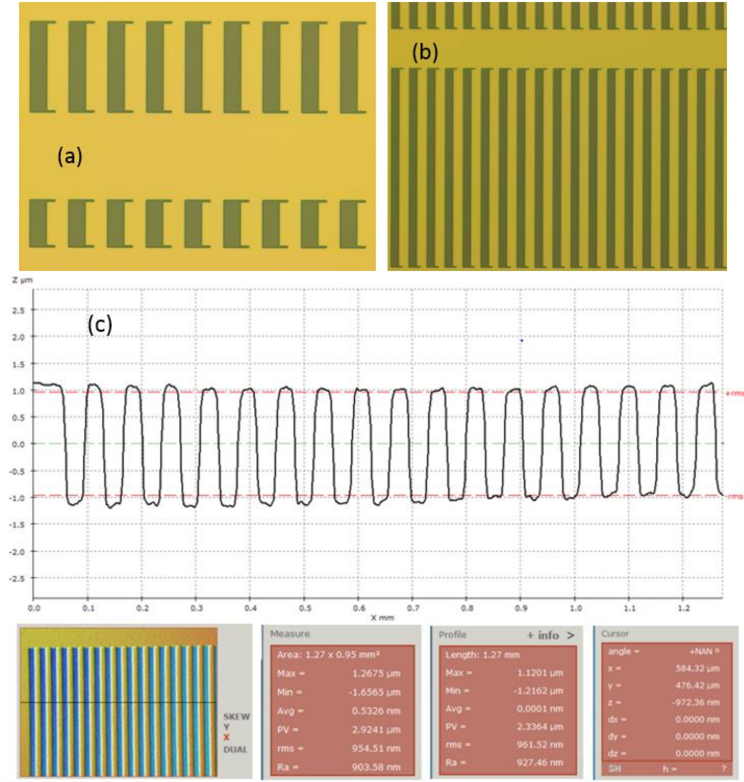


Figure. 4.12. Optical graphs of Si microwires after photolithography and DRIE etching. (a) Si microwire with 50 µm trench, µm um width and 30 µm stress intensifier, (b) Si microwire with 40 µm and 30 µm trench and 20 µm stress intensifier. (c) Optical interferometer graph of the wires showing uniformity of the wires widths and trenches' depths.

After successful fabrication of Si microwires on SOI wafers, the developed structures are kept in buffered HF solution to etch away the buried oxide. The duration of under-etching, the oxide layer is dependent on the size of microwires. In our experiments, we have observed more than 95 % transfer yield in the first transfer steps by doing and extra over-etching of around 15 minutes. This confirms the complete removal of the buried oxide layer of the SOI wafer. Sometime, a piranha (solution of H_2SO_4 and

H2O2) is used before the etching step to completely remove any residual organic layers coated during the photolithography and DRIE processes. Wires are watched with acetone, isopropanol and deionized water gently after etching and kept in an oven for 10 minutes at 100 ^oC. Figure 4.13 shows optical micrograph of under-etched Si microwires before transferring to PDMS stamp. Transfer of Si microwires (discussed in more detail in chapter 5-7) to a secondary substrate take either the route of wet assembly or dry transfer printing. In wet assembly, the developed Si microwires are dispersed in a solution and deposited on the desired substrates at preferred locations. In this process the orientation of the finished surfaces of the Si microwires and doped sides cannot be maintained for further processing due to random dispersion of the microwires in the solution. As against, in dry transfer method a highly planar polymeric stamp made of PDMS is commonly used to pick the developed microstructures from donor wafer and transfer it onto a secondary plastic substrate with the desired orientation.

Figure. 4.13. Optical micrograph of the under-etched Si microwires before transferring to secondary substrate by a PDMS stamp.

4.6. Conclusion

The conventional microfabrication techniques used for development of for Si based microstructures is presented in this chapter. The different techniques to develop Si wafers and use them for development of microstructures by using standard photolithography techniques is described. Embarking onto the field of flexible electronics require flexible and foldable substrates without causing deterioration to the physical and mechanical properties of the substrate as well as the electronic devices developed on top of them. These different flexible and polymeric substrates are overviewed in this chapter with the specific requirements and critical thermal budgets. The development of reliable and high speed active electronics for supporting passive

pressure sensors need to incorporate inorganic microstructures as the semiconducting layers in the switching devices. For this purpose, Si in the shape of microwires are chosen for development of such devices. Different techniques of thinning down to make Si flexible and conformable to polymeric substrates are described. Two different approaches of top-down and bottom-up are presented here. The final section of this chapter discussed the development of photomasks for fabrication of Si microwires used in this research. Detailed description of the process development of planar microwires on a SOI wafer is presented. Investigations in this chapter related to development of Si microwires and their transfer to flexible substrate work as foundation, which lead to the advancements of functional devices in the forthcoming chapters.

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Chapter 5
Metallization and Characteristics of Si Microwires

Part of this thesis has been published in:

S. Khan, R. S. Dahiya and L. Lorenzelli, "**Flexible thermoelectric generator based on transfer printed Si microwires**", *44th ESSDERC, IEEE, 86-89, 2014*

Efficacy of the Si microwires need to be demonstrated with their useful application in a working device. A typical electronic device is constructed with three major functional materials such as conductor, semiconductors and insulators. Electronic components are manufactured by stacking layers or patterned films of these materials fulfilling the specific requirements of the physical and electrical properties. Towards the advancement of an electronic device, the foremost contact made is of a metal and semiconductor. Metal semiconductor junction is found in almost all electronic devices and therefore this is considered as the most important and preliminary part of the fabrication process. Therefore, the Si microwires transferred from donor wafers to flexible substrates need a suitable metallic material to pave way for wires-based electronic devices. This chapter explores different conductors interfacing with the silicon microwires especially a metallic ink of Silver (Ag) and an organic conductor i.e. PEDOT-PSS. Different patterning techniques have also been part of discussion within this chapter. Current-voltage response of the Si microwires in asymmetric metal-semiconductor-metal (MSM) configuration is investigated in different orientations as well response to the light illumination of the wires is discussed. The variations in the current response are also investigated on the type of doping and the transfer printing strategies i.e. flip-over and stamp-assisted transfer of Si microwires.

5.1. Introduction to Asymmetric MSM structures

Metal-semiconductor heterojunctions are contacts between two different materials resulting into very interesting electrical and electro-optical properties [1-4]. These type of contacts are of significant importance since they are present in all electronic devices in the shape of a discrete component or an intrinsic part of the device. A potential barrier is formed when metal is contacted with a semiconductor, which is responsible for controlling the current conduction and its capacitance behaviour [5]. The difference of the work function of the two contacting materials is very critical and this difference could be adjusted either by choosing a suitable metal or by changing the doping concentration of the semiconductor, which ultimately changes the electron affinity of the semiconductor material [6, 7]. Their behaviour is mainly dependent on the interface characteristics forming either schottky or ohmic contacts. The differences of the work functions and interface states define the barriers to be either having schottky or ohmic behaviour [6, 7]. Schottky barrier junctions are one of the simplest and exciting electronic devices, which have found attractions for variety of applications in integrated

circuits, photo, and power diodes [6, 7]. It has remained the attractive choice in modern electronics owing to their simple device structure, low capacitances and fast response [5]. Understanding the schottky barrier height is an important parameter for many electronic devices such as field effect transistors and asymmetric metal-semiconductor-metal photodetector structures. Adjustment of the barrier heights to the desirable lower junction potential values can lead to significant improvement of the device performances. The main reasons of deviations of experimental barrier heights from the ideal conditions are either an unavoidable interface layer or the presence of interface states [8]. Therefore, proper selection of materials and the manufacture process is important for controlled deposition and patterning for the desired properties.

A typical structure of MS junction diode is constructed by depositing metal on both the sides of a semiconductor material with desired doping concentrations. Recently new type of structures are investigated where the semiconductor is in the shape of micro or nanowires with metal deposited at both the ends. These asymmetric metal/semiconductor/metal (MSM) devices have attracted significant interest [2] especially in the field of flexible electronics where the semiconductor microwires are deployed on nonconventional flexible substrates [1, 3, 5, 6]. Among different compound and elemental inorganic semiconductors, Silicon (Si) has been the first choice for such investigations owing to its matured processing as well as well-known mechanical and electrical properties. Tuneable electrical properties by changing the type and doping concentrations effectively, these high aspect ratio microwires are foreseen to have significant contribution towards development of flexible sensors such as temperature, photodetectors and piezotronics [3, 9-11]. Si has also been found to possess piezoresistive behaviour while undergoing through compressive or tensile strains [9]. Piezoresistance in microwires is related to the change in electrical response during bend conditions both in convex and in concave orientations of the Si microwires. This characteristic of the microwires could readily be exploited for piezotronics. These type of sensors are ideal for applications such as a robotic skin, where strain related actions are desired to be monitored for dexterous manipulation of tasks.

To effectively utilize the Si microwires and design a process protocol for successful fabrication of devices, materials with compatible electrical and mechanical properties are highly desired to maintain the higher electrical performance as well as mechanical flexibility of the devices. Efficient functioning of metal contacts with microwires have attracted potential interest for applications such as solar fuel cells, artificial photosynthesis, strain sensors, piezo-photottronics detectors etc. [3, 10, 12]. The higher surface-to-volume ratio of the Si microwires make it interesting for these diverse applications. After transfer printing (discussed in chapter 2&4) of the Si microwires, a feasible as well as cost-effective patterning technique for the metal contacts is a challenging task. To compensate the higher cost involved during the photolithography and DRIE etching process, solution based manufacturing is the preferred option for the post-processing steps. The low cost printing technologies especially inkjet printing and spray coating are the most promising approaches for such type of devices. For

developing the asymmetric MSM structure, only patterned deposition of the conductor materials is required to complete the structure. Therefore, two different types of conductor solutions are utilized using spray coating technology to investigate the performance of each with the Si microwires. Metallic solution based on silver (Ag) nanoparticles and an organic conductor i.e. PEDOT-PSS is used for these purposes. Experimental investigation is done for fabricating and characterizing asymmetric MSM structures based on two differently doped Si microwires transferred to flexible substrates. This chapter discusses the patterning techniques, conductive materials followed by electrical characterization in planar and bent orientations. The MSM structures are also characterized at different light illumination to explore the possibilities to use the Si microwires as flexible photodetectors. MSM photodetectors are very interesting owing to their good electrical bandwidth, fast response, small capacitance, large available active area to be used as an optical sensor [1, 2, 13].

5.2. Materials and Experimental Procedures

5.2.1. Type of Si microwires

Two different types of Si microwires are used in the investigation of MSM structures i.e. p and n-type wires. Details of the fabrication process and transferring them onto secondary flexible substrates are discussed in the chapter 3. For the p-doped wires, the microwires were developed on the SOI wafers without altering the doping

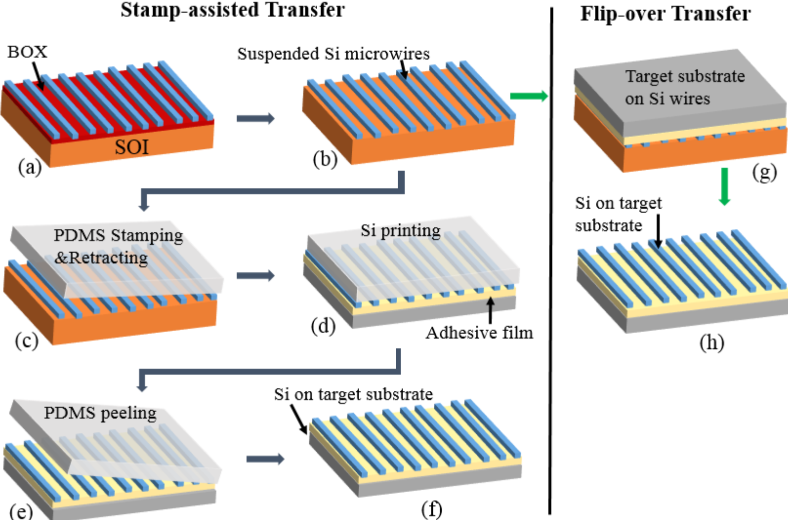

Figure. 5.1. Si wires on bulk wafer, (Left) stamp-assisted transfer printing (a). Si wires with buried oxide (BOX) (b). Suspended Si wires after etching BOX (c). PDMS stamping and retracting to pick Si wires (d) Stamping on adhesive layer on target substrate, (e) peeling-off PDMS stamp (f) Si wires transfer to target substrate. (Right) (g). Target substrate with adhesive side facing Si microwires and peeling-off (d) Si wires transfer to target substrate.

concentration. Whereas doping of the n-type wires is accomplished by implanting Phosphorous during the photolithography process. Besides these two separately fabricated microwires, alternately doped n and p-Si microwires on the same wafers are also fabricated in a second set of experiments. A slide mask is used to implant phosphorous at the alternate microwires. The alternately doped microwires are interesting to harvest the potentials of both types (n and p-Si) of microwires on a single flexible substrate. In addition to the stamp-assisted transfer, the flipped-over Si microwires are also characterized for the current-voltage (I-V) and optical response measurements. Fip-over is the type of dry transfer technique in which the Si microwires are directly transferred to the target substrate (PI tape for these) with adhesive side facing the microwires. After etching the buried oxide layer, the adhesive side of the PI tape is brought in conformal contact with the suspended microwires as shown in the Figure 5.1. As against the stamp-assisted transfer printing, flip-over transfer printing is more simple and a single step process. The main challenge involved with flip-over transfer printing is the availability of the bottom side of the Si for post-processing and device fabrication. As during the transfer printing, the top finished surface comes in direct contact with the adhesive layer, which is sacrificed during the transfer of wires to flexible substrate. For device configurations, only top-gated MISFET structures are possible to be fabricated with the flipped-over microwires, which also restricts their use for limited applications. In addition, the adhesive glue on the PI tape is not compatible with some of the chemicals used during the post-processing, which degrades the adhesion causing delamination of the Si microwires from the flexible substrates. Therefore, to investigate and confirm these claims, flipped-over n-and p-Si microwires are characterized and compared to the I-V and optical response of the stamp-assisted transfer printed Si microwires.

5.2.2. Silver-based Solution for Spray Coating

Solution-based conductive inks have been the main driving forces for advancement of printed and flexible electronics. The unique properties, these solutions exhibit before and after printing have made it more interesting to embark further into the field of flexible electronics. The conformable integration of conductive patterns and strong adhesion to nonconventional polymeric substrates after printing has given sufficient confidence to work with these materials. Amongst the list of available solution processable conductors with stable properties, silver (Ag) has emerged as the most promising in terms of synthesis, processing, robustness and more stability for longer time after curing on flexible substrates [14, 15]. Silver has been used in electronic devices since the birth of microelectronics and remains the most prominent material for diverse applications of nanotechnology. Several other metallic materials including both organic and inorganic have also been developed for conductive patterns such as copper, gold, platinum and tin [16-18]. Allotropes of carbon in the form of CNTs and graphene are considered as the most suitable conductors owing to their intrinsic mechanical

flexibility while possessing higher conductivities [8, 18]. However, developing stable solutions are needed with longer shelf life, which are more resistant to oxidation during pre and post-printing steps. Therefore, the easy and matured synthesis of stable solutions with tuneable properties have made the silver a preferred choice.

Silver paste (DuPont 5028) has been used for the conductive patterns in the MSM structures. The Ag paste is commonly used to develop low voltage circuitry, especially on flexible substrates. The composition is particularly suitable for applications requiring higher conductivities and fast curing. It can be used on fast speed roll-to-roll, semiautomatic and manual printers by offering prolonged residing time on the dispensers. The silver paste is primarily developed for screen-printing technology, which has higher viscosity in the range of 15-30 Pa. S as per supplier (DuPont) specifications. Inkjet and spray coating technologies required lower viscosities in the range of 0.001-.10 Pa. S as compared to viscosities desired for typical screen-printing, which is in the range of 0.50-5 Pa. S [17]. Therefore, to make the solution less viscous, a suitable thinner as recommended by the supplier i.e. DuPont 3610 is added to the paste in appropriate ratios to lower down to the level of desired inkjet/spray coating viscosities. A shadow mask is used for the patterned deposition through spray coating explained in more detail in forthcoming sections. Besides, spray coating a custom-made micro-spotting tool is also used to pattern the Ag paste (discussed in detail in chapter 6) and compared the processability with spray coating of Ag solution.

5.2.3. Patterning PEDOT-PSS by Spray Coating

The future of flexible electronics is foreseen to be having higher speeds and lower costs. The higher speeds come by introducing inorganic semiconductors into the stack of materials having intrinsic flexibility [19]. Processability of inorganic semiconductors such Si microwires and then transferring to secondary flexible substrates comes with higher costs. Therefore, to compensate the unavoidable higher costs of the Si microwires, choosing the cost-effective materials and fabrication techniques for the post-processes are the available alternatives to reduce the overall costs. Organic materials are solution-processable, inherently flexible and integrating these with inorganic semiconductors would lead to devices that are more economical in future. Less research has been reported for integration of organic conductors and inorganic semiconductor, therefore in this research we have studied the possible heterogeneous integration of dissimilar materials in the form of thin films. Among the list of available conductive polymers, poly(3,4-ethylene dioxthiophene) (PEDOT) doped with poly(styrene sulfonate) (PSS) is dominant for its distinguished mechanical and electrical properties [12, 20, 21].

PEDOT-PSS is transparent organic conductor in the visible range, have higher mechanical flexibility and excellent thermal stability [22]. PEDOT can be chemically polymerized in a poly(styrene sulfonic acid) (PSS) solution to give a PEDOT-PSS water emulsion. It results into a conjugated polymer with positively doped properties, where

the PSS are the counter ions used to balance the doping charges [23]. The transparent nature of PEDOT-PSS have played significant role in developing flexible optoelectronic devices [12, 20, 24]. These devices are mainly targeted for solar cells and energy applications utilizing also organic semiconductors or blend materials. However utilizing PEDOT-PSS as a conductive contact to Si microwires for the development of MSM and MISFETs structures would be step further towards more innovative devices. These structures would result in development of exciting applications as flexible photodetectors, mixers, strain cum optical sensors and flexible optical switches. PEDOT-PSS suffers from lower conductivities; however, research is in progress for exploring effective secondary doping to enhance the conductivity of PEDOT-PSS [22, 23]. The secondary dopant is apparently an "inert" substance, which further increases the conductivity of the primarily doped (with PSS) conjugated polymer [23]. It has been observed that conductivity of PEDOT-PSS can be enhanced by more than an order of magnitude by addition of polyalcohol's (alcohols with more than two OH groups on each molecule) [21, 22]. The possibility to enhance the conductivity of PEDOT-PSS compared to other polymeric conductors is a plus point to use it for high-end devices. Solution used for spray coating in these experiments was purchased form Sigma Aldrich (product no. 739332). A high-conductivity grade solution is prepared with a concentration of 1.1% in H_2O. Further specifications as per supplier include resistance <100 Ω/sq., < 80 % visible light transmission (40µm wet), refractive index n20/D 1.334, PH < 2.5, viscosity <100 cP (22 °C) and with a density of 0.999 g/mL at 25 °C.

5.2.4. Printing Experiments

The experimental details for fabrication of Si microwires and transferring them onto secondary polymeric substrates has already been discussed in previous chapters. Schematics of the stamp-assisted and flip-over transfer printing are shown in Figure 5.1 (a) and (b). Wires have been transferred to two different substrates i.e. Polyethylene terephthalate (PET) and PI. Choosing the two different substrates were based on motivation for exploring possible structures with the Si microwires. PET substrate is optically transparent and is the most feasible substrate for the stamp-assisted transfer. The receiving adhesive layer i.e. Su-8 in our case is UV-curable, which promotes the rapid transfer of Si from the stamp when brought in conformal contact to the receiver medium. The immediate curing of SU-8 when exposed to UV lamp from the backside of the substrates, the wires are transferred to the receiver layers along curing of the SU-8 layer. This completes the second transfer and the wires are ready for post-processing. In case of PI-tape, the adhesive part does not require any post-treatment and the wires are transferred just in one-step as shown in Figure 5.1 (b). Despite the simple processing, flip-over Si microwires have several drawbacks hindering their use for useful applications. The non-availability of the top-finished surface of Si device layer (of SOI wafer) is one of the major challenges. Additionally, it is impossible to pattern conductive contacts on the adhesive layer at the pre- and post-transfer stage. Processing

to pattern would deteriorate the adhesive layer ultimately affecting the microwires adhesion to the PI substrate. On the other hand, PET substrate is possible to be patterned before spin coating the SU-8 layer. Therefore, wires transferred to PET substrate have more attractions to be used for diverse applications. For instance, a back-gated structure is essential for using these microwires for sensor, where the top functionalized surface is available for direct interaction with the transducer materials. These back-gated structures are also interesting for optical related application such as UV and visible light detection (explored in this research), artificial photosynthesis and fuel cells etc.

Metal patterns were completed by using spray coating and micro-spotting tools. Spray coating is a direct writing technique where the solution is injected by a syringe pump, transported through a Teflon tubing and carried through the tip of a nozzle. Two types of spray configurations are practiced in microelectronics i.e. electrospray and aerospray. In electrospray, configuration of the system remains the same as aerospray except the nozzle types. The actuation mechanism of the electrospray is governed by application of a high electric field between the nozzle and a counter electrode. In this setup, an electric field is generated between the two electrodes to ionize the fluid in between. Positive potential is applied to the capillary nozzle while ground is applied to the conductive plate kept at a certain distance below the nozzle tip [25, 26]. Figure 5.2 shows schematics of nozzle configuration, nozzle setup and forces active during the spray process. Despite the capability to deposit, an ultrathin layer with minimum surface roughness, the complex system parameters and specific requirements of solution conductivities to get primarily a stable cone-jet in is more challenging. Additionally, the localized heating due to high electric field is undesirable for organic based materials as

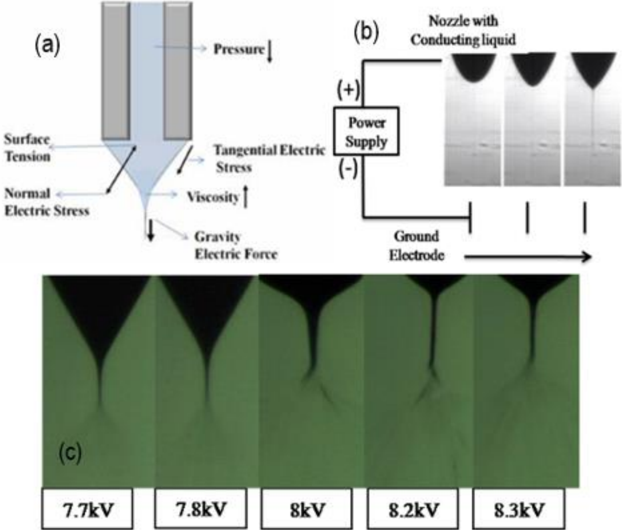

Figure 5.2. (a) Schematic of meniscus and affecting forces. (b) Meniscus shape after application of electric potential, (c) Meniscus behavior of electrospray upon increasing voltage [25, 26]

it promotes the nozzle clogging by immediate sintering of the materials in the nozzle. On the other hand, aerospray deposition is a good alternative having almost similar spray coating results but with more simplified operation.

A dual-concentric nozzle is used in aerospray deposition, where the internal nozzle is used to deliver the fluid while the external is used for air/N_2 flow to atomize the fluid into spray. Rheological properties of the solution are adjusted especially the viscosity to ease the spraying of the solution. Figure 5.3 shows schematics of the concentric nozzle and system setup for the aerospray coating developed in this research. A dual concentric (coaxial nozzle) purchased from NanoNC Korea is connected with the syringe pump (Harvard Apparatus, PHD 2000 Infusion) through a Teflon tubing. Syringe pump is used to control the flow rate. A higher flow rate i.e. 2000 ml/min is applied initially to flood the nozzle and then reduced to around 500 ml/min during the spraying process. A stable and continuous flow of fluid is essential for the uniform spray coated layer. A hot plate is used for the immediate evaporation of the surfactant used in the solution. For the silver solution, stage is heated at around 120 ^{o}C whereas for PEDOT-PSS the stage temperature is kept around 100 ^{o}C. The standoff between the nozzle and substrate is kept around 20 mm to cover the active area of the devices with the desired spraying material. For the patterned deposition, a shadow mask is used with two line openings. A rigid and high temperature resistant material is desired for the shadow masks to authenticate the firm attachment to the flexible substrate and Si microwires. Initially a 3D printed shadow masks (discussed in more detail in chapter 6&7) were used. These masks were prepared form stack of polymeric sheets glued to each other. They are ideal for solution, which does not need any heated stage (as in case of PMMA discussed in Chapter 7). However, for the metal deposition, these 3D printed shadow masks are challenging, as the stacked layers are unglued during the heating process and deteriorates the final structures. In addition, the firm attachment to the substrate and

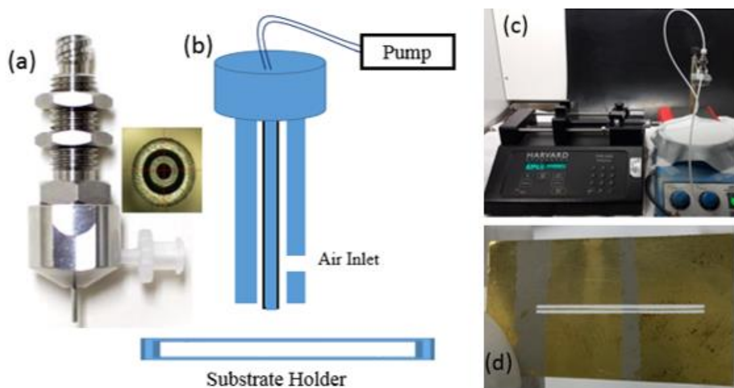

Figure 5.3. Optical images and schematics of (a). Dual concentric nozzle (Coaxial Nozzle, NanoNC, Korea). (b) Schematic of the cross-sectional view of the nozzle. (c) Spray system configuration with nozzle stand, heated substrate and a syringe pump. (d) Shadow mask prepared from brass by milling machine.

microwires is a serious issue and the solution undergoes through the elevated parts of the mask resulting into short-circuiting of the conductive contacts. Thin sheet of brass (50 um thick) is ideal for such applications that is rigid and can withstand higher temperatures at the same time as shown in Figure 5.3 (d). To make the fabrication of mask more robust, patterns are developed through a milling machine.

5.3. Results and Discussions

The Asymmetric metal semiconductor metal (MSM) structures were characterized in planar as well as bent orientations. The current-voltage (I-V) measurements were performed in ambient environment by probing both the metals contacts using semiconductor parameter analyser (4156C, Agilent) as shown in Figure 5.4. Current response of all the configuration of wires were analysed under similar conditions. Aim of these investigations is to compare the performance of both types of Si microwires independently on separate substrates and also on a similar substrate in the shape of alternately doped pn-Si microwires. Further investigation considered in this study are analysis of the two-step stamp-assisted transferred wires and flipped over transferred wires, which are accomplished just in one process step. Focus of these investigations is also on the junction characteristics of Ag and PEDOT-PSS with both types (n and p-Si) of microwires. Figure 5.4 shows images of the I-V measurements of the Si microwires in bent orientation. Here a simple setup is arranged to bend the microwires to a desired value by placing rectangular blocks at a distance of 15 mm apart on a planar thick acrylic sheet. Radius of curvature can be varied by changing the distance between rectangular blocks. With this configuration, we characterized the Si microwires in bend orientation and compared the values to the planar mode devices. Devices were checked lying in the centre where strain is effective at the centre of curve.

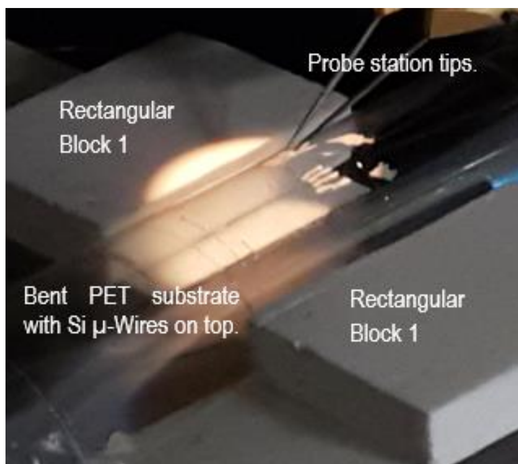

Figure 5.4. Current-voltage (I-V) measurements of Si microwires in bent (15mm diameter).

The MSM structures were also characterized under different illumination conditions. A Halogen lamp light with varying light intensity that is integrated to the microscope of the probe station is used to shine light from the top on the microwires. Whereas an ultra violet (UV) light source was used to investigate the current response of, the microwires compared to halogen light. The light intensity is varied for six different values ranging from 102 μW/cm^2-13.29 mW/cm^2. The UV-light source have a fix value so the lamp is kept at two distant positions to vary the intensity of light falling on the microwires. Intensity of UV-light at position 1 was 7.22 mW/cm^2 and 22 mW/cm^2 at position 2.

5.3.1. I-V Measurements of Planar MSM Structures

Devices were characterized based on the combination of differently doped Si microwire arrays. For the first combination of devices made of p and n doped Si wires on separate substrates and by making the metal contacts using Ag. Graphs in Figure 5.5 (a) and (b) show I-V measurements of the MSM devices in planar orientations. The highest current values of Ag/n-Si-Ag is observed to be 7.72 μA at a positive bias of 5V whereas maximum of - 12.8 μA at negative bias of -5V without any light illumination. Alternatively, the MSM structures made of Ag/p-Si/Ag have a highest current value of 0.14 μA for the positive biased voltage of 5.0 V and -0.73 μA for the negative bias of -5 V. The difference in the current response of the Si microwires is obvious owing to the differently doping types and concentrations as well. Doping concentration of n-Si microwires with Phosphorous (P) is about 1015 whereas p-type wires are moderately doped with Boron (B) i.e. 1012. Traps formed at the junction and the difference in the junction potentials between Ag with the n and p-type Si microwires are also responsible for the current response variations. The work function difference desired for the ideal schottky and ohmic contact are also playing role in variations of the current responses.

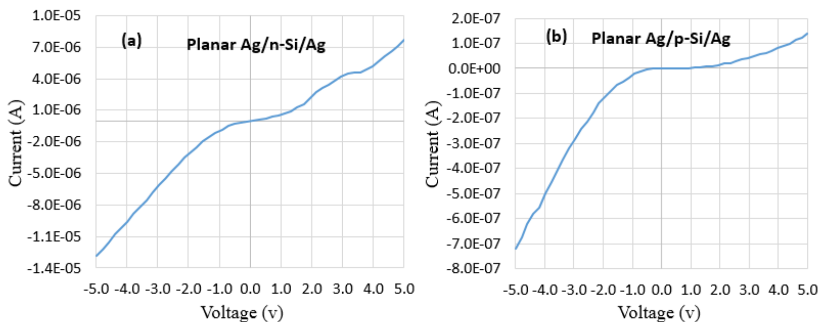

Figure 5.5. I-V measurement of the MSM structures by using Ag with n and p-Si microwires separately in planar mode.

Similarly, the devices were characterized made of PEDOT as a conducting contact to p and n-Si on separate substrates. The asymmetric MSM structure having PEDOT-PSS as the immediate conductive contact to the Si microwires and using silver paste as the

conductive pad for the probes is developed. Devices are characterized by putting probes on the silver spots instead directly contacting the PEDOT. After Spray coating of PEDOT-PSS, the patterned layers are sintered at 120 °C. To enhance the conductivity of PEDOT layers, ethanol was drop casted following the technique explored in [22]. The graphs in Figure 5.6 (a) and (b) show I-V curve for the PEDOT/n-Si/PEDOT and PEDOT/p-Si/PEDOT respectively in planar mode.

The current response is not very rapid for the hybrid junctions made between PEDOT/n-Si/PEDOT. PEDOT is usually used as hole injection material in optoelectronic devices where its metallic nature and transmittance in the visible range of light make it a good substitute for metals with no transmittance at all. An inversion layer is formed on the surface of n-type Si microwires as a result of large work function difference between the PEDOT (Φ_{PEDOT} 4.7-5.4 eV) and n-Si ($\Phi_{n\text{-}Si}$, ~3.85eV). Strong inversion occurs at the interface and the junction behaves more like a p-n junction diode [4, 27]. On the other hand PEDOT/p-Si/PEDOT shows very promising results due to the lower junction potential and minimal difference in the work functions of PEDOT (Φ_{PEDOT} 4.7-5.4 eV) and p-Si (Φ_{PEDOT} 4.95 eV). A moderate schottky junction at lower voltage and ohmic in the medium range is observed for the dark current measurement as shown in Figure 5.6 (b). Further, the current start to saturate at very low voltage, making the device ideal for low voltage thin film transistor applications. The current response in the saturation regime is in acceptable range for diverse transistor and switching applications in lightweight flexible electronics.

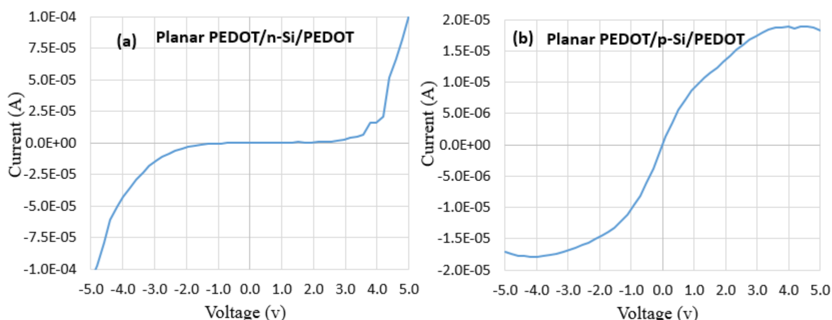

Figure 5.6. I-V measurement of the MSM structures by using PEDOT with n and p-Si microwires separately in planar mode

5.3.2. I-V Measurements of MSM in Bend Orientation

The similar MSM structures were characterized in the bend orientation and compared the values with the planar for possible changes in the resistance of the Si microwires as a result of tensile strain. Two rectangular blocks (as shown in Figure 5.4) were used at fixed positions using bi-adhesive tape and the plastic substrates were fixed between the edges of two blocks. The block were kept at 15 mm apart making a circular radius of around 7.5 mm at the centre, where maximum strain is to be observed in the microwires. The microwires were characterized in the convex position as shown in

Figure 4.4. Significant change in the resistance of the n-Si wires is observed as shown in Figure 5.7 (a) compared to the planar counterparts shown in Figure 5.5 (a). The maximum dark current response in the planar mode at positive bias of 5.0 V is 7.72 µA, whereas the same devices under bend conditions have a maximum current response of about 0.48 µA, which represents a significant increase in the resistance of Si microwires. On the other hand, the I-V curve for Ag/p-Si/Ag in bend mode experiences very less changes as shown in Figure 5.7 (b) compared to the I-V curve of the similar devices in planar mode shown in Figure 5.5 (b). The lower doping concentration of p-Si might be one of the reason for these less variations compared to the prominent variations in the heavily doped n-Si microwires. Another reason for the less variations is due to the non-uniform spacing between the metallic contacts. Deviations in the spacing could also lead to the variations in the response of microwires, as the wires with increased spacings would be subjected to more strain compared to closely spaced conductive patterns. The closely spaced metal patterns act as a supporting layer to prevent the Si microwires from undergoing any strain. This needs further investigation and in order to harvest the strain response of the Si microwires, spacing between the metal contacts need to increase.

Figure 5.8 (a) and (b) show I-V curves of the PEDOT/n-Si/PEDOT and PEDOT/p-

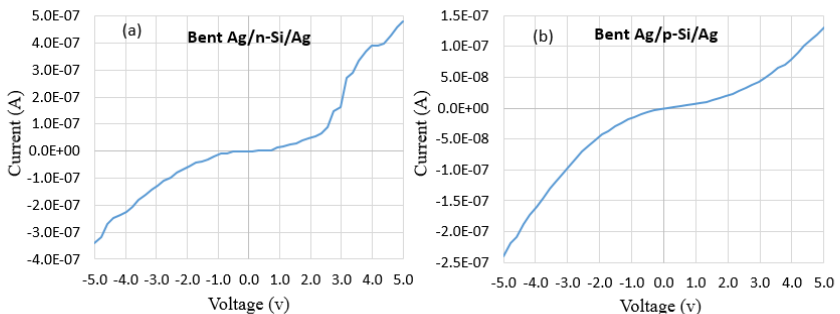

Figure 5.7. I-V measurement of the MSM structures by using Ag with n and p-Si microwires separately in bent orientation.

Si/PEDOT respectively in bend mode. In this case, significant variations were observed for both the devices compared to the current values in planar mode. For the PEDOT/n-Si/PEDOT, the dark current reduces from 101.0 µA (Figure 5.6 (a)) to 7.6 µA (Figure 5.8 (a)) for the positive biased of 5.0 V. The current response for the PEDOT/p-Si/PEDOT have less variations in the bend mode against planar. The dark current reduces from 18.3 µA (Figure 5.6 (b)) to 2.33 µA (Figure 5.8 (b)) in the bend mode, which is again due to the less doping concentration of the p-Si. All these variations in the current response in planar and bend mode of the MSM structures lead to interesting applications of using Si microwires as strain sensors [9, 10]. The slight changes in the orientation either convex or concave have a strong bearing on the current response of

the microwires, which could successfully be utilized as a strain sensor. These type of devices are attractive for applications such as prosthetic limbs and synthetic or electronic skin (e-skin) for robots where various dexterous manipulation tasks are monitored. Such type of sensors, if installed at the finger joints either on the back or on front side where the change in resistance due to convex or concave bending respectively would help in performing the manipulative tasks successfully. Strain sensors developed with Si microwires are more stable and reliable compared to sensors developed from organic based materials. The Si microwires based sensors are more responsive, repeatable and have longer life if properly encapsulated to prevent to harsh environments.

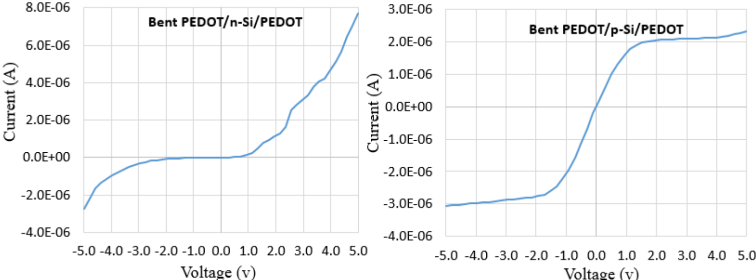

Figure 5.8. I-V measurement of the MSM structures by using PEDOT with n and p-Si microwires separately in bent orientation.

5.3.3. Photodetection and Optical Switching of the MSM

Photodetectors and especially UV photoswitches have emerged as vital components for a wide range of commercial applications including biological and chemical analysis, flame monitoring, missile detection, secure space communication and astronomical studies [2]. The Si microwires play a greater role in visible and UV phot detection owing to their high surface-to-volume ratio. The high responsivity and photodetection

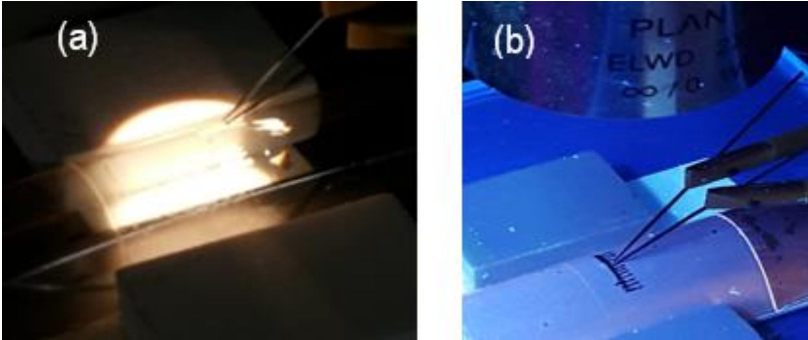

Figure 5.9. Current-voltage (I-V) measurements of Si microwires in bent (15mm diameter) (a). I-V under halogen lamp with varying intensities and (b) under UV- light.

gain has been traditionally found in the low-dimensional wide band-gap materials such as GaN, ZnO, TiO_2 and several metal-oxide bandgap nanostructures [28, 29]. However the high sensitivity to ambient environment such as temperature and humidity making these devices more prone to signal fluctuations and poor selectivity. These devices are less durable and have a short life in such variable and harsh environments [2, 29]. Additionally, the major challenge with the wide band-gap materials is their reliable integration onto flexible substrates. Therefore, to overcome these issues, Si μ-wires have been investigated as alternative to detect broad spectrum in visible and UV range.

The MSM structures were characterized for the optical response with different illuminations as shown in Figure 5.9. Halogen lamp with a broad spectrum of visible light was used with variable light intensity. The wires were illuminated with 6 different values of the light intensity and corresponding change in the current response was measured. The minimum light intensity was 102 μW/cm^2 and maximum as 13.29 mW/cm^2. In the second type of illumination, a UV light source is used at two different intensities. As the UV light generates a fixed value of light intensity without any control

Table 5.1. Intensities of the light sources

Halogen Lamp	**Intensity (mW/cm^2)**
Photo 1	0.12
Photo 2	0.407
Photo 3	1.417
Photo 4	2.91
Photo 5	6.85
Photo 6	13.29
UV Lamp	
Photo UV 1	7.22
Photo UV 2	22.0

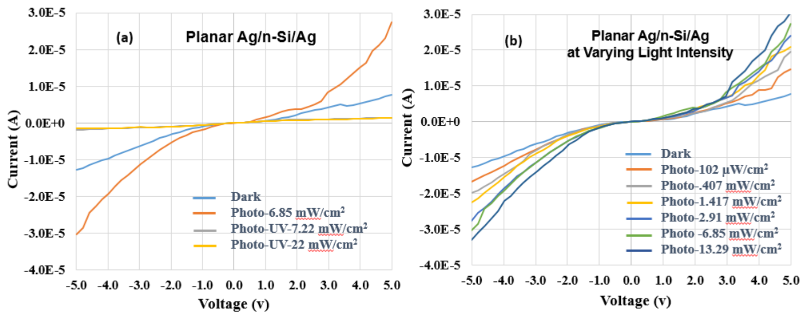

Figure. 5.10. I-V measurement of the MSM structures by using Ag with n-Si microwires separately in planar mode under (a) Light illumination of halogen and UV, (b). Current response to increasing halogen light intensity

knob to tune the intensity. Therefore, the UV lamp is kept at two different locations from the Si microwires where the light intensity was calibrated to two corresponding values. The light intensities were monitored by using an optical meter. The halogen light is integrated with the microscope of the probe station and the light source was right on top of Si microwires. Whereas in case of UV light, the lamp was kept on the side facing directly at an angle (~45°) to the Si microwires. All the light intensities are summarized in Table 5.1.

The MSM devices based on Ag contact with both n and p-Si were characterized under illumination conditions in planar mode in similar method described in previous section (5.3.2). Graphs in Figure 5.10 (a) and (b) show comparison of current responses of n-Si microwires with light illumination of UV and halogen lamp respectively. The dark current in the graphs of Figure 5.10 (a) is compared to the halogen light at photo 5 intensity i.e. 6.85 mW/cm^2 and both the values of UV lamp. Whereas devices were characterized for a varying intensity of halogen lamp ranging from photo 1 to photo 5 as shown in Figure 5.10 (b).

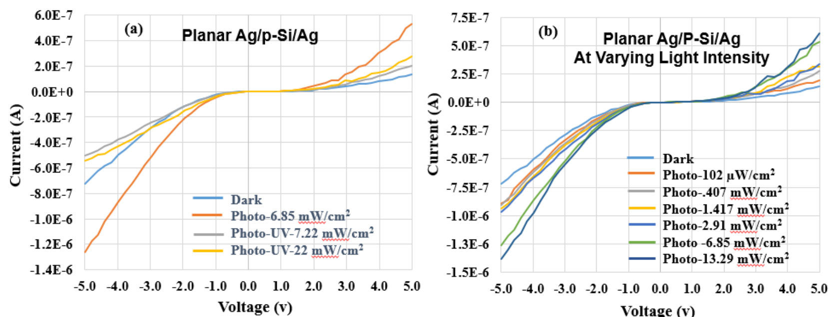

Figure 5.11. I-V measurement of the MSM structures by using Ag with p-Si microwires separately in planar mode under (a) Light illumination of halogen and UV, (b). Current response to increasing halogen light intensity

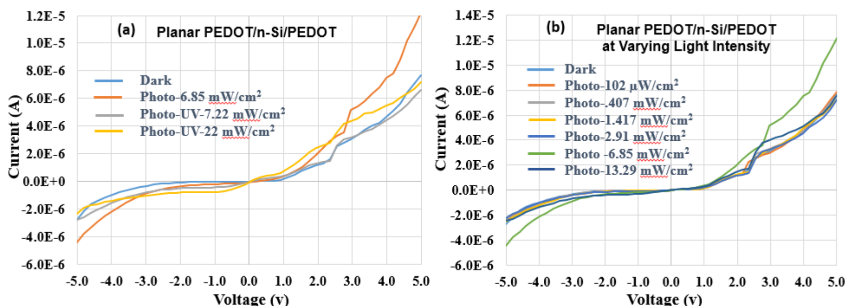

Figure 5.12. I-V measurement of the MSM structures by using PEDOT with n-Si microwires separately in planar mode under (a) Light illumination of halogen and UV (b). Current response to increasing halogen light intensity.

Both the Ag/Si/Ag structures are observed to be more responsive under exposure to the halogen lamp even with lower intensity (6.85 mW/cm^2) than the one with maximum UV-light (i.e. 22 mW/cm^2). The maximum change observed with the light illumination is 27.4 µA, three times higher than the peak value of dark current at the positive bias of 5.0 V. On the negative bias side increase in the current values by more than two order of magnitude i.e. 30.4 µA is observed as compared to 12.8 µA of the peak dark current at -5.0 V. On the contrary, not much change is observed with UV illumination of the n-type microwires. The I-V curves in Figure 5.11 (a) and (b) show response of p-Si microwires, which are observed to be responsive to both the illuminations and increase in current responses are observed as compared to the dark current values. The response is significant again for the halogen light especially on the negative bias where more than one order of magnitude increase in the peak dark current value is observed. However, the UV response is negligible and have adverse effect on current in the negative bias.

Devices made of PEDOT/Si/PEDOT have very exciting results in response to light illumination owing to the junction modification between PEDOT and Si microwires. The transmission window in the visible range of PEDOT allows the light to directly interact at the interface and hence increase the number of charge carrier. This has been observed from the experimental values of current gain during the I-V measurements. Figure 5.12 (a) and (b) shows current gains in at different lighting conditions. Again, the junction between p-type PEDOT and n-Si make an inversion layer at the Si surface by depleting all the majority charges (discussed in section 5.3.1). The moderate schottky-ohmic behaviour is dominant (Figure 5.12 (a)) behaving more like a pn-junction diode. The current response is lower at lower biasing values and increases abruptly after certain threshold. The current does not saturate and goes on increasing by increasing the biasing voltage. The switching window is very small by increasing intensity of the halogen lamp. The strong optical switching behaviour is shown by the PEDOT/p-Si/PEDOT structures, where the photo current is increased by few order of magnitudes as shown in Figure 5.13 (a) and (b). As against the previous devices (PEDOT/p-Si/PEDOT), here the UV response of the current is higher in both the positive and

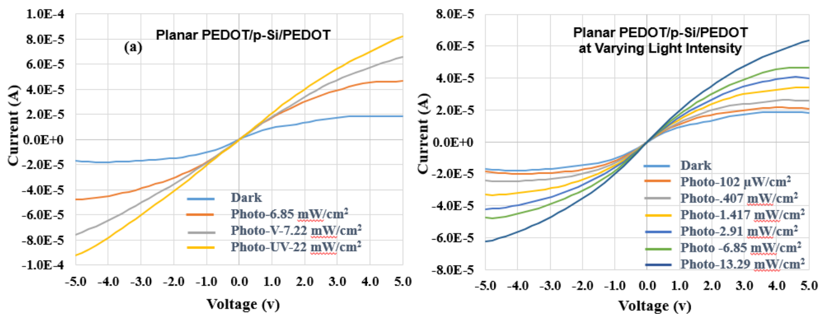

Figure 5.13. I-V measurement of the MSM structures by using PEDOT with p-Si microwires separately in planar mode under (a) Light illumination of halogen and UV (b). Current response to increasing halogen light intensity.

negative biasing conditions. The junction is moderately modified from schottky like junction towards more ohmic with the gradual increase of the light illumination shown in Figure 5.13 (b). The photocurrent gain (46.5 µA) increases by an amount of 28.2 µA compared to the dark current (18.3 µA). Similar trend of current enhancement is observed on the negative bias as well. The peak current values increase approximately by four orders of magnitude by illuminating the Si microwires with UV-light at higher light intensity i.e. 22 mW/cm^2.

Real-time switching behaviour of the PEDOT/Si/PEDOT was also investigated, where a lower biasing voltage i.e. 0.5 V was applied to the MSM structures and the light is switched on and off during the biasing conditions. The switching behaviour is evident from the Figure 5.14 (a) and (b), where halogen and UV lights are illuminated respectively on a PEDOT/n-Si/PEDOT structure. Both the graphs show an increasing value of the current with increased biasing, however by turning off the light an immediate loss in the current value is observed as shown in Figure 5.14 (a & b). A significant variation in the current values is detected light on and light-off conditions. For instance, at biasing voltage of 0.5 V is The peak current value for light-on is 11.5

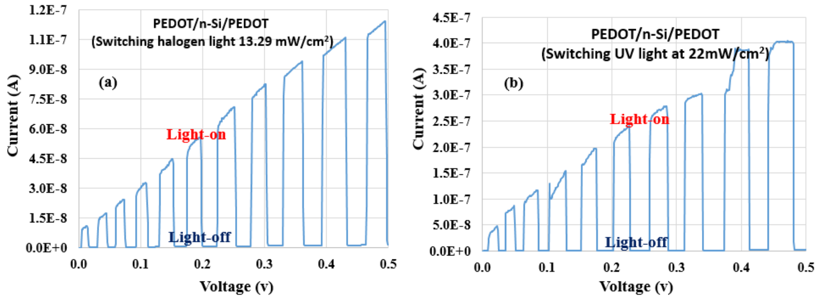

Figure 5.14. I-V response and switching behavior of the MSM structures using PEDOT with n-Si microwires separately (a) Light illumination of halogen (b) UV light.

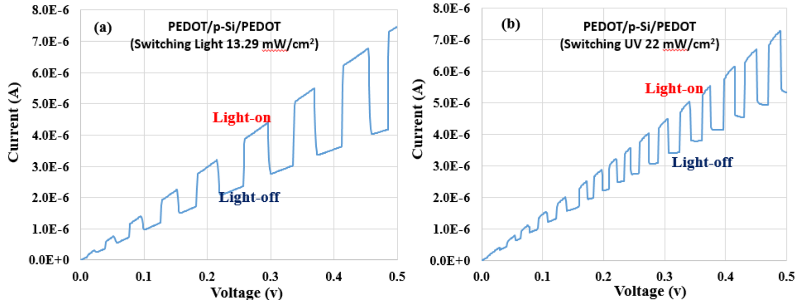

Figure 5.15. I-V response and switching behavior of the MSM structures using PEDOT with p-Si microwires separately (a) Light illumination of halogen (b) UV light.

μA, whereas a the current value drops to 1.5 nA with the light-off. The trend of change in the current values is same at each value of the biasing voltage.

This huge difference in the current gain just by turning-on and off the illuminating light is a very promising result for development of an optical switch as well as photodetection. An enhanced optical current response is observed for the UV light compared to the halogen lamp. An increased current value of 40.2 μA is detected at biasing voltage of 0.5 V with the light on and drops to 2.3 nA with UV light off. The increase in current gain with UV light-on i.e. 28.7 μA compared to halogen light-on at similar biasing voltages (0.5 V) confirms the superior performance of the optical switch for UV light with a wider operating and switching window. Figure 5.15 (a) and (b) show graphs of switching behaviour of a PEDOT/p-Si/PEDOT structure. The switching current window is small in case of p-Si due to the less charge carrier concentrations compared to the heavily doped n-Si (doping concentration is 1015). The variations in the photocurrent and dark current is very small for both the types of illuminations. In order to make the switching window wider, a higher doping concentration is desired.

5.4. I-V of Flipped-Over Si Microwires

Flip-over transfer printing is a one-step process for an easy and simple transfer of Si microstructures from the donor wafer onto secondary flexible substrates as shown in Figure 5.1 (b). All the devices discussed in previous sections were translated to flexible substrates using a PDMS-stamp, which involves a two-step transfer process. Wires are picked-up by weak Van der Waals forces from the donor wafer by the PDMS stamp. A very planar stamp is desired for such transfer process and a high active surface area of contact between the wires and stamp. Serious risk involved in this process is some wires cannot be detached from the tethered points and remain attached to the wafer. However, this could be avoided by over-etching (developed within this research) by completely removing the buried oxide. The over-etching approach is more effective for wires with wider dimension such as 30-40 μm widths or more. Wires with lower widths i.e. less than 20 μm are difficult to control as the wires are detached from the anchored positions after completing the etching of buried oxide. Additionally cleaning steps such as with deionized water to remove the etchants (BHF), wires can detach during this and the subsequent handling steps. Therefore, under-etching is desired for the type of structures having higher resolutions both in width and in thickness. In such scenario, a flip-over transfer, where the flexible substrates have one side adhesive such as scotch tapes. Here the interface of stronger adhesive layers and the under-etched microstructures is stronger and the wires could easily be transferred onto the target substrates.

To validate these observations, experiments were performed using a Polyimide (PI) scotch tape. The PI tape was fixed on a glass slide, the adhesive side facing upwards. After etching the Si microwires (30μm wide) and the cleaning steps, the glass slide is kept on top of the donor wafer and removed back directly. Transfer yield in this approach is 100 % as all the microwires were transferred onto the PI tape. Despite the

higher transfer yield, this procedure has serious challenges of the pre and post processing for the substrate as well as for the microwires. No patterning or metallization is possible before transfer, to realize for instance a back-gated FET. With metallization, the adhesive layer of the PI tape will be sacrificed; therefore, only top metallization after the transfer step is possible in this process. Additionally, the adhesive part of the substrate is not compatible with most of the cleaning solvents (i.e. acetone or ethanol required for removal of the PSS layer after deposition of the PEDOTT-PSS for conductive contacts) making the process more challenging. The most serious challenge is for the metal contacts, as backside of the Si device layer is available for the post-processing, therefore getting an ohmic behaviour at the junctions is very challenging. This is less critical for the structures requiring single type of doping (like MSM) structures; however, for complex devices such as transistors, different doping sections are desired within a single structure. Experimental investigation has been carried out to compare the current response and the junction behaviour of the flipped-over Si microwires to that of stamp-assisted transfer printed microwires in this section. The MSM structures from the flipped-over microwires have been developed with the similar

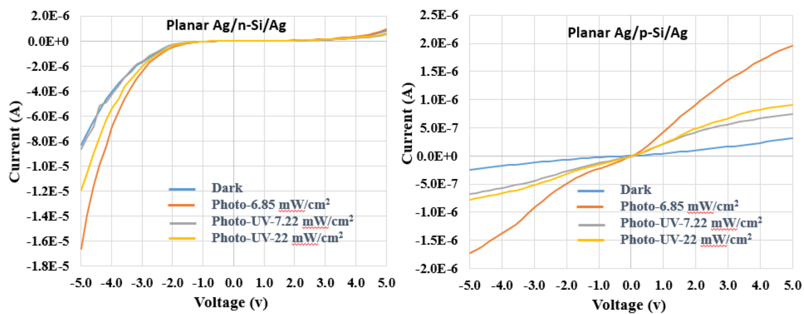

Figure. 5.16. I-V measurement of the MSM structures by using Ag with n and p-Si microwires separately in planar mode under. Characterized also for light illumination of halogen and UV.

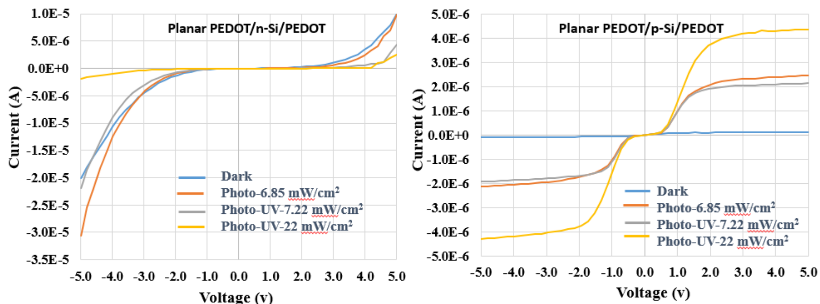

Figure 5.17. I-V measurement of the MSM structures by using PEDOT with n and p-Si microwires separately in planar mode under. Characterized also for light illumination of halogen and UV.

procedure as followed for the stamp-assisted microwires. The I-V measurements for the Ag/n-Si/Ag and Ag/p-Si/Ag are given in Figures 5.16 & 5.17 respectively. Comparing the results with graphs in Figure 5.10 & 5.11 (a), the schottky behaviour is dominant with the flipped-over wires. The current responses at the higher biasing voltages are in close ranges for the n-Si wires. Thickness of the n-Si is lower (500 nm) than the p-Si (2.5μm) and therefore the doping concentration is uniform on both the side. The variations in the junction contacts is due to the increased traps and residual oxide, affecting the ohmic behaviour even under illuminations. Comparing the results of Figure 5.17 with that of the corresponding devices in Figures 5.12 & 5.13 (a), the major deviations in the current response as well as the junction behaviour is observed. The current drops by 7.5 μA in the PEDOT/n-Si/PEDOT structure along with a strong schottky junction. A lower current response i.e. 0.12 μA is experienced with the PEDOT/p-Si/PEDOT with the flipped over microwires as compared to the 18.3 μA with the stamp assisted transferred microwires. The junction does not change for higher illuminations despite the lower difference in the work functions of PEDOT and p-Si and transmission window of the PEDOT to the visible light. Table 5.2 summarizes all the peak currents of the corresponding MSM devices in planar mode. It is evident form the current responses that flip-over currents are lower compared to the dark as well photocurrent of the stamp-assisted transferred Si microwires. Additionally the provision to pre-process the substrate for the back contacts and availability of the finished top Si device surface for post-processing make the stamp-assisted transfer printed microwires more interesting. The large window of optical switching, higher value of photocurrent and junction modification from schottky to ohmic junction under illumination make PEDOT/p-Si/PEDOT more interesting for practical applications as in flexible electronic systems.

5.5. Alternately Doped pn-Si Microwires

Alternately doped pn-Si are arrays of microwires comprising both types of Si (p and n) on a similar substrate. A slide mask is used to develop such type of wires, where the alternate wires are doped with new type of dopants. Phosphorous is implanted as an alternate n-type wire on the already p-doped SOI wafer. Such type of devices are very interesting to be investigated as they have the potential to be utilized for diverse applications in flexible electronics. Few of the potential applications of alternately doped pn-Si microwires is the development of flexible thermoelectric generators and solar fuel cells. Thermoelectric generators work on the principle of seebeck effect where two differently doped semiconductors are connected on the edges to generate potential by a thermal gradient. Large arrays of Si microwires (20 wires each array) are more effective compared to few wires or structures. The thin and lightweight thermoelectric generators would revolutionize the low voltage self-powered microdevices. Another interesting application of the alternately doped Si microwires is its utilization for developing a flexible CMOS circuit. This is one of the most demanding area for

advancing the discrete flexible devices to integrated circuits. Not much research has been carried out until now, and the area of research for CMOS is still underdeveloped. Alternately, doped pn-Si microwires are interesting for recently developed phenomenon i.e. artificial photosynthesis and solar fuel cells on planar substrates.

To explore the potentials of alternately doped pn-Si microwires on flexible substrates, prototype devices such as asymmetric MSM structures and thermoelectric generators (TEG) are demonstrated. The MSM structures are characterized for the optical illumination of the visible and UV light. They have potential applications to be used as optical sensors and photodetectors. Connecting an array of alternately, doped pn-Si microwires through transparent organic conductor such as PEDOT-PSS have good IV response, making them attractive for a range of optoelectronic devices. The prototype MSM devices have been developed, which is a step further towards successful fabrication of energy harvesting on planar flexible substrates. Additionally, development of a flexible thermoelectric energy harvester by using transfer printed doped Silicon (Si) microwires is also covered in this section. The TEG module, consisting of an array of alternately doped p-type and n-type Si microwires, is

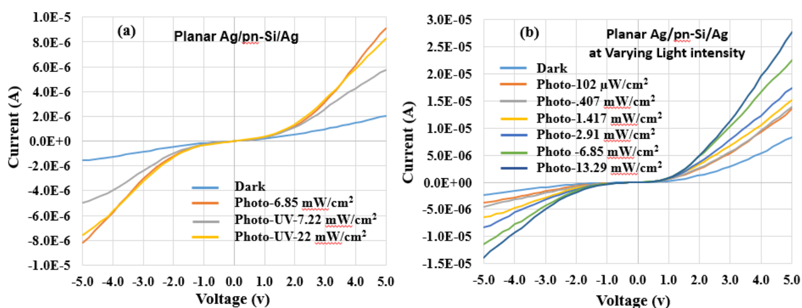

Figure 5.18. I-V measurement of the MSM structures by using Ag with alternately doped pn-Si microwires separately in planar mode under (a) Current response to light illumination of halogen and UV, (b). Current response to increasing halogen light intensity

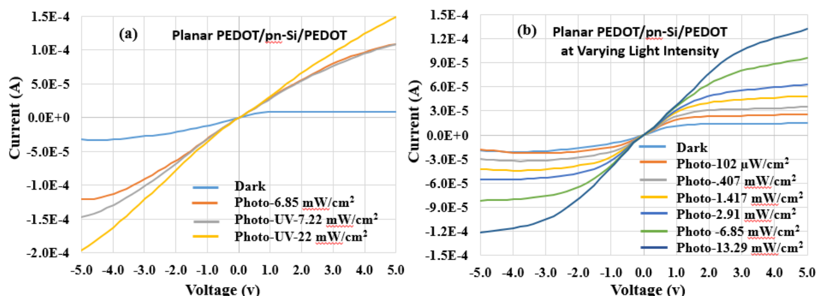

Figure 5.19. I-V measurement of the MSM structures by using PEDOT with alternately doped pn-Si microwires separately in planar mode under (a) Current response to light illumination of halogen and UV, (b). Current response to increasing halogen light intensity

developed on a SOI wafer using standard photolithography and etching techniques. The Si wires in the TEG module are 5mm long, 50µm wide, and the spacing between two adjacent wires is 50µm. The TEG modules are transferred from SOI wafer to Poly (ethylene terephthalate) (PET) substrate by using transfer-printing method, with Polydimethylsiloxane (PDMS) as transfer substrate. More than 90% of wires are transferred in the first transfer step (i.e. from wafer to PDMS) and 100% are transferred in the second step (i.e. PDMS to PET) has been achieved in this process. A maximum of 9.3mV open circuit voltage was recorded from the flexible micro TEG (µTEG) prototype with a temperature difference of 54 ^{o}C at two ends of the wires. Following sub-section provides details about the I-V measurements and thermoelectric response of the alternately doped wires.

5.5.1. I-V of Alternately Dope pn-Si Microwires

An asymmetric MSM structure is developed in the same manner as used for the single type doped wires. Similar steps of stamp-assisted transfer printing and metallization are followed. Figures 5.18 and 5.19 show graphs of the I-V measurements of the MSM structure mage with AG/pn-Si/Ag and PEDOT/pn-Si/PEDOT respectively. The current response in dark as well varying illumination intensities show very interesting and uniform behaviour compared to the separately doped Si microwires. The oppositely doped neighbouring microwire compensates the lower current response of the unfavourable junctions due to work function mismatches. Again, the UV-photocurrent is dominant for the PEDOT/pn-Si/PEDOT, making it a reliable optical switch. The junctions remain moderately schottky even with the illumination in the Ag/pn-Si/Ag structures (Figure 5.18 (a) and (b)) similar to the separately doped n-Si microwires connected with Ag. On the other hand, the PEDOT/pn-Si/PEDOT shows an immediate transition from schottky to an ohmic behaviour upon illumination of both types of light sources as shown in Figure 5.19 (a) and (b). This is the major variation observed within all the MSM structures characterized using separately doped and alternately doped Si microwires. Response of the alternately doped microwires is lower in the dark current compared to the single doped n and p-Si microwires junctioned with Ag and PEDOT. For the Ag/n-Si/Ag the peak dark current at 5.0 V is 7.22 µA 3.2 µA higher than the peak dark current of the of the alternately doped microwires. Similar case is with the PEDOT/n-Si/PEDOT where the peak dark current at 5.0 V is 7.6 µA and 18.3 µA for the PEDOT/p-Si/PEDOT structure, which is two times higher than the dark current of the PEDOT/pn-Si/PEDOT. On the contrary, a significant increase in the photocurrent of the PEDOT/pn-Si/PEDOT is observed where the dark current changes from 9.0 µA to 15 mA with UV light illumination. This property adds to the exciting applications foreseen for the alternately doped microwires where the high photocurrent gain and switching current window would lead to its reliable application for optical switches and fuel cell for self-powered autonomous flexible microsystems.

5.6. Thermoelectric Generators with alternately doped wires

5.6.1. TEG Background

The demand for self-powered or autonomous electronic systems in applications such as wearable electronics, body sensor networks and implantable devices has attracted an increased attention on the energy harvesting devices and systems. Harvesting energy from environment to power, a nano/microdevice is feasible and of vital importance to self-powered nano/microsystems [30-32]. The self-powered systems require their own power supply, which in most cases are the conventional electrochemical batteries having a limited lifetime. The task of replacing batteries is tedious and can become very expensive and risky especially in case of implantable devices. Such issues can be alleviated, if not prevented altogether, by developing the energy harvesting devices and scavenge the energy from the environment. The ambient energy source, which has received a great attention in the recent years, especially for applications such as wearable electronics, is the thermoelectric energy harvesting. Traditionally, thermoelectric generators (TEG) are energy harvesting devices made of all solid-state materials on rigid substrates that convert heat into useful electricity. Thermoelectric generators are different from dynamic heat engines, as they contain no moving parts and are completely silent [33]. Despite the lower efficiencies compared to dynamic heat engines, attractive features such as small, inexpensive and scalable have made the TEGs attractive energy harvesters for microsystems [33-35]. The increasing interest in developing thermoelectric energy harvesters is driven by the increased demand of long lasting operations of micro systems by utilizing heat energy from environment or heat emitted during system operation. The power consumption of nano/microdevices is usually in the range of micro to milliwatt [30, 35].

The flexibility or bendability of thermoelectric harvesters is a plus that improves their utility. For example, a flexible TEG can conform to body surfaces. Portable, personal and wearable self-powered nano/micro systems require the thermoelectric materials to be flexible and lightweight. Flexible thermoelectric generators deployed also on nonplanar surfaces are important for autonomous electronic systems due to the advantages of lightweight, portability, bendable, stretchable, large areas and more resistant to impact. For this reason, flexible thermoelectric energy harvesters are of great interest in variety of miniaturized wearable and distributed microsystems [36, 37]. Different materials, structural designs and fabrication techniques have been practiced for developing flexible micro thermoelectric generators (μTEG) [36, 38]. Thermoelectric material has been reported to be critically important as it has the major influence on performance of a μTEG. The Bi2Te3 and its alloys are commonly used thermoelectric materials [36]. The scaling down of bulk Bi2Te3 to harness energy conversions on larger areas is a challenge [39]. Fabricating synthetic micro/nanostructures of these materials for energy purposes is even more difficult and also expensive. In this regard, the semiconductor materials such as Si are ideal candidates for such type of devices. The suitability of Si is strengthened by its natural

abundance and wide usage in electronics, with a large industrial infrastructure for low-cost and high-yield processing. However, bulk Si have high thermal conductance, which is potentially an unwanted parameter for µTEGs. Due to this reason downsizing of bulk, Si to microwires has been investigated extensively on wafers scale [32, 39].

Most of the reported TEGs based on Si are vertically grown nanowires on wafers, which restricts their deployment on flexible substrates with proper orientation of the doped wires. In addition, integration of such structures for increased number of thermocouples for enhancing efficiency is challenging. A different approach for developing flexible µ-TEG on flexible substrates such as PET (poly(ethylene terephthalate)) is investigated here by using alternately doped Si microwires. The Si microwires were developed on SOI wafer and then successfully transferred to PET substrate by using PDMS stamp as an intermediate transfer substrate. A stamp-assisted transfer (similar transfer method discussed in section 5.2) method was selected also for the TEG devices. A slide mask is used to deposit alternate doping material on the already doped (p-type) SOI wafers. Thermoelectric structure has been completed by using a micro spotting technique for metallization after transferring microwires to flexible substrate. Sample devices were characterized at different temperature gradients and open circuit voltage was found to be in close approximation to state of the art device [32, 36]. To our knowledge, this is in one of the pioneering prototype devices, developed by using stamp-assisted transfer printing of alternately doped Si microwires onto flexible substrates.

5.6.2. Planar thermoelectric generator

A thermoelectric (TE) cell (or thermocouple) consists of two dissimilar conductors, often p-type and n-type doped semiconductors, connected at one end at the junction as shown in Figure 5.20 (a). The first TE effect, known as the Seebeck effect, occurs when the junction is heated while the other side is kept cool, so as to create a temperature difference across the thermocouple as shown in Figure 5.20 (b). The resulting ΔT generates an electromotive force (or voltage) along the TE materials [30, 36]. Figure 5.20 (a) shows schematic of two doped wires connected in series in which a heat difference at both the ends results in an electric current generation passing from n to p side of the couple. Figure 5.20 (b) shows a complete prototype of thermoelectric generator in which individual microwires are connected in series.

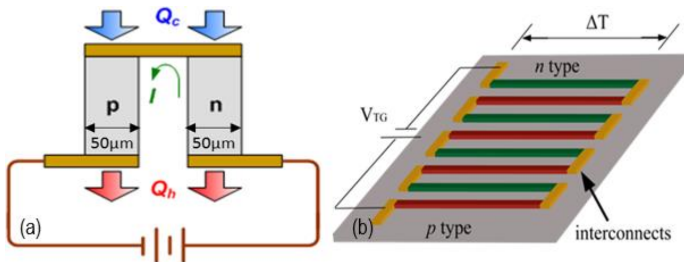

Figure 5.20. (a) Scheme of a thermocouple cell (b) Concept of a TEG module.

Top down approach for Si microwires is the most reliable and practiced technique in order to get uniform dimensions. Microwires are obtained by using standard photolithography technique with good control over geometric parameters like thickness, widths and lengths of the microwires. Better uniformity in geometry and thickness is essential for TEG applications, which could be easily achieved by using SOI wafers as against by bulk wafers. The similar geometry in turn contribute to the better and uniform response of the devices. Total of 34 microwires are fabricated for an increased number of therocells in a complete thermoelectric module. Spacing between the microwires are important to be adjusted and are defined by standard photolithography followed by deep reactive ion etching to produce trenches [40] among consecutive microwires. Si microwires in dimensions of 50μm wide and 5000 μm are developed. Alternate doping of p and n microwires are achieved by using a slide mask. In order to transfer these microwires onto an alien substrate, buried oxide layer has to be removed initially. Before putting the samples for etching the buried oxide layer, samples were put in piranha solution for 10 minutes to remove away any organic residue, which hinders the etching of oxide. In the next step, the samples were put in buffered hydrofluoric 40% (with etch rate of 13 min/1 μm) concentrated solution for a specific duration such that the oxide layer was etched away completely while remain anchored at the ends. In order to make the wires completely releasable from the donor wafer samples were retained in the etchant solution for an extra 10 minutes. After etching, deionized water was poured into the container so as not to disturb the attachment of microwires with the mother wafer.

Metallization of the transferred microwires on PET substrate is done by custom micro spotting technique. Silver (Ag) paste is used to connect wires in series by using a micro needle with 10μm tip. Small drops of Ag paste are used to connect two consecutive

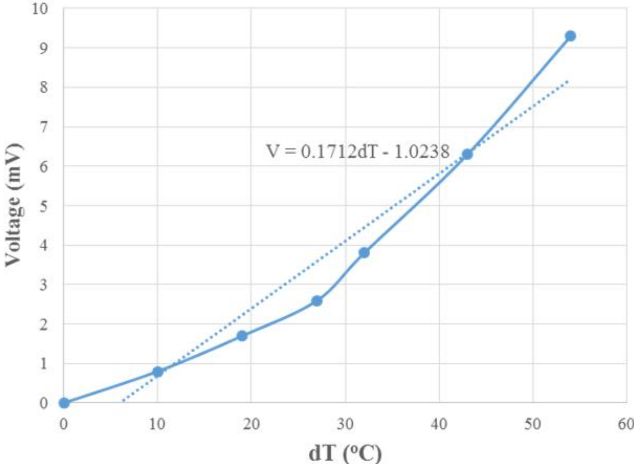

Figure. 5.21. Graph of open circuit voltage at different temperature gradients.

microwires. After completing the metallization of wires and pads at the ends, samples were put in furnace for 30 minutes at 120 °C. As a planar device was developed in this research, open circuit voltage was measured by putting the sample on two plates having different temperatures and placed 2 mm apart. Temperature of one of the plates is raised while that of the other is kept constant at room temperature. Samples were mounted on the plate at room temperature and brought near to the hot plate for a while and open circuit voltage was measured. After measuring the voltage, the sample is removed from the vicinity of the hot plate and temperature increased. Length of the wires (i.e. 5mm) is supportive in above configuration of putting the device on two separate plates. The open circuit voltage was measured by using high impedance Keithley 7410 voltmeter at gradually increased temperatures. Figure 5.21 shows graph of the measured voltage at different temperature gradients. Maximum open circuit voltage was measured to be about 9.3 mV for a temperature difference of 54 °C, which is a comparable value to state of the art devices i.e. [32, 36].

5.7. Conclusion

This chapter presented a comparative study of various configurations of asymmetric metal semiconductor metal structures. The two differently doped p and n-Si microwires were prepared by standard photolithography and etching techniques. Two different transfer printing approached were followed to complete the relocation of microwires onto secondary flexible substrates. A stamp-assisted and flip-over transfer printing approached are practiced to complete the transfer. A planar PDMS stamp is used to pick and place Si microwires deterministically at desired locations on secondary substrates. Alternately, the flip-over technique is completed by using the target substrate with one side adhesive to pick the microwires. The metallization is completed by developing a spray coating setup for deposition of two different conductors. A colloidal solution of Ag based paste and an organic conductor i.e. PEDOT-PSS is spray coated by using shadow masks. Ultra-thin brass sheets are used to prepare the shadow masks using milling machine. The MSM structures are characterized both in planar and bent orientations to investigate the strain response of the microwires. Additionally the MSM structures are subjected to optical illumination from two different light sources, i.e. Halogen and UV lamps. The optical response of wires is investigated in both planar and bent modes and compared with the dark current response of the wires in both the orientations. Similar characterization steps were performed for flip-over and stamp assisted Si microwires. Additionally a top-down approach of doped Si microwires on SOI wafer is presented and transferring them to PET substrate for realizing lightweight and robust flexible thermoelectric generators. Process protocol of transfer printing for enhancing the yield of doped microwires from SOI wafer to a flexible PET substrate is of prime investigative area in this research. A prototype flexible thermoelectric generator is presented based on alternately doped Si microwires transferred to flexible substrate by using an elastomeric stamp i.e. PDMS. The level of doping for optimum

operation of the thermoelectric generator can be controlled on wafer by using standard techniques and the prepared samples can be transferred successfully onto an alien substrate. The open circuit voltage response of the thermoelectric generator is well in compliance with state of the art devices. The alternately doped pn-Si microwires are also investigated under ambient environment for the photodetection and fuel cell applications. Flexible thermoelectric generators could successfully be implemented in light weight portable electronics applications due to the attractive advantages of light weight enhancing excellent portability, bendable, stretchable, large areas and more resistant to impact.

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Chapter 6
MISFET Devices with Single Si Microwire

Part of this chapter has been published in:

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S. Khan, N. Yogeswaran, L. Lorenzelli and R. Dahiya, "**Si microwires based FETs on flexible substrates**" *11th IEEE PRIME Conf. 338-341, Glasgow, UK, 2015.*

This chapter presents the advancement of Si microwires towards device manufacturing. A novel fabrication route is developed for obtaining high performance bendable field effect transistors (FET) by embedding silicon (Si) microwires (2.5 µm thick) in layers of solution-processed dielectric and metallic layers. The objective of this study is to explore heterogeneous integration of Si with polymers and to exploit the benefits of both microelectronics and printing technologies. Arrays of Si microwires are developed on silicon on insulator (SOI) wafers and transfer printed to polyimide (PI) substrate through a polydimethylsiloxane (PDMS) carrier stamp. Following the transfer printing of Si microwires, two different processing steps were developed to obtain top gate top contact and back gate top contact FETs. Electrical characterizations indicate devices having mobility as high as 117.5 $cm^2/V.sec$. The fabricated devices were also modelled using SILVACO Atlas. Simulation results show a trend in the electrical response similar to that of experimental results. In addition, cyclic test was performed to demonstrate the reliability and mechanical robustness of the Si µ-wires on flexible substrates.

6.1. Motivation for Microwires based MISFETs

Active flexible electronics especially MISFETs, are extensively explored devices in recent years for their increasing demand in a range of applications such as sensors, displays, robotics, prosthetics and health monitoring etc. [1]. Some of the driving features for flexible electronics are the requirements such as conformable integration to nonplanar objects, portability, foldability and large area coverage of uneven 3D surfaces [2-4]. A cost-effective and reproducible method for constructing such electronic devices is much needed and therefore the merging of conventional microelectronics technology with age-old printing/coating tools are foreseen to provide a feasible manufacturing platform. Research is already in progress towards this hybrid manufacturing with some positive indications for successful integration [2, 5-7]. Polymeric materials remain the preferred choice for printing technologies and a remarkable interest has been shown towards printing of organic materials due to their solution processability at low temperature and ambient environment. The intrinsic properties such as mechanical flexibility, low materials and fabrication costs give organic materials an extra edge for selection over other materials. Further, they are often compatible with roll-to-roll

processing and the thermal budget of polymeric substrates (< 300 ^{o}C). Despite these attractive features, obtaining high-performance devices from organic semiconductor remains a major challenge [8-10]. Devices made of organic semiconductors typically have low charge carrier mobility (~1 with respect to ~1000 cm^2/V.s of single crystal Si) [10-12], which makes them much slower to respond than crystalline Si built devices. Furthermore, poor stability and short life of the organic materials make them a poor choice for electronic systems requiring better performance and high durability. A large number of applications, especially where faster communication and computation is needed, require high-performance flexible electronics [9, 12].

In this regard, the electronics based on a mix of both organic and inorganic materials could be an attractive option, as high-mobility inorganic semiconductors would enable devices with faster speed and stable performances. In past, using polycrystalline Si in place of organic materials helped in overcoming some of the performance related challenges, but this came at the cost of complex procedures and sophisticated setups for achieving suitable uniformity [13-15]. Thinning down the standard Si wafers by mechanical or chemical-mechanical polishing is another approach, which has been explored to realize high-performance flexible electronic circuits [16, 17]. However, flexible chips are more prone to damage either during the thinning process because of the brittle nature of Si wafer or caused by small dislocations within the crystal. Overcoming issues related to small mismatches and cavities in the material crystal pose further challenges for wafer thinning route as these might rapidly propagate in the form of cracks during or after the thinning process. In this regard, the miniaturized structures such as Si nano/microwires could offer better solutions [18, 19]. The viability of Si nano/microwires for high-performance flexible electronics has been demonstrated recently with high temperature processing steps performed on the donor wafer and relocating or transferring the wires to flexible substrates [9, 10, 17, 20-23]. The transfer of wires to secondary flexible substrates can be carried out either by dispersing them in a solution or through a stamp-assisted dry transfer printing technique [5, 8, 18, 21, 23, 24]. However, stamp assisted transfer printing is preferred as it guarantees the orientation of finished or polished surfaces for post-processing of transfer printing for devices' fabrication.

The frequently reported devices with dry transfer printing of Si are back-gated FETs, where the dielectric layer is restricted to a single type of material, which is also used as the adhesive layer [10, 24, 25]. Devices developed with such configuration have potential applications in microfluidics and biological sensors where the semiconductors wires are left exposed for direct interaction with the external stimuli [18]. On the other hand, a number of physical sensors such as pressure, temperature, proximity, humidity and many other electronic devices can be developed in structures that have a direct interface of Si microwires with transducer materials. In this study, a new manufacturing technique is proposed and optimized for the development of both top and back-gated FETs on PI substrate by embedding Si microwires in solution-processed materials. A reliable and cost-effective manufacturing route is the focus of this research. The

processing steps for deposition of diverse gate dielectrics and screen-printed metallic contacts within the thermal budget of PI substrate are presented along with proof of concept devices. A single Si microwire (50µm wide) is selected for the fabrication of a typical FET in the shape of back and top-gated structures. The detailed description of technology, device designs and simulation results are presented in the following sections.

6.2. Si Microwires Designs and Fabrication

The manufacturing process begins with the definition of Si-microwires on SOI wafers through a top-down method, which involves standard photolithography and etching steps (discussed in detail in previous chapters 4-5). The SOI wafer (Soitec, p-type Boron (B) doped with resistivity of 15-20 ohm-cm and a device layer with thickness of 2.5µm) is selected as the donor or mother wafer to obtain microwires with similar dimensions such as thickness, width and length. The thickness of microwires is alike due to the well-controlled thickness of top Si layer i.e. above the buried oxide layer in

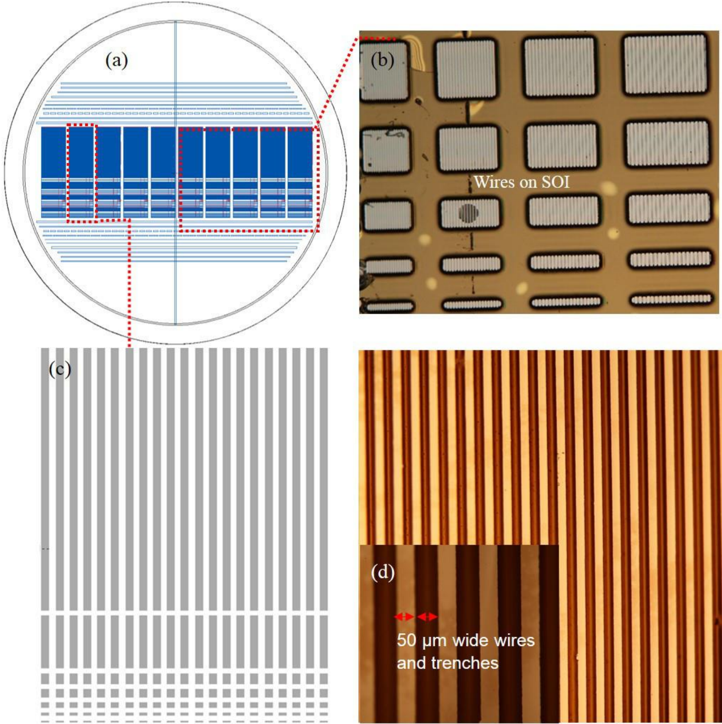


Figure 6.1. Microwires design, with corresponding lengths and modules, (a). Wafer-scale design of microwires, (b) Microscopic image of individual block of Si microwires, (c). Array of 200, 500, 1000, 2000 and 5000 µm long wires, (d) Microscopic image of etched wires.

SOI wafer. Using deep reactive ion etching (DRIE), the vertical trenches (with depths up to the buried oxide) are realized between the microwires. The modules with different lengths and widths of microwires were fabricated in parallel arrays of 20 wires, as shown in Figure 6.1. Different dimensions of the microwires were investigated to understand and evaluate the influence of interface between carrier stamp and Si microwires and hence optimize the transfer yield. The widths of microwires investigated in this study were 10, 20, 30, 40 and 50 µm. Similarly, the lengths of the wires were 200, 500, 1000, 2000, and 5000 µm. The width of the trenches also plays an important role during etching of the buried oxide layer as well in the first transfer-printing step. For this purpose, the trenches with varying widths i.e. 10, 20, 30, 40 and 50 µm were realized. Anisotropic etching is desired to develop high aspect trenches with vertical cut at 90° and uniform edges, which was achieved with DRIE.

Before initiating the under-etching of buried oxide from microwires, the trench edges were completely cleaned of all the passivation and organic residues. To do this, the microwires were bathed in piranha solution prepared by H_2SO_4 and H_2O_2 in 3:1 respectively, followed by rinsing in deionized water. The standard etchant for SiO_2 i.e. 40% buffered hydrofluoric (BHF) is used to etch away the buried oxide and release the microwires completely until the anchored points at the ends. To ensure the complete release of the wires, samples were retained in the etchant solution for 10 extra minutes from the time required for complete under-etching of the oxide layer. After completing the etching step, the microwires are gently cleaned with deionized water and dried in furnace at 100 ^oC. The post-processing steps after under-etching the oxide layer need proper care to ensure the microwires remain tethered to the donor wafer. In current study, transfer printing of 50µm wide wires are explored and the same were ultimately used for field effect transistors.

6.3. Experiments and Characterization

The PI substrate (25 µm thick) is selected for the development of FETs, owing to their good stability and high thermal budget ~ 300 ^oC. PI substrate was cleaned with isopropanol, deionized water and attached to a glass slide, which is used as a temporary carrier and removed after the process is complete. For better hydrophilic property and enhancing the adhesion of subsequent layers, the substrates were treated by plasma oxidation and subsequent layers were printed immediately. This step is essential for the back-gated FET structure, as the silver gate electrode was to be patterned with screen-printing technique. As screen-printing is nearer to manufacturing, the patterning of back-gate electrode using screen-printer is a step towards low-cost manufacturing of the flexible FETs. The physical and electrical properties of metal patterning through screen-printing is described in detail elsewhere [26]. Converse to the back-gated FETs, the SU-8 that acts as the primary adhesive layer for receiving Si microwires was directly spin coated on PI substrate after treatment with oxygen plasma for the development of top-

gated FETs. Following sections describe the fabrication of flexible FETs from arrays of Si microwires.

6.3.1. PDMS Moulding and Stamp Development

Development of a planar stamp is highly desired for reliable transfer of Si microwires, which could satisfy a conformable contact and maximized interface area with these wires. For this reason, a mouldable elastomeric polymer i.e. poly(dimethyl siloxane) (PDMS) is used for the development of carrier stamp to pick up the free standing microstructured Si from donor wafer and transfer them with controlled orientation to the final flexible substrate. A special setup for the stamp mold is designed from acrylic as shown in Figure 6.2, which is configured to clamp two silicon or quartz wafers. Reason for using these commercial wafers is to get uniform and smooth surfaces of the PDMS stamp i.e. with minimal surface roughness. The uniformly polished surfaces of the silicon wafers are kept in face-to-face in the mold setup and PDMS (base: curing agent, 10:1) is poured into the mold. For proper control and easy release of the stamps, plasma oxidation of wafers followed by silanization is an efficient way to help peeling off the wafers afterwards. After filling the mold with PDMS, setup is kept at 60 ^{o}C for 2 hours for complete polymerization and wafers are removed from stamp.

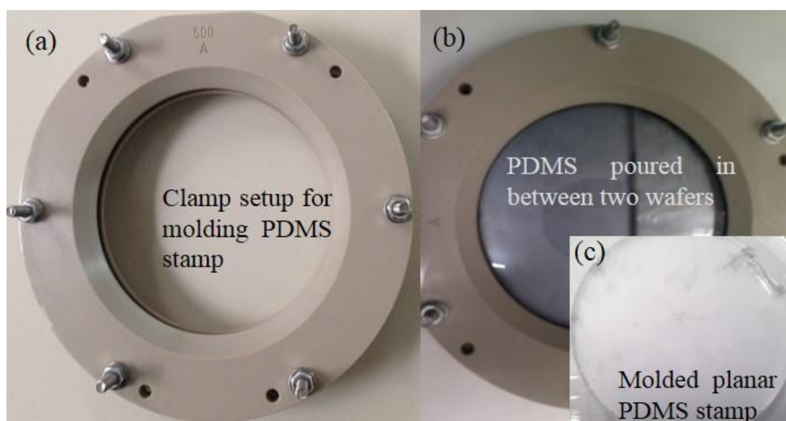


Figure 6.2. Setup for development of a planar stamp (a). Clamp setup for holding polished wafer face-to-face, (b). PDMS poured in between two wafer and curing (c). Final moulded stamp after removing Si wafers.

6.3.2. Deterministic Transfer Printing of Si Microwires

The transfer of Si microwires can take the route of either wet assembly or a stamp assisted dry transfer technique. Dry transfer of Si microwires through a carrier stamp is

the preferred approach for deterministic placement of microwires and to guarantee the same orientation of top surface of microwires for subsequent processing layers of the MISFET devices. Further, the crystallinity and doping profile are assured to remain on the top of microwires as developed initially on the SOI wafer. The materials that could be easily moulded in different structures with the clear and uniform surfaces are desired for transfer stamps. In this regard, PDMS (poly (dimthylsiloxane)) is a natural choice as in addition to the easy moulding in different shapes, its viscoelasticity also enhances the transfer printing with possibility of tuning the peel off rate of the stamp.

To increase the transfer yield in the first transfer step, a planar surface of the stamp is desired for a conformal contact with the microwires and to maximize their interface area with the microwires. A slight misalignment or gap between the two surfaces can result in a weaker bond, which may not be sufficient enough to detach the microwires from the donor wafer, especially at their tethered positions. For this purpose, a dedicated mold was designed to hold two polished Si wafers at a defined distance and the PDMS (base: curing agent, 10:1) was poured between them to be moulded. Prior to dispensing PDMS within the mold, the wafers were silanized to obviate the development of stronger bonds between moulding wafers and PDMS, which ultimately helps in removal of PDMS stamp from the wafers. After filling the mold, the PDMS is kept for

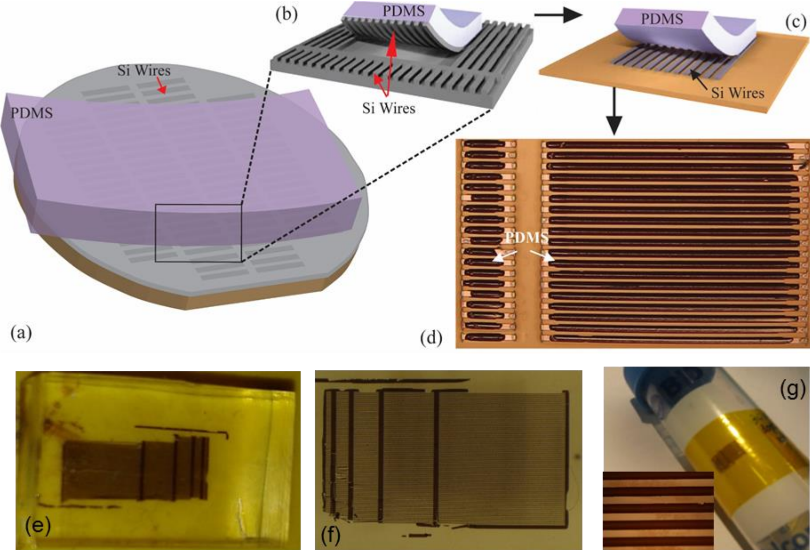


Figure 6.3. Fabrication of Si microwires and transfer printing to temporary transfer substrate. (*a*) Patterning of wires and under-etching of buried oxide (b) Transferring Si wires from wafer to PDMS stamp (c) Stamping PDMS with microwires on final receiver substrate (d) Peeling off PDMS, leaving behind microstructures on PI. (e) Corresponding experimental step for transfer of Si to PDMS from mother wafer (f) Experimental results of transferring Si wires to PI substrate after removing PDMS stamp (g) PI substrate with transferred Si microwires wrapped around circular shaped object. [1, 17].

polymerization in a furnace at 60 ^{o}C for 3 hours.

Transfer printing of Si microwires to PI is accomplished in two steps through the PDMS stamp as shown in Figure 6.3. A thicker stamp is used for easy handling and also to avoid breaking of the wires during the transfer process. Thicker stamp also aids in keeping a large peel-off angle, which is an essential requirement in the first transfer step to avoid cracking of the Si microwires during the course of detachment. PDMS stamp was treated with oxygen plasma to tune its surface properties for better pick-up of microwires from the donor wafer. Other parameters enhancing the detachment of tethered wires from the donor wafer include over-etching of oxide under the wires and the peel-off rate. More than 95% yield of microwires transfer was achieved in the first transfer step as shown in Figure 6.3(f), which is a significant improvement over our previous results [20]. In the second transfer step, a stronger adhesive is needed on receiver substrate so as to detach the microwires from PDMS stamp. Therefore, SU-8 (a high contrast photoresist and sensitive to ultra violet (UV) light) is used as the adhesive layer. SU-8 has the desired level of stickiness when partially sintered, and hardens after complete sintering. A thin layer of SU-8 is spin coated at 5000 rpm to achieve thickness of about ~800 nm. This layer is partially sintered by putting it on a hotplate at 90oC for 80 seconds. PDMS stamp with Si microwires is then brought in conformal contact with SU-8 layer and passed through UV light for complete sintering. The transparent PDMS allows UV light to pass through the spaces between the microwires, which results in the hardening of SU-8. The UV light is also used on the sideways and backside of the substrate to complete the sintering process. As a result, 100 % transfer yield is achieved after removing back the PDMS stamp as shown in Figure 6.3 (e & f). Finally, the SU-8 layer is hard baked at 130 ^{o}C for 30 minutes in a furnace and subsequent layers are deposited for development of FETs. Figure 6.4 shows microwires on PI substrates placed on objects with different curvatures. The SU-8 layer is also used as the gate dielectric for back-gated FETs. The thickness of SU-8 layer was optimized to suit its use both as the adhesive and as the dielectric layer.

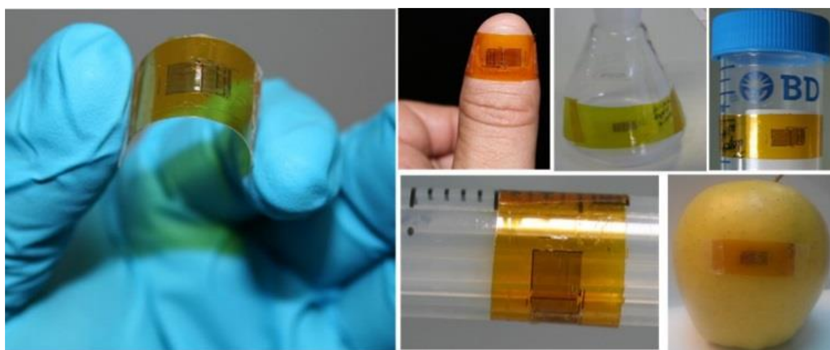


Figure 6.4. Transferred Si microwires on PI substrate and attached to various objects with different orientations and radius of curvatures.

6.3.3. Screen Printing of back-gate metal

Screen-printing is a robust technology where materials are patterned in a single step by dispensing the solution through stencil/screen masks. It is the most prominent and matured technology for printable electronics as it has remained the dominant technique in electronics industry for long time to print metal interconnects on PCBs (printed circuit boards). It is faster and more versatile in comparison to other printing tools, as it adds simplicity, affordability, speed and adaptability to the fabrication process. The results from screen-printing can be reproduced by repeating a few steps and an optimum operating envelope can be developed very quickly. Most of the solvents/pastes are optimized and available commercially in the market for printing with desirable properties. Screen printer has simple setup comprising of screen, squeegee, press bed, and substrate, as shown in Figure 6.5. A flatbed screen-printed is used for printing metal contacts of the back-gate MISFETs. In flatbed, the ink poured on the screen is squeegeed to move across the screen resulting in its transfer through the stencil openings to the substrate beneath it.

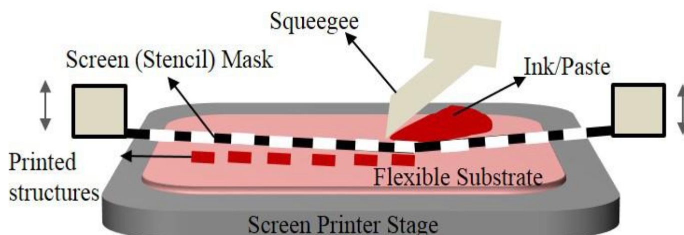


Figure 6.5. The flatbed screen printing with planar substrates for solution dispensing

Metal patterning is the preliminary step prior to the transfer process. Silver (Ag) based paste (DuPont-5028) is used for patterning on the flexible substrate. A bare Si wafer is used as the carrier for flexible PI substrate, which is attached to it by using a reproducible scotch spray on the rim of the wafer. The PI substrate is properly cleaned using ethanol, isopropanol and DI water to remove the contaminants. To enhance the adhesion of the Ag patterns to the PI, an extra step of plasma oxidation is performed. The metal patterns are 100 µm as per design, but the width of the lines obtained on the PI are increased due to spreading of the solution. To minimize the variations in the patterns widths, printer parameters as the stage height and speed of the squeegee are adjusted, which helped in reducing the widths as well as maintaining the uniformity of the patterns edges. Figure 6.6 shows image of the screen printer and printed metal patterns. The PI is then cut into small pieces to utilize each wire for individual back gate application. Sheet resistance of the conductive patterns has been measured in planar and bent mode to check any change in conductivity. Four-point collinear probe setup was developed by using high impedance Keithley 7410 voltmeter for current and voltage analysis. The sheet resistance value given by the supplier for the printed silver paste is

about 12Ω/sq., for the layer with thickness about 25μm. The sheet resistance measured in our samples (layer thickness of about 8μm) is 14.15 Ω/sq. in the planar mode, which is in the close range of expected sheet resistance of silver paste after sintering.

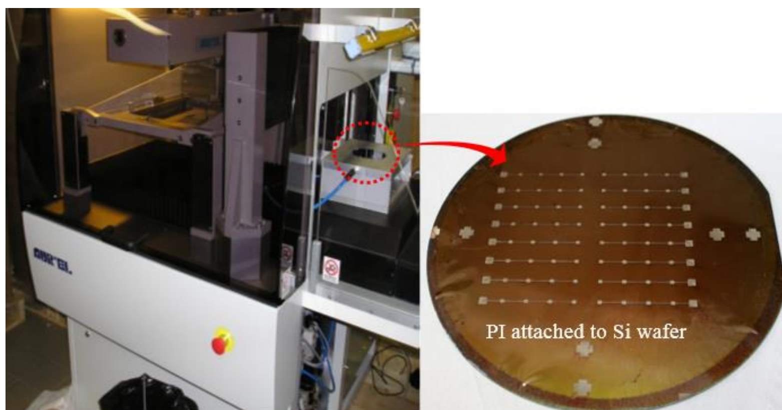


Figure. 6.6. Screen printer used for patterning of Silver (Ag) for the back-gate of MISFETs

6.3.4. Fabrication of FETs structures

The efficacy of transferred miniaturized Si microwires can be authenticated by their potential use in an active device. For this purpose, the transferred Si microwires are incorporated within layers of dielectric and metallic materials to complete the manufacturing steps for a typical FET structure. Two types of structures are investigated in this work. These are: (a) back-gate top contact, and (b) top-gate top contact FETs. For the back-gated FETs shown in Figure 6.7, the silver (Ag) gate electrodes are screen-printed on PI substrate. The adhesive layer is then spin coated, which is followed by transfer of Si microwires. This is followed by micro spotting of Ag paste for source and drain contacts.

The processing steps for the back-gated FETs are shown in Figure 6.7. The back-gated FET structure has single dielectric material (in this case, SU-8), which is also the essential adhesive layer needed for transferring of Si microwires. SU-8 is the most suitable material in the proposed fabrication process, as it also possesses suitable optical properties such as high contrast and sensitivity to UV light. The optical transparency is required for the overlay registration accuracy of the Si microwires with the underlying patterns of back-gate electrodes. As explained earlier, the sensitivity to the UV light also helps in the hardening of SU-8 before PDMS stamp is removed in the transfer print process. The UV curability makes the transfer printing process robust and helps us achieve 100% microwires transfer yield in the second transfer step. In this regard, the SU-8 layer in back-gate FETs has to meet the trade-off between thicknesses needed for better performance of the transistor (when its use as dielectric is considered) and for its

use as adhesive to detach Si microwires from PDMS stamp. To meet both the requirements, the recipe for spin coating was optimized and SU-8 was coated at 5000 rpm to achieve a thin layer of ~800 nm.

To expand the field of applications of Si microwires and make process compatible with a wide range of dielectrics or transducer materials, top-gated FET structure is desired. This approach can also lead to processes, whereby organic materials could be integrated with the inorganic semiconductors. This will ultimately result in low-cost fabrication as a result of the lower cost of organic materials and their solution processability. In this case, the top dielectric and metal layers also serve as the encapsulation layer for the Si micro wires and protect them from harsh environment. Embedding the brittle Si microwires in suitable solution-processed materials could also improve overall bendability and prevent breaking of wires during bending [16]. The construction of top-gated FETs starts with the spin coating of SU-8 layer on top of cleaned PI substrate, with the same spinning recipe as described above for the back-gated FETs. The design and process steps for the top-gated FET utilizing a single Si microwire are shown in Figure 6.8. After transfer printing of Si microwire and hard baking of the SU-8 layer, silver (Ag) paste is patterned on top of Si microwire using micro-spotting technique. After thermal treatment of the Ag paste, the dielectric material was spin coated on top of these patterns and Si microwire. To make the process robust, a UV-curable dielectric material was selected. The spin speed was kept at around 5000 rpm where thickness achieved was in the range of 300-400 nm. The

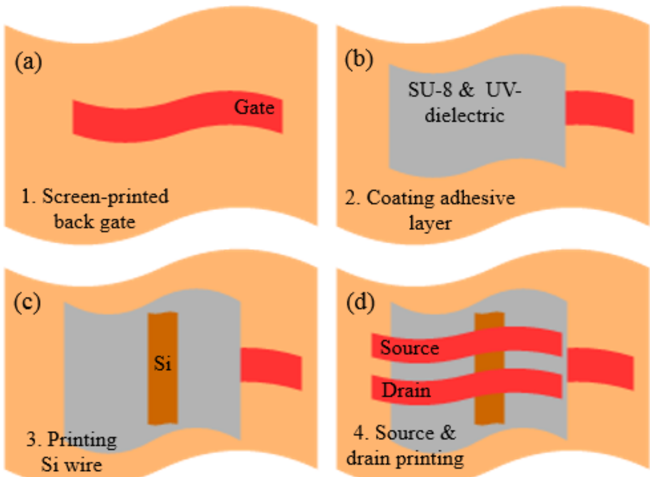


Figure 6.7. The process flow showing the step by step material layers deposited for a back-gated FET. The numbering show the sequence of steps performed for developing each layer for development of field effect transistor from a single Si microwire. (a) Screen printed back-gate lines on PI substrate. (b) Spin coating of dielectric adhesive layer. (c) Transferring Si microwires on adhesive layer (d) Patterning source and drain on top of Si microwire.

variation in the thickness is due to the non-planar surface as a result of Si microwire on the PI substrate, which hinders the uniform spreading of the dielectric material and thus results into non-uniform thickness of the final layer.

The mechanical reliability and adhesion of Si microwires under different bending radii was investigated through cyclic tests. The physical robustness of the structures was evaluated by observing crack propagation and delamination of the microwires from the receiver substrate. Substrate was wrapped around different circular and nonplanar shapes for one time bent as shown in Figure 6.4, while cyclic tests were performed for repeated bending of the microwires. During the course of cyclic tests, the secondary PI

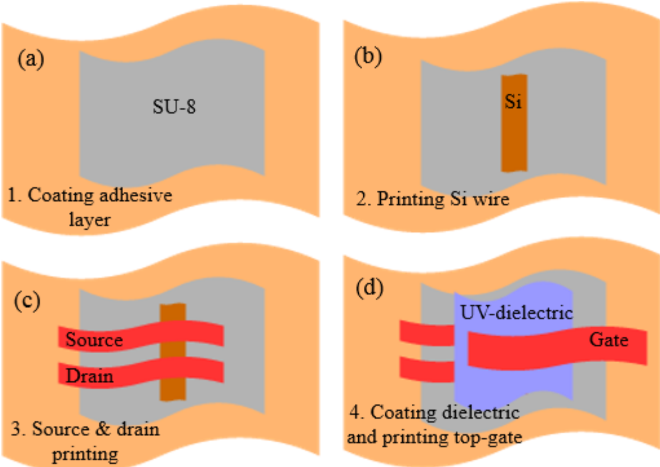


Figure 6.8. The process flow showing the step-by-step materials layers deposited for top-gate FET. (a) Spin coating adhesive layer on PI substrate. (b) Transferring Si microwires on adhesive layers, followed by patterning source and drain contacts. (c) Spin coating UV-dielectric layer. (d) Patterning top metal layer as a gate electrode.

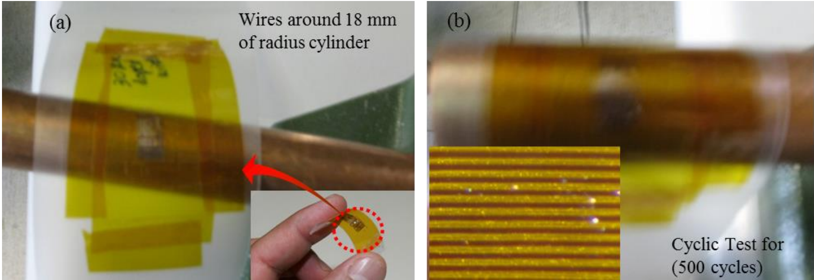


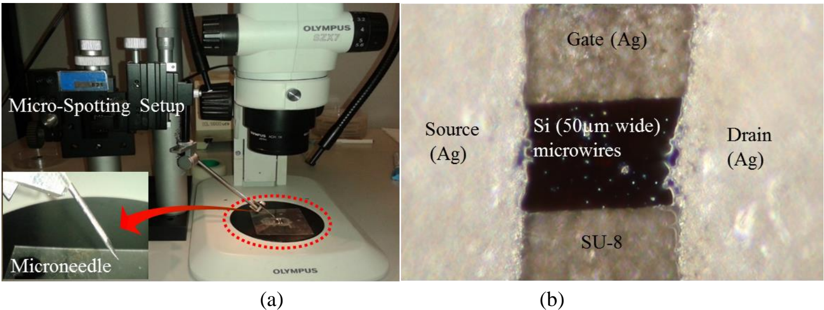
Figure 6.9. Cyclic test for testing cracks or delamination of Si microwires from the adhesive layer (a). PI substrate containing Si microwires is fixed to a separate plastic sheet and wrapped around different size nonplanar surfaces, (b). During the cyclic test, the inset image shows wires after the cyclic test.

substrate containing the microwires are attached to a separate plastic sheet as shown in Figure 6.9. Where it is revolved around cylinders with outer diameters of 8, 12 and 16 mm. Bending tests are performed through the plastic sheet for about 500 cycles around each cylinder and observed under an optical microscope for cracks or delamination from the substrate. By observing all the microwire arrays under an optical microscope, we observed no cracks or delamination of the wires from the adhesive layer after cyclic tests, which confirm the mechanical robustness of the wires.

6.3.5. Micro-spotting of Ag for metallization

The micro spotting is performed using a custom-made tool comprising of a precise positioning setup and tungsten needle of micrometre size tip. The needle in the setup is clamped with a steel rod, which is free to move in three dimensions. The tungsten needle is used to pick up a small droplet of Ag paste from solution and source and drain contacts are realized by micro spotting at the desired areas and simultaneously observing it through a microscope. The spacing between the two electrodes defines the effective channel area of the FETs on the Si microwire. After deposition of the dielectric layer, the gate electrode is designed to align over the effective channel areas, making it possible to realize a field effect transistor at the crossing. Each transferred block contains a parallel array of 15 microwires of 50 µm wide each. Amongst these, a single microwire is selected for the construction of FET devices to investigate its physical and electrical characteristics.

The proposed approach is unique as the aspect ratio, which is conventionally used to set the current in transistors, can simply be changed with increasing the number of Si microwires in a single block or by increasing the number of electrodes on a single wire, assuming 100% overlay registration accuracy of gate electrodes is possible. Figure 6.10 (a & b) show the micro-spotting tool used for patterning of Ag paste for the source and drain contacts and a typical FET structure realized by using this micro-spotting tool. The order of patterning is different for top and back-gated structures. Micro-spotting is



(a) (b)

Figure 6.10. (a) Micro-spotting tool for Ag metallic contacts of FETs in, (b) developed FET structure by using a single Si microwires as a the semiconductive layer, silver (Ag) for source drain and gate and SU-8 as the adhesive and dielectric layer.

applied only for source and drain patterning on top of Si microwire in the back-gate FETs, whereas the source and drain are patterned in the first place in top-gate FETs by micro-spotting followed by spin coating of dielectric layer and again micro-spotting of the top gate. The edges of the source and drain patterns are not uniform, as the low viscosity Ag paste tends to spread irregularly after micro spotting. This non-uniformity

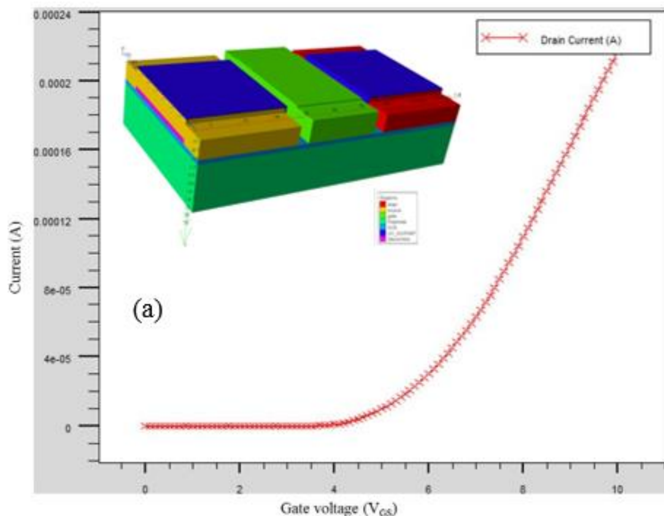


Figure 6.11 (a)

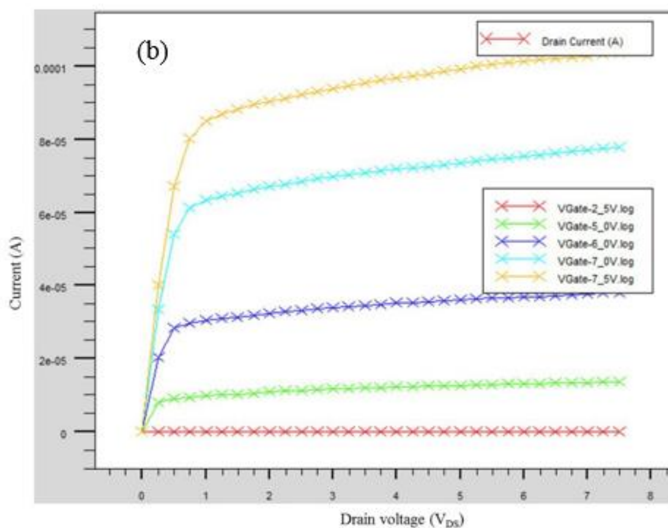


Figure 6.11. Simulation with similar structures & materials as used in this work, (a) FET model for top gated FET, (b) Output response and, (c) Transfer curve of the simulated device.

could be reduced either by using smaller droplets or by using a more viscous solution, which has a low co-efficient of spreading.

Simulations of the proposed designs were initially performed with SILVACO Atlas by assuming a Si strip. The dielectric materials were defined by using existing models for the standard materials of MOSFET technology. Simulation results by using close

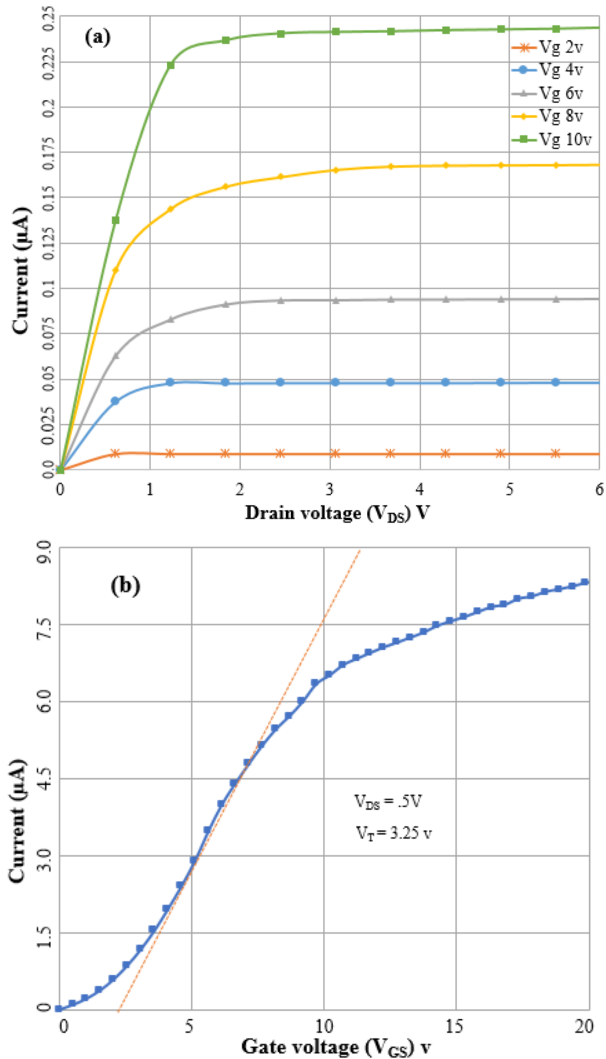


Figure 6.12. (a) Output response with SU-8 3010 as dielectric material in a back gated FET, (b) Transfer curve with UV-DuPont as dielectric material in back-gated FET

matching dielectric properties of the material used in experiments i.e. UV-curable dielectric are shown in Figure 6.11, which presents the output and transfer characteristics of the device. The output characteristics of the simulated devices showed similar behaviour as obtained with experiments. The small deviation in the experimental results (in Figure 6.11 and 6.12) is due to the non-ohmic contacts of the Ag paste with lightly doped Si microwires. The silicide contacts made by using Ag paste on top of Si microwires also contribute to the lower values of output currents in the experimental results. Further, the semiconductor and dielectric interface also affects the performance of the device. On average, the device's response with different dielectric materials simulated with the same model show similar trend of performance to the experimental results.

Electrical characterizations of both devices were performed in ambient environment using semiconductor parameter analyzer (4156C, Agilent). By efficient transferring of 50 µm wide wires onto PI substrate, the FET device fabricated from a single microwire has a channel length and width of ~ 60 µm and 50 µm respectively. The channel length of the microwire based FET is dependent on the high-resolution patterning of metals for source and drain contacts. Being a manual technique the channel length is controlled in close ranges to ~ 60 µm. On the other hand, the channel width can be well controlled, as the standard lithography tools set the width of Si microwires, which defines the channel-width. In these experiments, the maximum width i.e. 50 µm wires are selected due to the good transfer yield.

The Si-microwires FETs on PI substrate were characterized and Figure 6.12 (a & b) and Figure 6.13 (a, b) show the plots for the output and transfer current-voltage (I-V) characteristics of the back-gated and top gated FETs respectively. The field-effect mobility (µFE) of devices was extracted using $\mu FE = L_G g_m / (W_G C_G V_D)$, where L_G (~ 60 µm) and W_G (50 µm) are the physical dimensions of the gate length and width respectively. The highest value of field effect mobility recorded was 117.5 cm^2/V.sec and this was achieved with top-gated UV-curable dielectric material. The mobility achieved with the bottom gated SU-8 was 69 cm^2/V.sec. The threshold voltage measured through extrapolation in the linear region show 2.75V and 3.25V for bottom and top gate FETs respectively. As the Si-microwires are not heavily doped, so the linear region indicates the large parasitic resistance associated with the source and drain contacts, the behaviour that is similar to a small schottky barrier FET.

The small parasitic resistance indicates the need for further doping of the Si-microwires and optimization of the patterning in future to obtain ohmic contacts and lowered barrier for charge carriers. The output and transfer curves in Figure 6.12 and 6.13 show clear saturation behaviour at larger positive biases. Further, the gate dependence of the curves confirms the operation of the device inversion mode of the p-type microwires. All devices were operated in the inversion mode requiring a positive gate voltage to turn on the device. The back-gated FETs showed poor modulation of the channel conductance due to the increased thickness of SU-8 gate dielectric accompanied by the thickness of the Si microwires (2.5 µm). The fabricated FETs were also tested

after cyclic tests and the electrical characteristics remained the same as observed in Figures (6.12 & 6.13) before the cyclic tests. The mobilities achieved with the top-gated FETs are in the ranges needed for applications in flexible electronics circuit such as inverters, ring oscillators and as active matrix for displays on polymeric substrates [27].

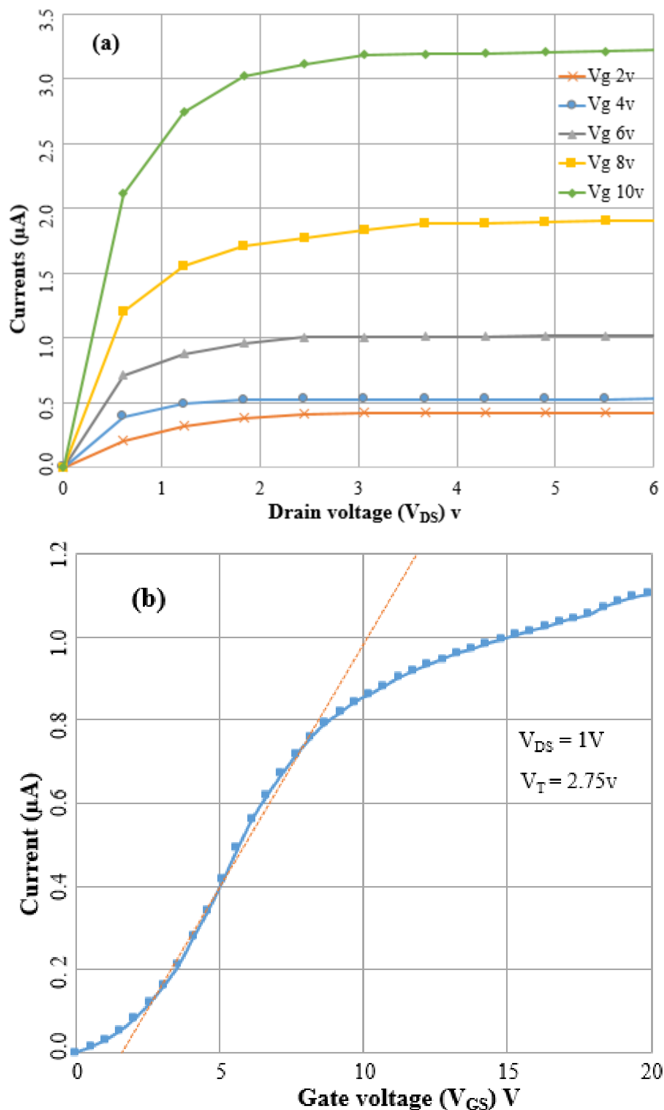


Figure 6.13. (a). Output curve of UV-DuPont dielectric as dielectric material for top-gated FET (b). Transfer of UV-DuPont as dielectric material for top-gated.

6.4. Conclusion

In Summary, a reliable and cost-effective manufacturing route is presented for top and back-gated FETs on flexible PI substrates by incorporating single crystal Si microwires in diverse solution processed dielectric and adhesive materials. Si microwires are obtained by top-down fabrication approach and transferred to an adhesive layer on PI substrate by using PDMS assisted transfer printing. The back-gate electrode is screen-printed, which is a step towards low cost manufacturing. Results validate the top and back-gated FETs and the use of different dielectric materials in fabrication of these FETs. The feasibility of embedding Si-microwires within layers of solution-processed materials opens new avenues for fabrication involving both microfabrication and printing tools. The physical and mechanical characterizations of the devices are performed by doing cyclic bending tests by monitoring the cracks or delamination of the microwires from the adhesive layer of flexible substrate. The I-V measurements show a better range of performance as compared to the devices developed from organic based materials.

The back-gated FETs have great potential for chemical and gas sensing applications due to the direct interaction of the stimuli with the Si microwires. Similarly, the top-gated configurations provide an opportunity to deposit diverse transducers such as piezoelectric, pyroelectric or ferroelectric materials to develop sensors for measuring physical parameters such as tactile, soft touch and temperature. The behaviour similar to schottky barrier FET needs further investigation for the devices to offer an alternative for future flexible and large area printed electronics. To enhance the performance of FETs, potentially the metal-semiconductor interfaces could be processed through silicidation instead of using heavily doped semiconductors.

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Chapter 7
MISFETs with Ensemble of Multiple Si Microwires

Part of this chapter is in review process:

S. Khan, L. Lorenzelli and R. Dahiya, **"Flexible MISFET Devices from Transfer Printed Si Microwires and Spray Coating"**, *IEEE J. Electron Device Society (under review)*

This chapter presents two types of MISFETs (metal insulator field effect transistors) devices fabricated from Si microwires through a new manufacturing route, which advances the manufacturing route towards the establishment of solution based printing and microfabrication technologies. Si microwires, developed through standard lithography and etching steps, are transferred from a SOI (silicon on insulator) wafer onto polyimide (PI) using stamp-assisted transfer printing. The MISFETs are then obtained by spray coating the dielectric layer and metal contacts. Therefore, the proposed work presents an innovative approach for merging single crystal Si microwires within spray coated organic dielectric and metal patterns for development of MISFET structures. Reliability of the manufacturing process has been investigated in connection to reproducible results. Efficacy of the Si microwires and investigations of the variations caused by heterojunction of organic and inorganic materials for MISFET devices. Thorough description of the technological challenges, designing the most feasible fabrication route, device designs along with experimental details are covered within this research. Two groups of the devices are fabricated, one based on single Si microwire and the other based on the array of multiple (i.e. 15) Si microwires. The variations in the output response of the two groups of devices are investigated. The devices based on array of microwires are observed to have less variation in the output response, with lesser standard deviations as compared to MISFETs made from single Si microwires.

7.1. Motivation for MISFETs with Multiple Si Microwires

Accuracy in the repeatability of printing technologies is highly desired for realizing flexible electronics. The cost-effectiveness of the printing technologies would be fruitful if the devices manufactured are more reliable without significant variations. To make the fabrication process cost-efficient, the current trend indicates the merge of well-established microelectronics and conventional printing technologies in the future [1-3]. Solution based printing technologies are used to print functional materials in liquid or colloidal form, where a specific amount of desired materials is deposited and residual solution is collected back for reuse. Organic materials (especially semiconductors) have dominated the solution based printing technologies for flexible MISFETs. Organic materials have the advantage of inherent mechanical flexibility, and the lower material and fabrication costs. However, there are major challenges associated with obtaining stable devices with repeatable response and high performance i.e. at par with Si based

devices (mobility of organics is ~1 with respect to ~1000 $cm^2/V.s$ for single crystal Si) [4-6]. In this regard, the printing of inorganic semiconductors such as Si will be a promising alternative, as Si based devices are stable, faster, and have repeatable response [4, 7-10]. Transfer printing of nanostructures of single crystal Si has been demonstrated recently as viable route for high-performance electronics over flexible substrates [4, 8-14] (discussed in detail in chapter 6). Using Si in the form of nano/microwires to construct devices such as MISFETs also helps in overcoming the physical and mechanical reliability related challenges. The high aspect ratio of the Si nano/microwires widens the range of applications from basic electronic devices to

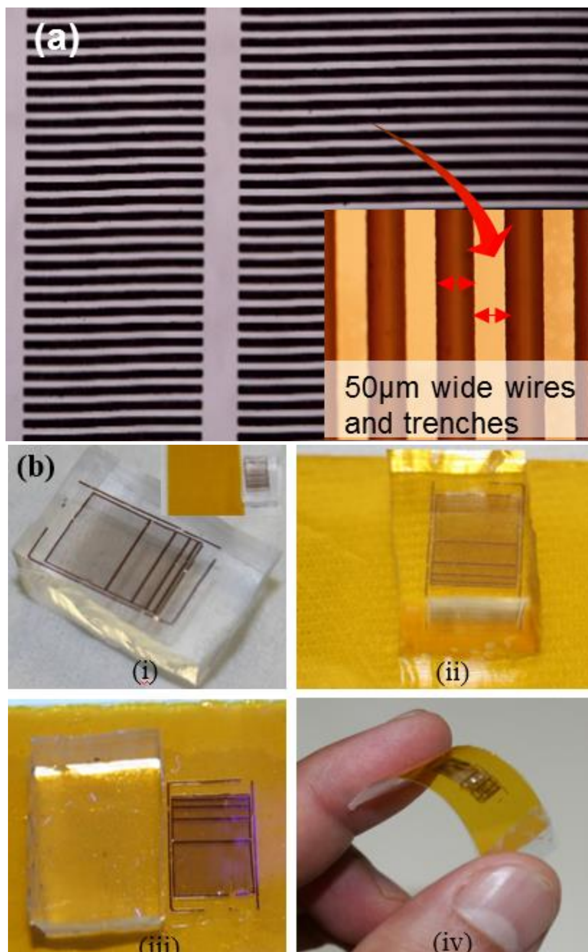

Figure 7.1. (a).Si wires on SOI wafers (b) Transfer printing steps: (i) Wires picked-up by PDMS stamp (ii) PDMS stamped on adhesive SU-8 layer (iii) Wires transferred to substrate after removing PDMS (iv) Wires in bent mode.

diverse applications such as sensors and energy harvesters.

The rapid development of flexible electronics based on different combination of Si microwires especially for thin film field effect transistors is key to the advancement of macroelectronic technology. Reliable manufacturing process and repeatable device responses are highly desired for Si microwires based transistors. As the manufacturing process is based on combination of different processes of transfer printed Si microwires and solution based patterning through printing, there is a greater risk of variation in device's geometric parameters. For instance, the solution flowability of conductor paste lead to nonuniform deposition with perfect control on the pattern edges. This would result in non-uniform channel lengths and widths of the MISFETs realized by using solution based patterning. The usefulness of Si microwires based devices are bound to have uniform or similar responses than the devices with non-uniform response. Greater variations in the discrete devices with similar geometric parameters lead to less acceptability. The efficacy of uniform response from Si microwires based MISFETs is more demanding when these devices are advanced towards circuits. For instance, with two similar transistors having dissimilar responses, the circuit design become extremely challenging. The attractive features such as portability, conformability and large area coverage of flexible and wearable electronics could only be harnessed if the individual devices' responses are in close range of operations [1, 15-17].

This work presents a promising approach for ensemble of single crystal Si microwires in thin films to fabricate MISFETs, using a mix of conventional microfabrication and printing steps. Using conventional microfabrication, the Si wires are defined on SOI wafer and then transfer printed onto final substrate (i.e. PI) using PDMS as career or transfer substrate. Spray coating has been introduced for the first time to deposit dielectric and metal thin films on Si microwires for fabrication of MISFETs. The spray coating to print dielectric and metal layers is a step further towards the integration of hybrid organic and inorganic materials. Spray coating is a low cost method and has low material wastage compared to other solution processed techniques [1, 18-20]. Therefore, spray coating has been used here to compensate the higher costs involved in the photolithography process for Si microwires. Two different types of MISFETs have been developed and evaluated for uniformity of responses among a set of each type of devices. These MISFETs are based either on single Si microwire or on an array of microwires. While conventional microfabrication tools allow better control over dimensions, the coating methods are not as good. As a result, the approach reported here is likely to result in the variability among the responses of similar type of devices. The MISFETs based on array of Si microwires are likely to have better response uniformity due to lesser statistical variation, which is also reflected in the results presented here. The heterogeneous integration of Si microwires with solution processed spray coatings, characterization of devices, and the effectiveness of the arrays of Si microwires in minimizing the device response variations are the focus of this chapter.

7.2. Experiments and Device Designs

The Si microwires (Figure 7.1(a)) were obtained from SOI (P-type silicon on insulator, 2.5-µm top silicon device layer and resistivity ~ 16 Ω.com) wafers using standard lithography and etching steps (described in chapter 2). The SOI wafer used here allows better control over the geometric parameters such as thickness, width and lengths of Si microwires leading to less design variations in first place. A stamp-assisted transfer printing technique (Figure 7.1(b)) is then used to transfer Si microwires from the mother wafer onto flexible PI substrates (thermal budget of PI ~300 °C) [21]. The details related to the transfer process and planar stamp are described in previous chapters and elsewhere [21, 22]. The efficacy of transferring Si microwires can only be validated by their usefulness in development of an active device with repeatable performance. To investigate the optimal solution for device variations, two types of MISFET structures developed and presented here are based on: (a) single microwire of 50µm width, and (b) an array of 15 wires (each 50 µm wide). The wire width of 50µm was chosen because of higher transfer yield obtained with this width of wires, as shown in the past [21]. The size and number of microwires could easily be reduced or

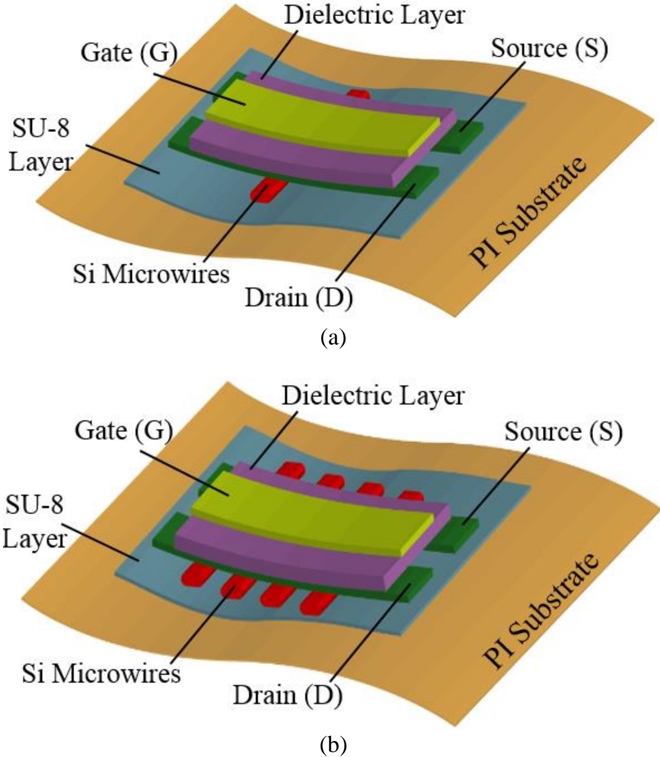

Figure 7.2. The scheme of MISFET devices using (a) array of Si microwires, (b) Single Si microwire.

increased during the photolithography stage in order to minimize or maximize the overall area of the final devices based on single as well as multiple microwires.

Top-gate top-contact MISFET structures are fabricated by using single and multiple Si microwires. Schematics of the architecture of top-gate top-contact MISFET structures based on single and multiple Si microwires are shown in Figure 7.2 (a & b) respectively. The device fabrication starts after placing microwires on flexible substrates. For top-contact, the source and drain need to be patterned on top of microwires. For this reason, a new innovative technique of spray coating (discussed in detail in next section) the silver paste is selected to deposit the metal patterns. Spray coating is helpful in maintaining the uniform boundaries, which in turn assist in minimizing the variations in the channel lengths of the MISFET devices. The fabrication steps are similar for both single and multiple Si microwires based MISFETs. Single wires from the array of 15 are selected after removing rest of the wires at the end of first transfer step, when the microwires are on the PDMS carrier stamp. Managing the number of microwires is challenging to control on the receiver substrate as the receiver layer have stronger adhesion to the SU-8 layer compared to weak interface of Si microwires and PDMS stamp. Additionally the transfer to the target flexible substrate is permanent as the receiver layer is sintered and the microwires are strongly adhered to the layer.

To make a trade-off and produce the transfer printing compatible with solution based printing and coating techniques, a reliable deposition and patterning mechanism of materials is desired to make the overall fabrication route feasible for integration of organic and inorganic materials. For instance, deposition of the dielectric layer and patterning of metallic contacts for the source, drain and gate contacts after transfer of Si microwires need to be developed from solution to lower the overall cost of the fabrication process. For this purpose, a spray coating technique has been developed in this research where all the post-processing steps after the transfer of Si microwires have been performed. Shadow masks were prepared by using a thin sheet (40 µm thick) of brass through milling machine and were used for deposition of organic dielectrics i.e. PMMA (Poly (methyl methacrylate)) and PC (Polycarbonate) and for patterning of source and drain contacts using Ag (Silver) based solution. Spray coating technique helps in reproducibility of the devices by maintain the similar fabrication steps and as a result the electrical response of the devices within close ranges.

7.3. Spray Deposition Through Shadow Masks

The overall cost of the fabrication process and functional materials for devices utilizing Si microwires as the semiconductor layer could be lowered by introducing solution based techniques of spray-coating/printing for the post-processing. Spray coating is a single step deposition process of functional materials where a hard/shadow mask is used to define the patterns. It is a low-cost process and experiments are performed in ambient conditions making spray coating compatible for the post-

processing of microwires. The post-processing steps after successful transfer of Si microwires are to deposit the dielectric material and metallic patterns a shown in schematic of the device designs in Figure 7.2 (a & b). All the post-processes of transfer printing are desired to be at low temperatures within the thermal budget of the polyimide substrate i.e. < 300 ^{o}C.

Similarly, all the chemicals are needed to be compatible with the polymeric substrate as well as with the adhesive layer to avoid deterioration of the interface between Si microwires and the adhesive layer. For this reason, the standard photolithography and etchants cannot be used for further processing of the Si microwires. Moreover, the surface of the Si microwires is not continuous because of the trenches between consecutive wires a uniform coating of the materials from solution is a challenging task. The aerospray coating technique is therefore an attractive choice for deposition of the dielectric and patterning of the metallic materials using shadow masks. Figure 6.3 shows images of 3D printer and masks prepared by using it. Shadow masks are made of plastic sheets, which are layered by gluing separate sheets of plastic to each other containing the desired structures. This is a fully automated way of producing these masks using a 3D printer (SD300). Such type of masks are more useful in spray coating of low viscosity solutions, where uniformity of layers are needed to be maintained after printing.

Figure 7.3. 3D-Printer with the final developed shadow mask for spray deposition of metal and dielectric solutions.

Spray coating is a direct deposition technique where the material is deposited from solution with specific process parameters like atomization pressure, snap-off between substrate and nozzle tip, speed and temperature of the supporting plate for the substrate. All the surfactants and solutions evaporate either during the spraying or immediately after deposition on the hot substrate. As a result, a very uniform and thin layer can be deposited from top covering the whole area especially the non-continuous surface of Si microwires. Spray coating is a robust process and there is less material wastage

compared to other solution-processed techniques. These features make the spray coating ideal for compensating the higher cost involved during the initial photolithography steps for wires development. Figure 7.4 (a&b) features the spray coating schematics where the influence of atomization pressure and fluid flow having a direct bearing on the control of the coated layer is presented. The significance and film quality dependence on the substrate heating is also highlighted in Figure 7.4 (b).

The quality of the coating by increasing the temperature to the level where all the surfactants are evaporated and solid particles adhere to the target surface. A UV-curable as well as organic dielectrics such as PMMA are selected for deposition of the dielectric layer for the field effect transistor, whereas Ag (silver) based paste is used to develop the metallic patterns for the source, drain and gate contacts. For patterned deposition of both the materials, shadow masks are used which are prepared by using a 3D printer. Spray coating system used for these experiments along with prominent components of

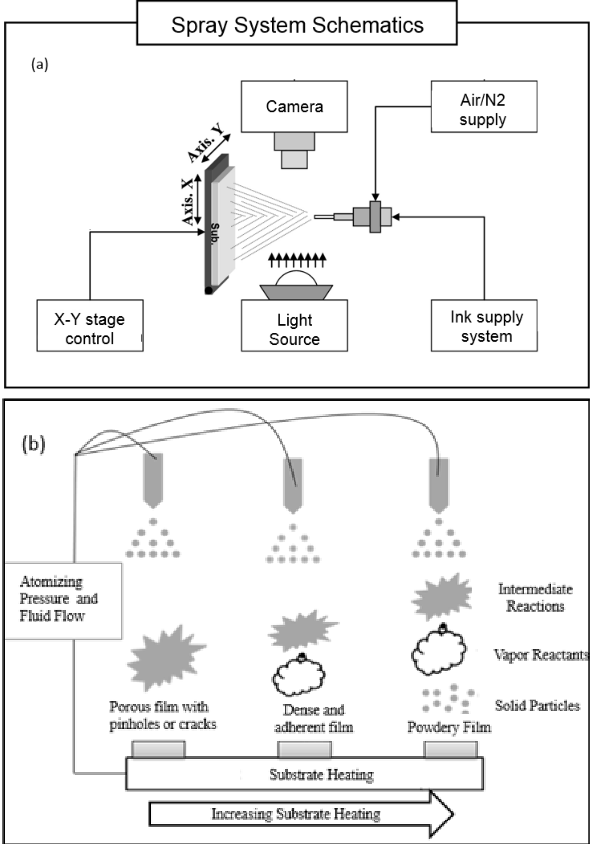

Figure 7.4. Spray deposition and influence of increased substrate temperature on the quality of the layer

spray deposition such as syringe pump, Teflon tubing for fluid delivery, nozzle holder, hot plate and shadow masks for patterned deposition are shown in Figure 7.5 (a-d). A double concentric nozzle with internal diameter 500 µm and external diameter of 1 mm as shown in Figure 7.5 (b) was used for the spray deposition. The internal nozzle was used for fluid delivery while the outer is used to allow compressed N_2 (Nitrogen) for spraying the solution.

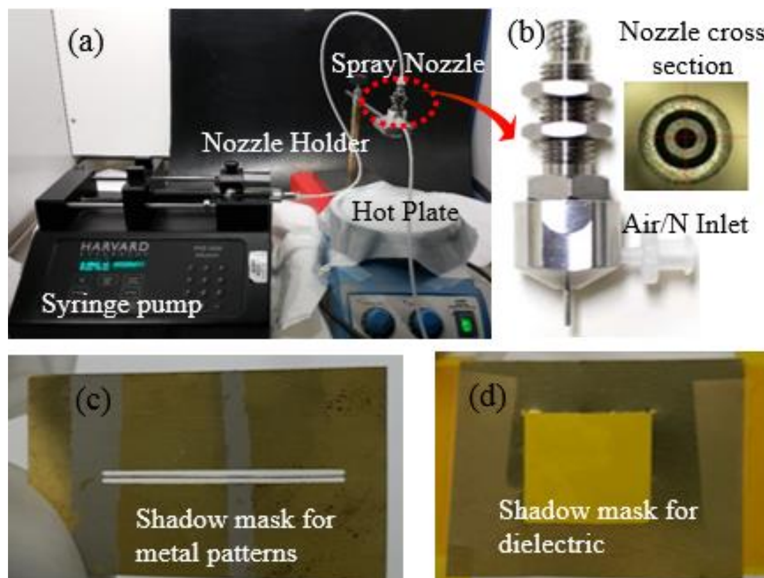

Figure 7.5. Spray coating system (a) main components of spray coating i.e. syringe pump, tube delivery, hot plate and spray nozzle. (b) Dual concentric spray nozzle with cross sectional view. (c). Shadow mask prepared using milling machine for metal patterns (d) Shadow mask for dielectric deposition.

A UV (ultraviolet) curable and solution of organic dielectric i.e. PMMA are spray coated at the channel area of the devices. Spray coating of dielectric layer is critical as the solution deposition from top covers all the exposed areas within the shadow mask for uniform deposition of a thin layer. The wire trenches could hinder the uniform or planar spreading of dielectric during the coating step; especially with conventional coating methods such as spin coating. Therefore, to make the process more robust and cost-effective, solution of organic dielectric i.e. PMMA was spray-coated to cover all the Si microwires including both the active area and trenches. A thin layer of about ~450 (±30) nm was achieved as a result of spray coating the dielectric solution. Variations in the layer thickness are observed because of multiple passes of the spray nozzle as shown in Figure 7.6. If sufficient time is not given for the solvents to evaporate from the substrates, multiple passes of the spray coating results in

accumulation of the solution at random locations. This occasional wet on wet deposition could be overcome by properly adjusting the spray nozzle height from the substrate and speed of the stage.

Additionally, the spinning of the substrate enhances the spread of the nano/micro-droplets ejecting from the spray nozzle. In current setup, there is no setup for the rotation and the substrates were kept on top of a plated support. Therefore, to enhance the spread further and make the thin film more uniform, the spray coated samples were immediately rotated at higher speeds as 3000 RPM by using a spin coater. As the metal pads are already covered with a scotch tape, the spreading of any existing solution from the desired spray coated area is not so critical to badly affect the device structure or performance. Substrate heating is not required for the deposition of the dielectric layer, due to the requirement of the final spinning of the substrate. Therefore, in this case not all the solvent is evaporated during the time of flight of the droplets from the nozzle nor after coming in contact with the substrate. An additional step to promote the adhesion and spreading of the solution on the plastic substrate and also on the Si microwires, plasma oxidation (20 % for 20 seconds) is performed before spraying the dielectric solution. Similarly, the metal pads are protected by putting a small piece of Polyimide

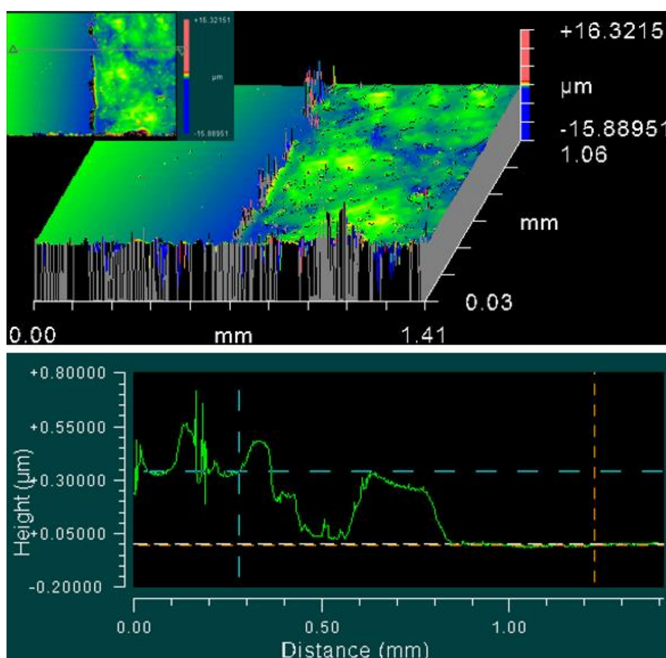

Figure 7.6. Thickness measurements using optical interferometer.

scotch tape on the edges of the contact pads and removed after completing the plasma and dielectric spray deposition.

A very thin solution is required for the spray coating which is prepared by using Silver paste (DuPont) by adding more surfactant solution. The standard thinner solution provided by supplier of the silver paste was used in ratios of 15 wt. % of the paste. In the case of flowable or low viscosity paste, these trenches act as micro-channels for the

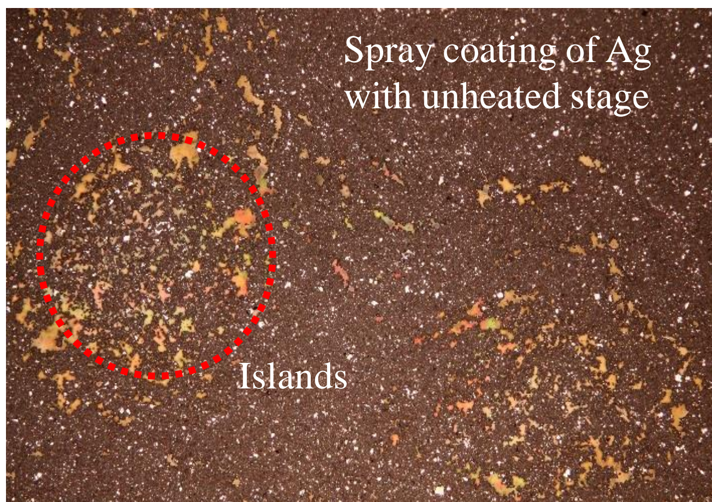

Figure 7.7. Spray coating of silver (Ag) on PI without introducing substrate heating

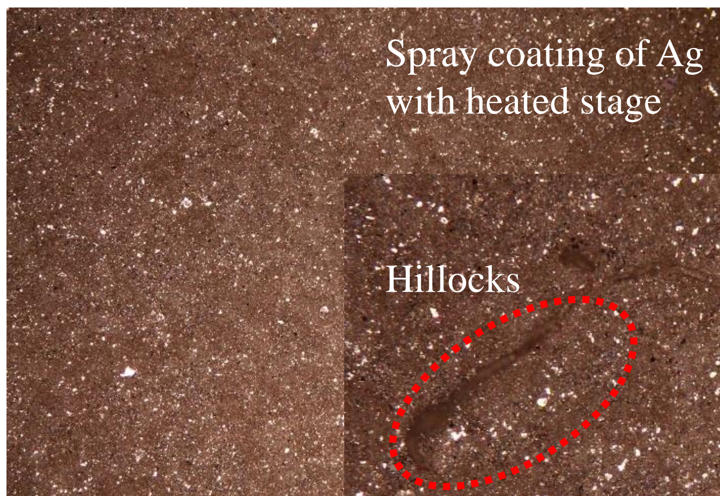

Figure 7.8. Spray coating of silver (Ag) on PI with substrate heating

paste to flow, which eventually may result in the short-circuiting of source and drain. This is one of the major issues experienced during our previous experiments [12, 21]. Two different solutions are foreseen here to address this issue - the first is to use the Si wires with reduced thickness (i.e. using SOI wafer with Si layer in nanometer) and the second is the quick solidification of spray-coated metals. The first solution comes with greater risk of thinner Si microwires breaking during the transfer-printing step. Partial sintering or instant solidification of spray–coated Ag paste, e.g. due to a heated substrate, can be used to avoid short-circuiting of source and drain. The latter option is also closer to rapid processing for large area flexible electronics.

A shadow mask developed from Brass as shown in Figure 7.5 (c), was used to realize the source and drain contacts. For the spray solutions, requiring a heated substrate, it is essential to use a reliable material, which can sustain higher temperatures. The shadow masks developed by using 3D printer are more suitable for coating dielectric materials, as no heating is required for them. However, the shadow masks developed by 3D printer are stack of plastic sheets adhered to each other by using glue. The plastic material of the shadow mask as well the glue does not sustain temperatures higher than 100 ^{o}C, and shrinks by deteriorating the desired structures on the mask. Therefore, to avoid this problem Brass was used as the hard shadow mask for the Ag patterned deposition. To keep the metal layers thin (~1µm.), the substrate was heated at around 120 ^{o}C so as to evaporate the surfactants immediately. This step ensures the deposition of metal layers with good control on the edges especially in the case of MISFETs made of array of Si microwires, as the trenches between the wires (Figure 7.1(a)) make the surface uneven.

Substrate heating is critical in case of metals deposition layers, in order the control the uniformity of the layer and maintain the same conductivities. Spray coating without heating the substrate results in a layer, which have islands because of the solution accumulation at specific locations on the substrate as shown in Figure 7.7. Subsequently, after sintering step of the silver, big voids are generated after complete evaporations of the solvent and surfactants creating islands of conductive grains. On the other hand, heating substrate while spraying results in a dried layer in real time as all the solvents are removed as soon as the droplets are deposited on the hot substrate as shown in Figure 6.8. A very thin conductive layer is possible to be deposited with maximum of two passes of the spray coating. The less number of spray passes are desired in this approach also to minimize wet-on-wet deposition, as multipasses can results in developing hillocks due to increased solution deposition and immediate sintering. These hillocks (shown in the inset of Figure 7.8) can result in short-circuiting if multi-layer structure is desired where multiple metals solutions are supposed to be deposited. Therefore, a single or a maximum of two passes of the metallic spray deposition is the preferred approach for such type of structures. This also helps in minimizing the solution wastages and reducing the overall cost of the materials.

Finally, a separate shadow mask is used to pattern Ag for the gate contact with good alignment to the channel area. Various steps related to spray coating were carried out within the thermal budget of PI substrate. For example, during spray coating the substrate was kept at 120 °C to ensure that the surfactants and solvents evaporate immediately after spray deposition of materials. Similarly, the sintering of Ag paste was carried out at 120 °C. The solvents used were also compatible with PI and SU-8, which is used here to adhere Si microwires on PI. As a result, uniform thin dielectric and metal contacts were deposited on Si microwires. The final assembled microwires and developed metal insulator field effect transistors based on multiple and single Si microwire are shown in Figure 7.9 (a & b) respectively.

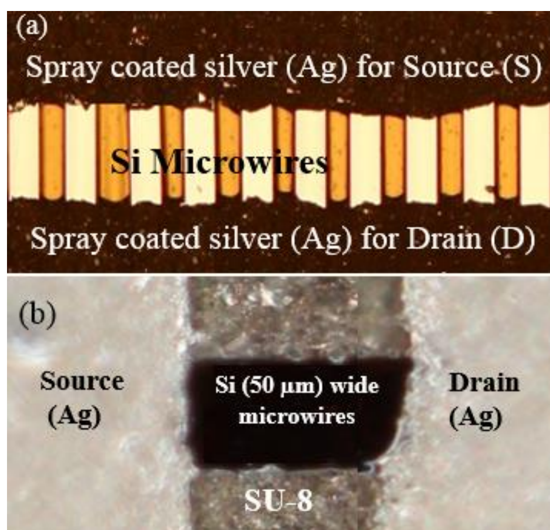

Figure 7.9. (a) & (b). Final assembly of MISFET devices developed from multiple and single Silicon microwires

7.4. Results and Discussions

The top-gate structures of MISFETs so obtained are mechanically robust as the materials on top of Si microwires prevent their dislocation or breakage. The fabricated FETs have channel length of ~30µm and channel width of 50µm for the single wire devices. The channel width increases 20 times for the array based devices. As the channel length depends on the resolution of printing tools, the device performance is linked to the printing resolution. As a result, small variations in dimensions during printing may lead to bigger variations and non-uniformity of response among similar devices. In this regard, the MISFETs based on array of Si microwires are expected to be better as dimensional variations are distributed over large number of wires, which then leads to lesser variations among device performances.

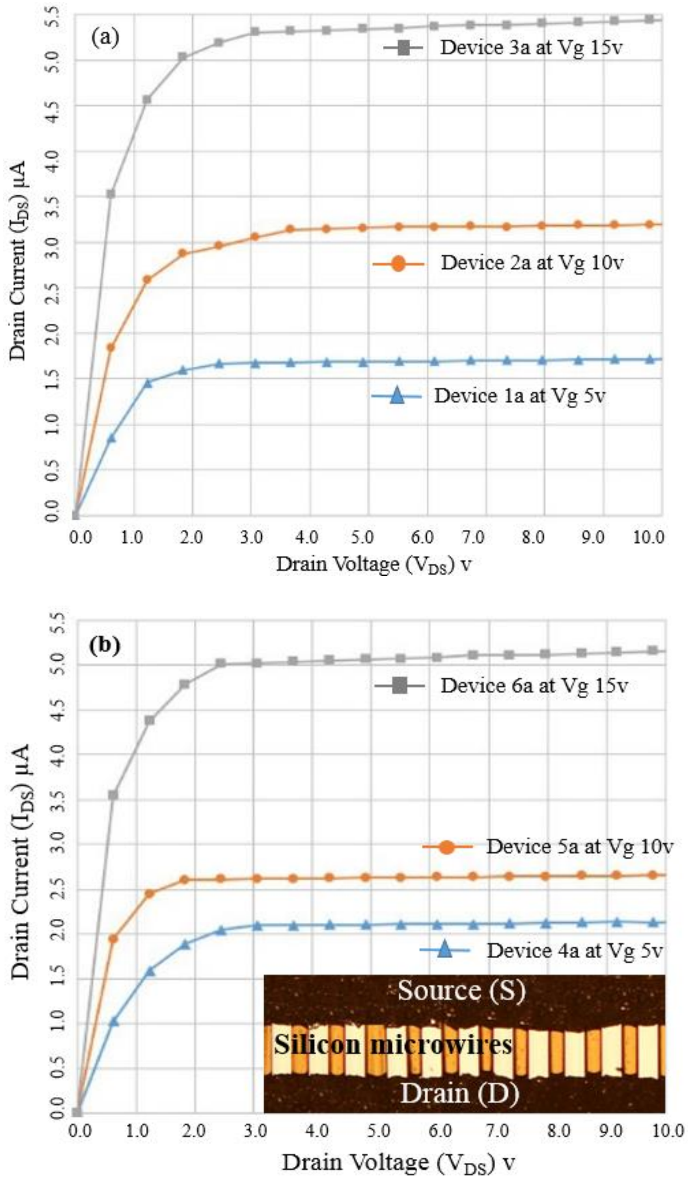

Figure 7.10. (a) and (b). Output response of MISFET devices made of Si multiwires with similar geometric parameters at different gate voltages.

After device fabrication, the bending tests were performed to inspect the mechanical

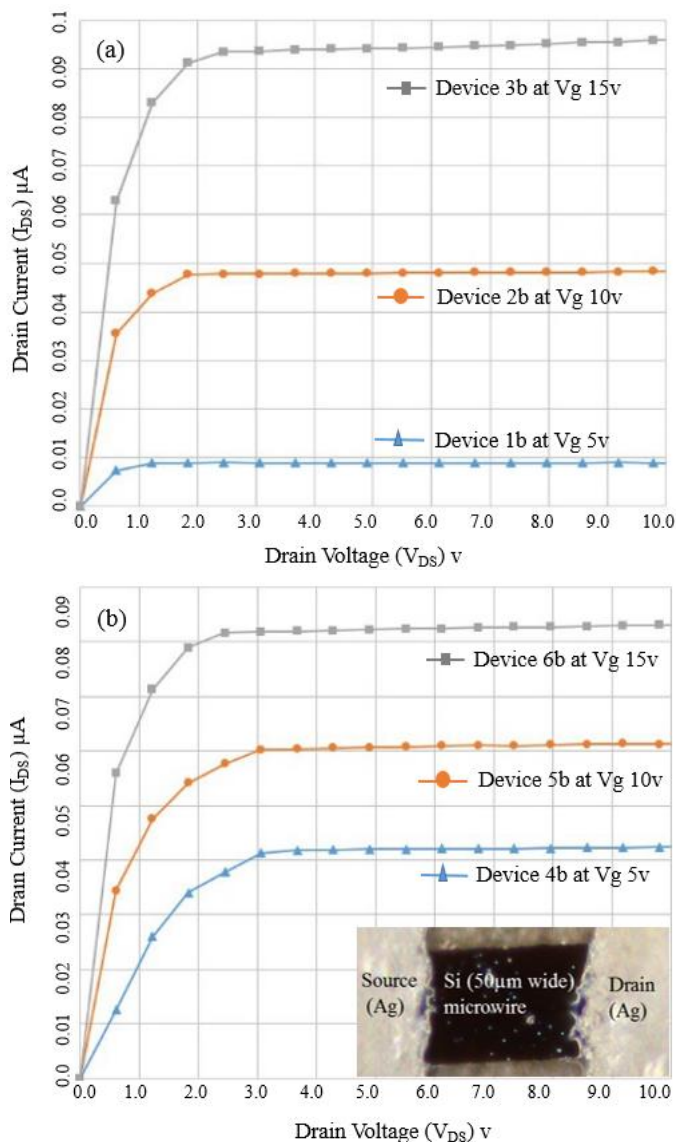

Figure 7.11. (a) and (b). Output response of MISFET devices made of Si single wires with similar geometric parameters at different gate voltages.

reliability of the structure and to investigate the adhesion-loss at the interface of Si microwires and SU-8. For this purpose, the structure was attached to a separate plastic sheet and wrapped around cylinders with different diameters of 8, 12 and 16 mm, which are revolved for 500 cycles. Bending test is critical for monitoring cracks caused by the stresses within the layers during the bending process. It is used also to check any dislocation or delamination of the wires from the adhesive layer. No crack or delamination was observed after repeated bending tests.

For electrical characterization, 12 devices (6 from each type, as described in Table 7.1) are evaluated in terms of drain current and threshold of onset voltages. A set of 2 devices from each group was investigated under similar gate voltage and the responses were compared for any variation. Figure 6.10 shows the output response of MISFETs based on array of 15 Si microwires. Figure 7.10(a) shows responses of devices 1a, 2a and 3a at different gate voltages. Figure 7.10(b) shows the response of other 3 similar devices (i.e. 4a, 5a and 6a) at similar characterization conditions. For device 1a in Figure 7.10 (a), the saturation threshold voltage for the onset is ~2.1V (VDS) and a drain current of ~1.75μA, whereas its corresponding device i.e. 4a in Figure 6.10 (b) has a threshold voltage at ~2.2V (VDS) and a drain current of 2.0μA. The difference in drain currents of these devices is 0.3 μA and the onset voltage difference is 0.1V. Similarly the threshold voltage for the onset of device 2a is 2.5V (VDS) and a drain current of 3.1μA while the onset voltage for its corresponding device 5a is 2.1V (VDS) and a drain current of 2.75μA. The corresponding devices 3a and 6a with similar structural parameters have a difference in the onset voltage of 0.4V (VDS) while the change in current response is about 0.2μA. Similarly, Figure 7.11 (a) and (b) show the variations in the drain current of the devices made of a single Si microwire. Comparison of the data extracted from both the graphs in Figure 7.10 and Figure 7.11 show an increased drain current with less variations among devices made of multiple Si microwires.

Table 7.1. Summary of the responses with corresponding device variations.

Relevant Devices	ΔV_{th} (v)	$\delta (V_{th})$	ΔV_{th} %	ΔI (μA)	$\delta (I)$	ΔI %
1a, 4a	0.1	0.07	4.65	0.25	0.18	13.33
2a, 5a	0.2	0.18	9.52	0.35	0.25	11.96
3a, 6a	0.1	0.07	3.27	0.15	0.11	2.76
1b, 4b	1.2	0.85	48.00	0.03	0.03	> 50.00
2b, 5b	0.6	0.43	22.33	0.01	0.07	18.18
3b, 6b	0.2	0.15	6.45	0.02	0.09	14.62

a, corresponds to the type of multiwires based MISFETs (1a, 4a), (2a, 5a) & (3a, 6a) are corresponding devices characterized at similar gate voltages.
b, corresponds to the type of single wires based devices (1b, 4b), (2b, 5b), and (3b, 6b) are corresponding devices at similar gate voltages.

Table 7.1 summarizes the net changes in the characterization values of the devices with standard deviation and percentage changes between corresponding values. Statistical analysis of the data in the graphs of Figure 6.10 and Figure 6.11 show mean values of 1.6, 2.4 and 1.9 for the threshold voltages of related devices i.e. (1a, 4a), (2a, 5a) and (3a, 6a) respectively for the multiwires based devices. Similarly, the mean values for the drain current of multiwires-based devices are 1.8, 2.9 and 5.3 respectively. On other hand, the mean threshold voltage values for the single Si microwire based devices i.e. (1b, 4b), (2b, 5b) and (3b, 6b) are 2.5, 2.7 and 3.1 respectively. The mean drain current values for the same set of devices are 0.03, 0.06 and 0.09 respectively. The standard deviation and the average change (in percentage) of threshold voltages for the multiwires-based devices is lesser as compared to the single wire counterparts, as shown in Table 7.1. It is observed that devices made of multiwires better mitigate the response variations. Further, they are more reliable, as any variations due to physical disruptions of a single wire within the array could be compensated by rest of the wires.

7.5. Conclusion

A new fabrication route, using conventional microfabrication technology and printing tools, is presented for development of transistors. Two types of MISFETs have been investigated to understand the types of device structures possible with presented methodology. It has been observed that devices with multiwires have better performance and lesser variations compared to single Si microwire based devices. The ensemble of multiple number of Si microwires are useful when these discrete devices are advanced to flexible circuits where variations in the device responses are desired to be as minimum as possible. Further improvement in the device performance is obvious by decreasing the width of microwires from 50 μm, which would result in increasing the aspect ratio and diminishing the overall size of the device. The spray coating in particular is a significant achievement within this research, as diverse solution based materials could easily be printed in a one-step process. The reliable processing of spray coating with minimum control parameters expand the use of Si microwires for a range of applications. Not only MISFET devices, the processing of several solution based organic transducer materials could be integrated with Si microwires for diverse sensing applications. We conclude that devices using arrays of Si microwires are less prone to printing related dimensional variations and have better reliable performance compared to devices with single microwire.

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Chapter 8
Conclusion

8.1. *Conclusion*

In this research work, an investigation towards the mergence of three potential printing technologies have been carried out for developing electronics on polymeric substrates. These hybrid electronic components are fabricated by integration of diverse organic and inorganic materials in the form of thin films. A feasible technological platform is established, where Si microwires could easily be merged with the thin films of organic dielectric and conducting materials. These diverse, solution based and dry transfer printing technologies have been utilized for fabrication of flexible electronics by successful demonstration of prototype devices on PET and PI substrates. The advancements made toward the fabrication route of large area flexible devices and feasible integration of transfer printing, spray coating and screen-printing technologies have been highlighted within this research.

Screen-printing is the exceptional fabrication scheme, which has been explored in the first part of the thesis for rapid prototyping of metal contacts and large area pressure sensors. The screen-printed metal contacts are used for the back-gated MISFETs, where Ag paste is printed prior to deposition of an adhesive layer for the Si microwires transfer. An all screen-printed fabrication route has been potentially explored for fabrication of two types of pressure sensors. In both the variants, flexible pressure sensors are in the form of segmental arrays of parallel plate structure - sandwiching the piezoelectric polymer Polyvinylidene Fluoride Trifluoroethylene (P(VDF-TrFE)) between two printed metal layers of silver (Ag) in one case and the piezoresistive (Multiwall Carbon Nanotube (MWCNT) mixed with Poly(dimethylsiloxane (PDMS)) layer in the other. The screen-printed piezoelectric sensors array exploit the change in polarization level of P(VDF-TrFE) to detect dynamic tactile parameter such as contact force. Similarly, the piezoresistive sensors array exploits the change in resistance of the bulk printed layer of MWCNT/PDMS composites.

Transfer printing of Si as the semiconductor layer has been introduced to fabricate active devices on polymeric substrates, is investigated in the second part of the thesis. The transfer printing technique is optimized by introducing stress intensifiers and an extra over-etching technique, which resulted in enhanced transfer yield in both the transfer steps of Si microwires, from donor wafer onto secondary polymeric substrates. Both the dry transfer printing techniques i.e. flip-over and stamp-assisted transfer are evaluated on the basis of current response and junction formation with conductive patterns in MSM structures. The better response of stamp-assisted transfer printing has been pursued for fabrication of MISFET devices on PET and PI substrates. Spray coating is a step further towards easy and reliable manufacturing of hybrid flexible electronics by incorporating Si microwires within thin layers of organic dielectrics and metallic conductors. Spray coating with the help of shadow masks prepared by using a 3D printer and a milling machine are used to deposit the organic dielectric and

patterning of metallic contacts for the source and drain for MISFETs. Spray coating offers the innovative features to the fabrication platform that help in rapid deposition of diverse solution based materials with repeatable coating parameters. Additionally the MISFET responses are characterized by including a single and multiple Si microwires in the device architecture. Based on the results obtained by including both single and multiple Si microwires, it is concluded that MISFETs based on multiple Si microwires have less response variations compared to MISFETs made of a single Si microwire.

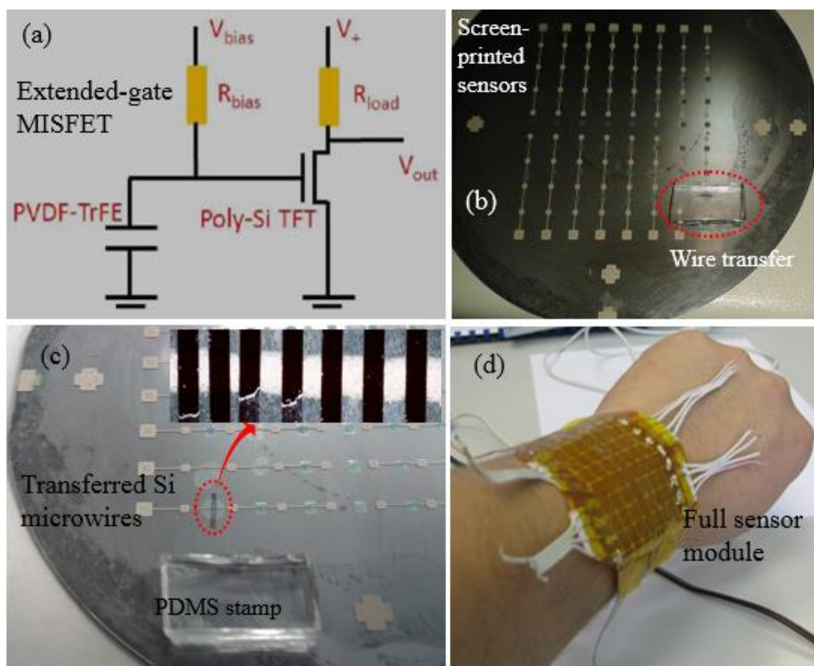

Figure 8.1. Future scope of current research achievements, (a) Schematic of an extended gate MISFETs connected to a sensor, (b) Screen-printing of large area tactile/pressure sensors, (c) Transfer printing Si microwires on the extended gate area, (d) Full sensor modules and patches.

8.2. Future Outlook

The exceptional growth of printed and flexible electronics have been witnessed in recent years for diverse applications. Although rapid advancements have been observed in various fields of the flexible electronics, still there is a lot of room for development of reliable manufacturing platform by harvesting potentials of different printing technologies. Electronic skin (e-skin) is one of the various exciting applications of large area flexible electronics, where the sensor patches are desired to be mounted conformably on a robot body or on prosthetic limbs. This will revolutionize the artificial

intelligence by making robots (industrial and social) more interactive. This technological platform developed by merging the three different potential printing technologies is aimed for development of such large area sensor patches as shown in Figure 8.1 (c & d). Utilizing a single fabrication technique is always hindered by intrinsic properties of the materials (organic and inorganic), processing conditions (temperatures and vacuum environment) and the substrates used for developing electronic systems on top of the surface. Hybrid thin film (organic and inorganic) devices have got the opportunity to shape up for getting large area electronics devices that can effectively be used and merged in different odd structures.

The next step of this research project is to utilize the fabrication platform and bring together the discrete devices i.e. MISFETs and large area pressure sensors on a single foil for developing an active pressure mapping system. Therefore, achievements in this research have a strong potential to be advanced further towards heterogeneous integration of devices made of organic and inorganic materials. To utilize effectively and bring all the devices on a single foil would provide an attractive opportunity to get the benefits from both the streams of materials. For instance, Si microwires based devices would provide fast switching or signal conditioning electronics whereas solution based materials would help in bringing down the overall cost of the system. The final patches are planned to be developed by following an extended gate structure (Figure 8.1 (a)); where the bottom electrode of each sensor is coupled as a back gate for the transferred Si microwires (Figure 8.1 (b & c)) based MISFETs. Preliminary experiments have been performed in this direction and a prototype patch is demonstrated as shown in Figure 8.1.

Scientific Production

Submitted and in progress

1. **Saleem Khan**, Leandro Lorenzelli and Ravinder Dahiya "Flexible MISFETs Developed from Transfer Printed Si Microwires and Spray Coating" **IEEE. Elect. Dev. Soc.**, Under Review.
2. **Saleem Khan**, Leandro Lorenzelli and Ravinder Dahiya "Recent Advances of Conductive Nanocomposites for Flexible Sensors and Electronic Skin Applications", In Review.

Published

1. **Saleem Khan**, Nivasan Yogeswaran, William Taube, Leandro Lorenzelli and Ravinder Dahiya, "Fabrication route to embed ultrathin Si μ-wires in solution-processed layers for flexible FETs", **J. Micromech. Microeng**. 25 (2015) 125019 (10pp).
2. **Saleem Khan**, Wenting Dang, Leandro Lorenzelli and Ravinder Dahiya, "Flexible Pressure Sensors based on Screen Printed P(VDF-TrFE) and P(VDF-TrFE)/MWCNTs" **IEEE, Trans. on Semiconductor Manufacturing**, Vol. 28, No. 4, (486-493), 2015.
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9. Nivasan Yogeswaran, **Saleem Khan**, Wenting Dang, Emre Ozan Polat, Leandro Lorenzelli, Vincenzo Vinciguerra and Ravinder Dahiya, “Tuning Electrical Conductivity of CNT-PDMS Nanocomposites for Flexible Electronic Applications” **IEEE Nano**, Rome, Italy, 2015.
10. Cristian Collini, Valentina Prusakova, **Saleem Khan**, Giuseppe Resta, Leandro Lorenzelli, Sandra Dirè, “Development of microfabrication technologies enabling the realization of memristor-based devices and building blocks for logic circuits”, **NanotechITALY**, Bologna, Italy, 2015.
11. Wenting Dang, **Saleem Khan**, Leandro Lorenzelli1, Vincenzo Vinciguerra and Ravinder Dahiya, “Stretchable Interconnects using Screen Printed Nanocomposites of MWCNTs with PDMS and P(VDF-TrFE)”, **11th IEEE PRIME**, Glasgow, UK, 2015.
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13. Stuart Hannah, Helena Gleskova, **Saleem Khan** and Ravinder Dahiya, “Response of P(VDF-TrFE) Sensors to Pressure and Temperature”, **11th IEEE PRIME**, Glasgow, UK, 2015.

Participation to Congresses, Schools and Workshops

Conferences

ASMC 2014, IEEE-PRIME 2014, ESSDERC 23rd Sep 2014, IEEE-Sensors Nov 2014, MSCA Nov 2014, AISEM 2015, IEEE PRIME 2015.

Workshops and Seminars

Workshop on Silicon Photonics: Recent Advances (Univ. of Trento), Workshop on Advances in Photovoltaics (Univ. of Trento), Seminar on Flexible Electronics Technology (Univ. of Trento), ICT Days 2014, Univ. of Trento.

Secondments at Partner Institutes

1. Secondment at Fraunhofer EMFT, Munich, Germany
   - ❖ Activity: Roll-to-Roll screen-printing, ESD Test, Physical Reliability and Life Cycle Tests.
2. Secondment at Technical University Munich TUM, Germany
   - ❖ Activity: Spray Deposition of CNTs for Sensors, Characterization of the Sensors.
3. Secondment planned at University of Glasgow.
   - ❖ Activity: Nanofabrication, Inkjet Printing, Physical & Electrical characterization of flexible electronics.

Summer Schools

1. 2nd International Summer School on Smart Materials & Structures, July 22-26, 2013, Trento, Italy.
2. “Flexible Sensors and Electronics-Materials Methods & Technologies” 11-13 Sept. 2013, Catania, Italy.
3. Joint Summer School of the European Projects CONTEST–OLIMPIA–EAGER on “System Integration”, May 26– 28, 2014, Fraunhofer EMFT, Munich, Germany.
4. ITN Marie Curie Joint Summer School CONTEST PROTOTOUCH, UNIVERSITÉ LILLE1, France 18-22, MAY 2015

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