

**International Doctorate School in Information and  
Communication Technologies**

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**CMOS READOUT INTERFACES FOR MEMS  
CAPACITIVE MICROPHONES**

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## Abstract

*This dissertation demonstrates the feasibility of three novel low-power and low-noise schemes for the readout interfaces of MEMS Capacitive Microphones (MCM) by presenting their detailed design descriptions and measurement results as application-specific ICs (ASIC) in CMOS technology developed to exploit their application scope in consumer electronics and hearing aids. MCMs are a new generation of acoustic sensors, which offer a significant scope to improve miniaturization, integration and cost of the acoustic systems by leveraging the MEMS technology. Electret-Condenser-Microphones (ECM) are the current market solution for acoustic applications; however, MCMs are being considered as the future microphone-of-choice for mobile phones in consumer electronics and for hearing aids in medical applications. The readout interface of MCM in an acoustic system converts the output of the MEMS sensor into an appropriate electrical representation (analog or digital). The output of a MCM is in the form of capacitive-variations in femto-Farad range, which necessitates a low-noise signal-translation employed by the readout interface together with a low-power profile for its portable applications. The main focus of this dissertation is to develop novel readout schemes that are low-noise, low-power, low-cost and batch-producible, targeting the domains of consumer electronics and hearing-aids. The presented readout interfaces in this dissertation consist of a front-end, which is a preamplifier, and a backend which converts the output of the preamplifier into a digital representation.*

*The first interface presents a bootstrapped preamplifier and a third-order sigma-delta modulator (SDM) for analog-to-digital conversion. The preamplifier is bootstrapped to the MCM by tying its output to the sensor's substrate. This bootstrapping technique boosts the MCM signal by  $\sim 17$ dB and also makes the readout insensitive to the parasitic capacitors in MCM electro-mechanical structure, achieving 55dBa/Pa of SNDR. The third-order low-power SDM converts output of the PAMP into an over-sampled digital bitstream demonstrating a dynamic-range (DR) of 80dBa. This ASIC operates at 1.8V single-supply and 460uA of total current consumption; thus, highlighting the feasibility of low-power integrated MCM readout interface. This ASIC is also acoustically characterized with a MCM, bonded together in a single package, demonstrating a reasonable agreement with the expected performance.*

*The second interface presents a readout scheme with force-feedback (FFB) for the MCM. The force-feedback is used to enhance the linearity of the MCM and minimize the impact of drift in sensor mechanical parameters. Due to the unavailability of the sensor, the effect of FFB could not be measured with an MCM; however, the presented results point out a significant performance improvement through FFB. The preamplifier in this ASIC utilizes a high-gain OTA in a capacitive-feedback configuration to achieve parasitic insensitive readout in an area and power -efficient way, achieving 40dBa/Pa of SNDR. The digital output of the third-order SDM achieved 76dBa of DR and was also used to apply the electrostatic FFB by modulating the bias voltage of the MCM. A dummy-branch with dynamic matching converted the single-ended MCM into a pseudo-differential sensor to make it compatible with force-feedback. This interface operates at 3.3V supply and consumes total current of 300uA.*

*The third interface presents a chopper-stabilized multi-function preamplifier for MCM. Unlike typical MCM preamplifiers, this preamplifier employs chopper-stabilization to mitigate low-frequency noise and offset and it also embeds extra functionalities in the preamplifier core such as controllable gain, controllable offset and controllable high-pass filtering. This preamplifier consists of two stages; the first stage is a source-follower buffering the MCM output into a voltage signal and the second-stage is a chopper-stabilized controllable capacitive gain-stage. This preamplifier employs  $M\Omega$  bias resistors to achieve consistent readout sensitivity over the audio band by utilizing the miller effect, avoiding the conditionally-linear  $G\Omega$  bias resistors. The offset control functionality of this preamplifier can be used to modulate idle tones in the subsequent sigma-delta modulator out of the audio-band. The high-pass filtering functionality can be used to filter-out low-frequency noises such as wind-hum. This preamplifier operates at 1.8V and consumes total current of 50u with SNDR of 44dB/PA, demonstrating the feasibility of a low-power low-noise multifunction preamplifier for the MCM sensor.*

### Keywords

MEMS Capacitive Microphone, Silicon Microphone, Condenser Microphone, Low-Noise Preamplifier, Readout Interface, Sigma-Delta Modulator, Force-Feedback.



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## List of Abbreviations

MEMS Capacitive Microphone	MCM
Complementary Metal Oxide Semiconductor	CMOS
Micro-electro-mechanical System	MEMS
Application Specific Integrated Circuit	ASIC
Integrated Circuit	IC
Readout Interface	RI
Preamplifier	PAMP
Analog-to-Digital Converter	ADC
Sigma-Delta Modulator	SDM
Electret Condenser Microphone	ECM
Sound-Pressure-Level	SPL
Backplate	BP
Moving membrane (diaphragm)	MM
Substrate	SUBS
Discrete-Time	DT
Continuous-Time	CT
Capacitance-to-Voltage	C-to-V
Oversampling Ratio	OSR
Source-Follower	SF
Noise Transfer Function	NTF
Signal Transfer Function	STF
Dynamic Range	DR
Signal-to-Noise Ratio	SNR
Signal-to-Noise-and-Distortion Ratio	SNDR
Transconductance	gm
Unity Gain Bandwidth	UGBW
Figure of Merit	FOM
Operational Transconductance Amplifier	OTA
Common-mode Feedback	CMFB
Common-mode Transfer Function	CMTF
Bandgap	BG
Charge-pump	CP
Force-feedback	FFB
Double-Poly Quad-Metal	2P/4M
femto-Farad	fF
pico-Farad	pF
Chopper Stabilization	CHS
Correlated Double Sampling	CDS
Decibel A-weighted	dBA
Offset Control Circuit	OCC
Decibel Full-Scale	dBFS
Focused-Ion-Beam	FIB
MIM	Metal-Insulator-Metal

# Chapter 1

## Introduction

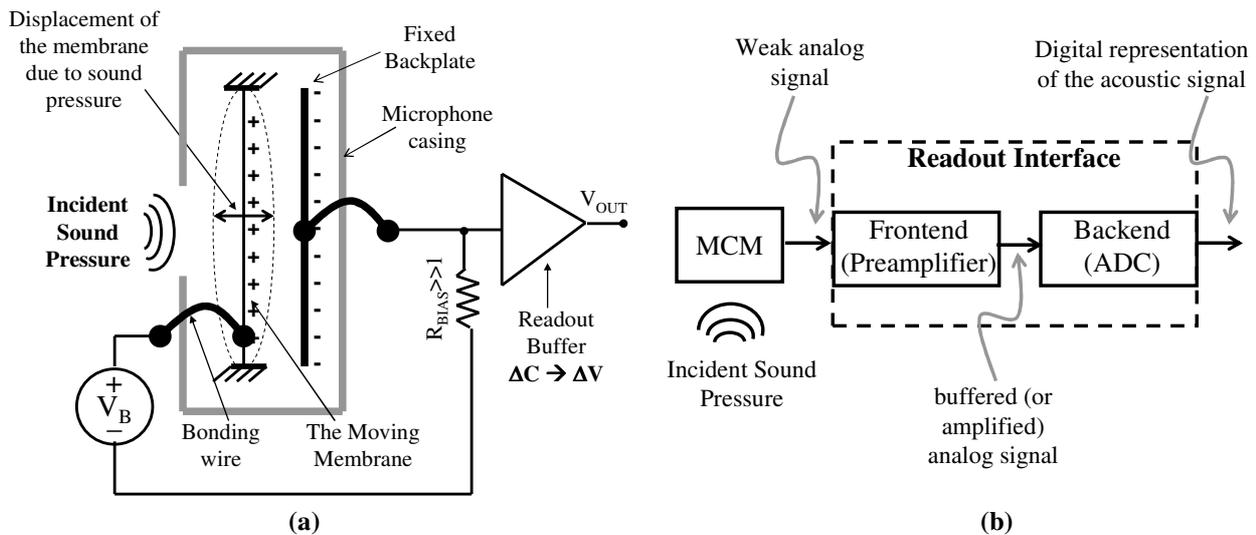
Microphone sensor has evolved through several phases since its invention in 1876. The carbon-microphones developed in 1878 were the essential ingredient of the early telephone systems. Ribbon-microphones were invented in 1942 for radio-broadcasting. The introduction of a self-biased condenser microphone in 1962, i.e. the Electret-Condenser-Microphone (ECM), combined high-sensitivity and broad frequency-range features with low-cost [1]. ECMs have been the microphone-of-choice for high-volume applications with a production of almost 1 billion parts per year. Nearly 90% of all microphone produced currently are ECMs [2]. The first condenser microphone based on silicon micro-machining was introduced in 1983, also known as the first MEMS capacitive microphone (MCM). MCM offered a whole new scope of system miniaturization and integration by leveraging the MEMS technology. With the desire for more functionality integrated in a compact system, MEMS capacitive microphones are now being proposed to become the microphone-of-choice for consumer applications [2]. The applications for the microphone sensors can be found in consumer electronics, medical domains, sound recording and broadcasting, telephony and recently in industrial and automobile domains [3]. However, the two major areas that are driving interest in MEMS microphones are hearing aids and consumer electronics. For hearing aids, the size of the overall system and the integration with digital signal processing are the critical factors. While the consumer electronics is driven by the desire of an integrated system with added-functionalities and reduced cost [4].

MCMs offer several improved aspects over the ECMs. MCMs are smaller in size, compatible with high-temperature automated PCB mounting process and are less susceptible to mechanical shock. Furthermore, the possibility of monolithic integration of the sensor with the CMOS electronics is another major advantage towards a robust and cost-effective system, enabling the micro-system to take advantage of both electrical and mechanical properties of silicon [9]. Due to their smaller foot-print, applications where an array of acoustic-sensor is needed are also becoming perceivable [6,7]. MEMS microphones employ different transduction principles such as piezoelectric, piezoresistive and optical detection [8]. However, 80% of the produced MEMS microphones utilize capacitive transduction since it achieves higher sensitivity, consumes low-power and is more inline with batch production [10].

MCM is an electro-acoustic transducer realized to detect airborne sound pressure, primarily consisting of two electrodes; one is fixed while the other is moveable [9]. The electro-mechanical structure of MCM is polarized to store a certain amount of bias charge. This bias charge gives rise to a capacitance between the two electrodes and air between the electrodes serves as dielectric. The deflection of the moveable electrode, due the incoming sound pressure, changes the inter-electrode gap, thereby changing

the inter-electrode capacitance, which is detected and readout as a voltage, current or frequency -signal by the readout-interface (RI) of the MCM. Figure 1-1a shows a typical scheme to readout the capacitive variations in MCM. Figure 1-1b shows a block-level representation of a typical RI for MCM, partitioned in front-end and backend. Front-end of the RI usually employs a preamplifier, feeding the backend which subsequently converts the analog signal into a digital representation.

The capacitive variations in MCM are directly related to strength of the incident sound pressure, where sound pressures are expressed in Sound-Pressure-Level (SPL). Sound pressure of  $20\mu\text{Pa}$  represents  $0\text{dB-SPL}$  and it is the auditory threshold, i.e. the lowest level a human ear can detect of a  $1\text{kHz}$  signal [11]. The typical sound-pressures are very weak as compared to the atmospheric pressure ( $101.3\text{kPa}$ ). The sound pressure levels of a face-to-face conversation range between  $60\text{dB-SPL} - 70\text{dB-SPL}$ . The sound-pressure goes up to  $94\text{dB-SPL}$  if the speaker is at a distance of one-inch from the listener, which is close to the case when talking into the microphone of a mobile phone [12]. Sound pressure level of  $94\text{dB-SPL}$  corresponds to  $1\text{-Pascal}$  and is used as a reference for acoustic applications. The performance pointers (such as SNR) for acoustic systems are typically specified for  $1\text{Pa}$  and  $1\text{kHz}$  signal. This highlights that the acoustic system, i.e. the MCM with the RI, should have a high sensitivity to detect weak acoustic signals.



**Figure 1-1 : (a) A typical scheme to readout the capacitive variations in a MEMS Capacitive Microphone, (b) A generic functional partitioning of the Readout Interface**

For an optimal design of the acoustic system, the readout interface must be tailored and design-approaches be customized accordingly for MCM sensors. This puts forward a multifaceted design task for the readout interface because of the following reasons: (1) The weak capacitive variations from the MCM necessitate a low-noise readout with an adequate integration with the electronics to minimize parasitic interconnect loading. (2) Since most of the applications of MCM are in battery-operated devices [1-4], low-power consumption is an implicit requirement for the readout electronics. (3) Moreover, the micro-mechanical structure of the sensor has an optimal range of operation beyond which it violates linearity and stability specifications. Therefore, the main challenges for the RI of MCM are to address the low-

power and low-noise design paradigms together with the development of a miniaturized and low-cost readout scheme suitable for high-volume production. The RI also has to follow the trend of having added functionalities while improving the compactness and reducing the cost of the system. Therefore, while a constant progress is made on the development of better sensors, a parallel effort on the RI development for MCMs is imperative, which can couple up with the evolving sensor features and application requirements, giving rise to an integrated acoustic system fully exploiting the technology at hand.

This dissertation focuses on the development of low-noise and low-power electrical readout interfaces in CMOS for MEMS capacitive microphones. The targeted domain lies in the portable acoustic applications, such as mobile phones and hearing aids, where a precise balance must be struck among performance, power and cost of the system. The reason behind opting for CMOS is based on the fact that it is a well-characterized and low-cost technology extensively used for high-volume IC production. Furthermore, micromachining uses similar processing techniques as CMOS for MCM fabrication; therefore, enabling a high-degree of integration and miniaturization of the whole system on the same wafer. The design methodology adopted in this dissertation involves literature review and establishing a proof-of-concept based on simulations, followed by custom mixed-signal integrated circuit design, eventually leading to the electrical and acoustic testing of the electric RI ASIC. It is important to note that the design of RI front-end is strongly dependent on the characteristics of the MCM sensor. Consequently, the resulting design of the front-end affects the backend. Therefore, to build an optimal RI based on a goal-oriented approach, it is important to understand the relevant sensor characteristics from the perspective of readout interface. Therefore, the literature review is extended to include the material explaining electromechanical properties of the MCM. For the purpose of broadening the literature review on the readout interface, this dissertation perceives the RI partitioned into its major functional blocks. Subsequently, the relevant knowledge-base on each of the functional block is searched not only in the already-existing MCM-based systems, but also from other similar capacitive sensor systems. This enables the literature review phase to benefit from profuse literature and techniques available on other similar capacitive sensors.

This dissertation presents design and measurement results of three readout interfaces for MCMs, organized in five main chapters. The organization of this document is based on the chronological order of the study and design activities carried out during this research. Following the same sequence helps in developing an incremental sense of understanding in which the later work infers knowledge from the earlier work. The second chapter starts with a review of the MEMS microphone from a structural and technological perspective, highlighting its major characteristics, which should be understood for developing its electrical interface. It is followed by exhaustive literature review on the major functional components of the electrical interface. The third chapter presents the design details and measurement results for the first readout interface (Interface-I), which was designed in collaboration with ST Microelectronics, Milano. This interface consists of a Preamplifier (PAMP), a Sigma-Delta Modulator (SDM), integrated biasing and digital control, converting the capacitive variations of MCM into an over-sampled digital bitstream. This interface employs a modified bootstrapping approach to achieve a parasitic insensitive readout. Elec-

trical and acoustical characterization of this interface highlights the feasibility of an integrated low-power and low-noise readout interface for MCM. The fourth chapter presents the second readout interface (Interface-II), consisting of a charge-amplifier based topology PAMP and a third-order SDM, moreover, embedding force-feedback (FFB) functionality for the MCM within the interface. The presented simulation and measurement results demonstrate that FFB can be applied to improve the linearity, stability and mechanical imperfections in MCM. FFB is commonly employed for other MEMS capacitive sensor such as accelerometers; however, its application to MCM is not so frequent. This is due to the single-ended structure of the MCM sensors. This chapter demonstrates that FFB can be viably applied to single-ended MCMs, achieving considerable improvements in the performance. The fifth chapter presents design and measurement results of a multi-function preamplifier for MCMs (Interface-III), which was designed in collaboration with Analog-Devices, Denmark. The typical PAMPs for MCMs are straightforward capacitance-to-voltage buffers and switched offset and noise cancellation techniques are also not commonly employed by MCM PAMPs. This PAMP employs chopper-stabilization to enhance the noise performance and embeds extra functionalities within the PAMP, such as gain-control, offset-control and high-pass filtering, highlighting the feasibility of a multifunction PAMP for MCMs. The last chapter of this dissertation presents a comparative discussion on the presented approaches in the light of achieved results and also briefly addresses the issues for the future research activity.

# Chapter 2

## State of the Art and Background

The reviewed literature in this dissertation is partitioned into several sections for reasons that are discussed below. The first section presents a review of the applications, available technology and structure of the MEMS microphone sensor. The second section provides an exhaustive review of state-of-the-art literature on the major functional components inside a readout interface for a MEMS microphone. These components include preamplifier (PAMP), analog-to-digital converter (ADC), biasing network and digital control logic. The PAMP and ADC define the main characteristics of the readout interface while the other components play a supporting role. Therefore, a separate state-of-the-art review is presented only for PAMP and the ADC, however, the latest literature on the other components is referred to while describing their design details in the following chapters. The third section provides literature review for force-balancing techniques through which the readout interface can be used to affect sensor's electro-mechanical properties by enclosing it inside an electro-mechanical loop. To develop a readout interface for the MCM that achieves a balance among power, performance and cost, the main characteristics of the sensor must be understood from the RI perspective; therefore, a brief review of the sensor is necessary. The mechanical, structural and technological aspects of the MCMs are briefly reviewed in the following section; however, the focus remains on an interpretation that is needed to be understood for RI design of an MCM. This partitioning of the literature review is shown in figure 2-1.

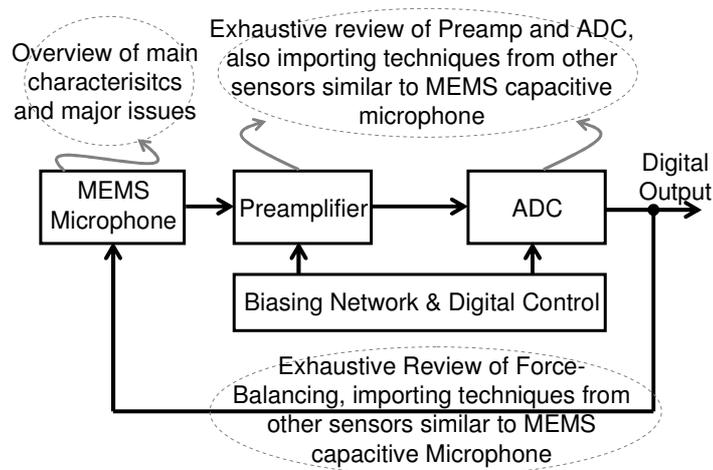


Figure 2-1 : Partitioning of the Reviewed State-of-the-art

Electret-Condenser-Microphones (ECMs) are the current market standard for high-volume acoustic applications, details on ECMs can be found elsewhere [13]. Condenser Microphones detect sound-pressures by detecting capacitive-changes between a mobile-diaphragm and a fixed backplate. A high voltage should be applied as a condenser polarizing voltage. In ECMs, this polarizing voltage is stored inside the sensor using a pre-charged Electret layer. MCMs are the variants of condenser microphones in which the capacitive structure is implemented using MEMS technology. MCMs are gradually replacing ECMs in different applications due to their improved characteristics in certain aspects. These improved characteristics include reduced drift in parameters with temperature, better immunity to mechanical shock, compatibility with standard high-temperature PCB mounting process, which minimizes the manual intervention required for sensor's integration on the PCBs and consequently decreases the overall cost of the system. However, the two major advantages include a smaller foot-print of the sensor that allows a miniaturization of the whole system, and the other is the increased degree of integration with the associated electronics in a single die, since the MEMS capacitive sensor is based on silicon-micromachining.

Therefore, driven by their improved features and the scope of the applications, MCMs are currently an active area of research, which is progressively maturing [14]. There is an eminent drive towards further optimization and miniaturization of the sensor itself, along with a parallel development of suitable low-noise and low-power methods of interfacing that should also contain extra functionalities such as configurability or adaptability [3,4]. However, most likely due to the current market scope, the research results are being held-back and there exists a scarcity on the publicly available literature on MCMs. This evolving research trend for MCMs and the lack of publicly available literature can benefit from the knowledge-base available for other similar sensors that have been extensively researched and profuse literature is available on them, e.g. MEMS capacitive accelerometers. To import the relevant knowledge-base from other sensors, it is more appropriate to partition the system into its major functional blocks and consequently import the literature for each component. The major functional components of the RI that are of major concern to this work are preamplifiers, analog-to-digital converters and the force-feedback logic.

Figure 2-2a depicts the evolving application domains of the MCM; dark spheres signify established applications, while lightly-shaded spheres represent recently emerging applications [7,15-17]. Six out of top thirty MEMS manufacturers are involved in MEMS microphones based systems (ADI, Infineon, Panasonic, Knowles, Avago-Tech and Omron) [3]. Market reviews [3,14] predict that MEMS microphone will be pre-dominantly applied to mobile phones and hearing-aids till 2011 followed by their application in other areas of consumer electronics, such as headsets and notebooks. World market of hearing aids had a volume of 6 million/year in 1998 [4] and 8 million/year MEMS microphone based hearing aids are expected by 2010 [17]. Figure 2-2(b) shows the expected growth for MCMs till 2010.

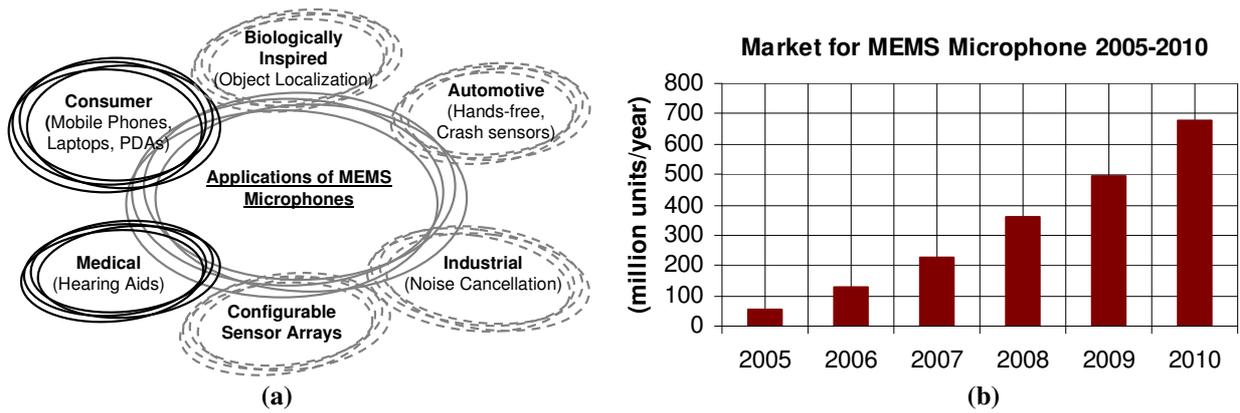


Figure 2-2 : (a) Applications domains of the MEMS Microphone, (b) Predicted growth in MEMS Microphone Market Shares

## 2.1. Overview of the MEMS Microphone Sensor

To explain the main characteristics and major issues of a MEMS capacitive microphone from the perspective of its RI, IRST-MCM is taken as a case-study, which is shown in figure 2-3a [9]. The available literature does not provide enough insights to the sensor-specific issues that the RI might confront. Furthermore, although the designed readout interfaces are compatible with any generic MCM; however, their specifications are derived from the IRST-MCM characteristics.

The MCM shown in figure 2-3a is designed by means of a single-wafer fabrication technology, combining bulk and surface micromachining techniques [9]. There is a perforated membrane with acoustic holes in it, which serves the purpose of a fixed backplate (BP). Due to acoustic holes, it is insensitive to incident acoustic pressure. The other membrane, termed as moving-membrane (MM), is attached to the substrate through springs, and it vibrates with the incident sound pressure. This structure is enclosed in a case, termed as back-chamber. The MM in IRST microphone is stiffened by vertical ribs, to mimic a rigid piston-like movement with a lighter diaphragm, which allows the whole membrane to contribute to the signal transduction [9]. In this dissertation, the characteristics of the IRST MEMS microphone, listed in table 2-1, are used as one of the main driving specifications for the readout interface design and are referred later in the text.

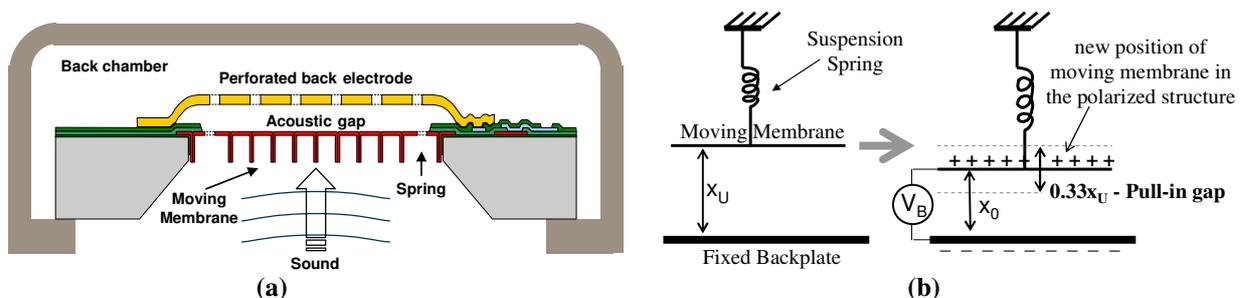


Figure 2-3 : (a) Cross-section of IRST MCM, (b) Simplified representation of the MCM mechanical structure, unbiased and biased

**Table 2-1 : Main Characteristics of IRST MEMS Capacitive Microphone**

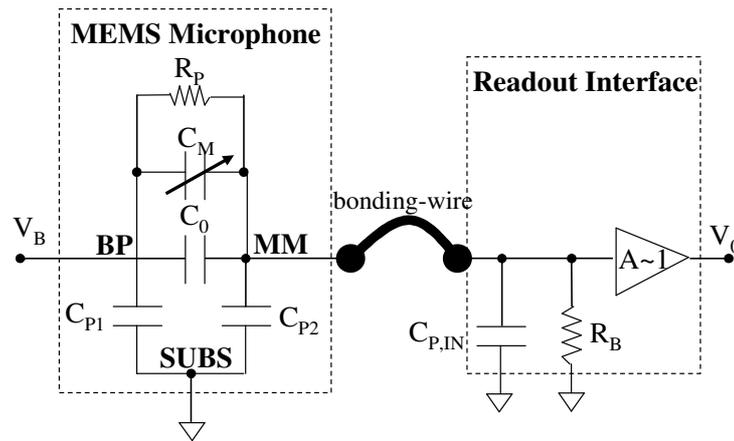
IRST MCM Characteristics	
Effective Area of the MM	0.25mm <sup>2</sup>
Volume of Back-Chamber	0.4 mm <sup>3</sup>
Inter-Electrode Gap	1.6μm
Pull-in Voltage	10V
Sensitivity @ 1Pa, 1kHz	4.2mVpp (-53dBV/Pa)
Parasitic Capacitors in the MCM	
- Back-plate to Substrate Parasitic Capacitor	30pF
- Moving Membrane to Substrate Parasitic Capacitor	3pF
- DC-bias Parasitic Capacitor between MM and BP	6pF

The capacitive microphone sensor is biased using  $V_B$ , as shown in figure 2-3b. This polarization stores a certain amount of bias-charge in the capacitive structure and biases the sensor at the targeted readout sensitivity. The readout sensitivity can be defined as the ratio between the readout-voltage (or current) and the capacitive variation in the MEMS due to sound pressure. The electrostatic force due to polarization deflects the moving membrane from its equilibrium position ( $x_U$ ) to a new position  $x_0$ , where it is eventually counter-balanced by the spring restoration force. When the moving membrane moves due to the acoustic pressure in this polarized structure, the inter-electrode capacitance changes and is readout by the RI.

The attractive electrostatic-force, between the two electrodes, increases quadratically as the inter-electrode gap decreases. Whereas, the mechanical restoration force of the spring, which is keeping the electrodes apart, increases by first order of the displacement [20]. Therefore, after a certain displacement threshold, the electrostatic force cannot be further counter-balanced by the mechanical force and the moving membrane snaps on to the backplate. This is called pull-in, and it defines the maximum sensitivity achievable for a certain inter-electrode airgap. Typically, in a voltage biased MEMS capacitive sensor, such as shown in figure 2-3b, pull-in occurs at 1/3<sup>rd</sup> of the initial inter-electrode gap [18,19], significantly limiting the moving membrane’s travel-range. The travel-range of MM can be extended beyond pull-in by controlling the bias-charge inside the MEMS [18,19], which is also termed as charge-biasing. However, the charge-control schemes should be critically evaluated with respect to the targeted application since they increase the complexity of the system.

Figure 2-4 shows the simplified electrical model of the MEMS microphone along with a typical constant-charge voltage-readout scheme. This model neither includes the dynamics of the electro-mechanical sensor nor the effect of the non-linear nature of forces inside the MEMS [9]. However it highlights the major issues that are important to electrical interfacing of the sensor, as discussed in the following text. The capacitance between the BP and MM in the polarized structure is shown as  $C_0$ . It is termed as the nominal bias capacitance. The capacitive-variation that is sensitive to acoustic pressure is represented as  $C_M$ . The electrode-to-substrate parasitic capacitors are shown as  $C_{p1}$  and  $C_{p2}$ . These parasitics in

a micromachined capacitive structure are inevitable since both the electrodes are mounted on the substrate and therefore they develop a certain capacitance with it. These parasitic capacitors might also suffer from dielectric relaxation on the higher side of the audio-band [20]. Therefore, the value of these parasitics changes in the audio band. These parasitic capacitors are a critical issue for the readout interface since they considerably deteriorate the readout sensitivity, as discussed in the next section. The interconnect parasitic from the bonding wire and the parasitic from the input device of the PAMP also contributed to the total parasitic capacitance at the sensing node and is shown as  $C_{P,IN}$ . A high-value parasitic resistor ( $R_p$ ) exists between BP and MM, due to some process anomalies explained elsewhere [20].



**Figure 2-4 : A Simplified Electrical Model of MEMS Capacitive Microphone and a typical Constant-Charge Voltage-Readout Scheme**

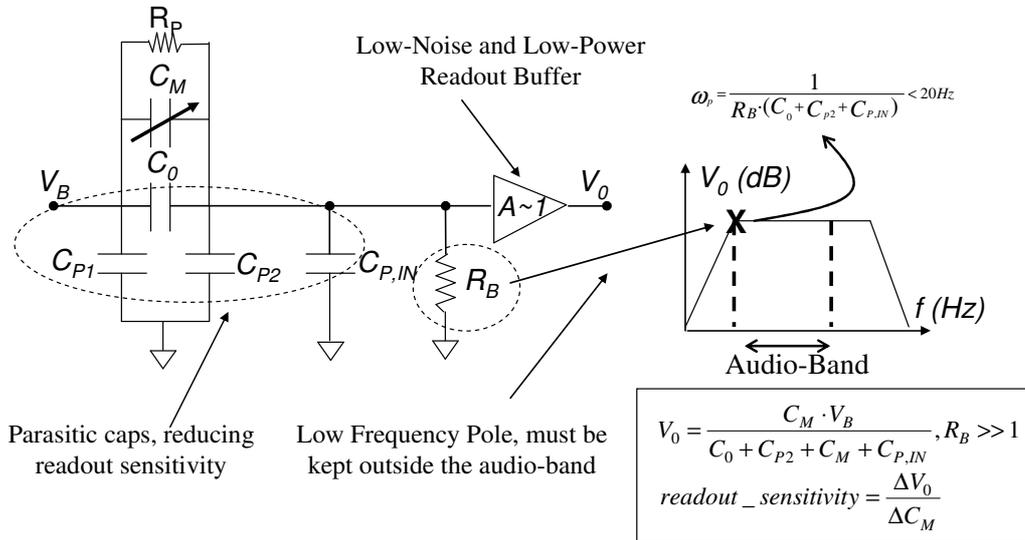
The readout sensitivity depends on the bias charge stored in the MCM, which in turn depends on  $V_B$ . Depending on the inter-electrode gap and the parasitic capacitors, a high value of  $V_B$  might be required to achieve the required readout sensitivity. A common practice in voltage biasing is to bias the sensor around 70% of the pull-in voltage [19], which translates into 7V for the above mentioned IRST MCM. This dc bias is usually higher than the supply voltage battery-operated acoustic systems and therefore requires an integrated charge-pump to produce this high-voltage. In portable systems, maintaining the high dc-bias intact requires a precise control on charge-pump [21].

The MCM structure shown above is referred to as single-ended MCM since only a single un-complemented polarity of the capacitive variations is available as the transduced signal. Examples of other single-ended MEMS microphones in the literature can be found in [6,7,10,22-24]. Some approaches employ differential structures [4,25,26] using either double-diaphragms or double-backplates. The motivation behind the differential structure is to mitigate the dilemma between stability and higher sensitivity and developing a structure that is also suitable for force-balancing. However, a differential MEMS microphone requires relatively complicated processing for fabricating either dual backplate or dual diaphragm in the structure [4].

## 2.2. State-of-the-art on Main Functional Components of the Readout Interface

### 2.2.1 Preamplifiers

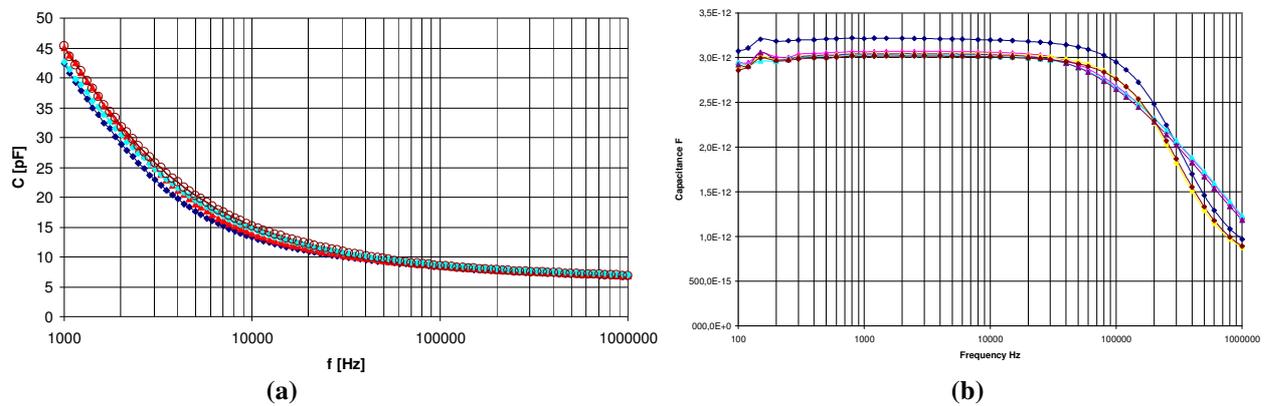
The preamplifier interfaces directly to the sensor and its design is a strong function of the sensor's characteristics. The sensor features and the targeted application drive the selection of the topology for the PAMP, the power consumption and its total area. The MCM sensor has no driving strength; therefore, the PAMP has to buffer the capacitive variations, marred by parasitics, into a voltage (or current) representation. The following text highlights the major issues that the PAMP faces and their state-of-the-art solutions. In short, these issues include mitigating the impact of sensor parasitics, implementing a suitable dc-biasing network that achieves a consistent sensitivity throughout the audio band and achieve a low-noise and low-power implementation of the readout scheme in CMOS. Figure 2-5 conceptually represents these issues.



**Figure 2-5 : Conceptual Representation of the major issues in the Preamplifier Design for MCM**

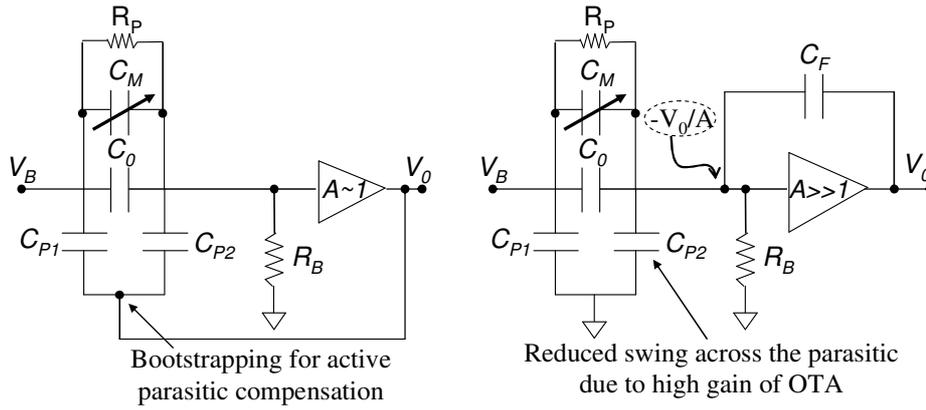
As discussed above, the MCM is based on micromachining technology and the presence of unwanted parasitic capacitors ( $C_{p1}$  and  $C_{p2}$ ) is inevitable. The nominal dc bias capacitance  $C_0$  due to the dc biasing of the sensor, is also considered as a parasitic capacitor. A constant-charge voltage-readout PAMP scheme is shown in figure 2-5, which is commonly adopted in the literature for capacitive sensors [24]. It provides a simple and robust interface with minimal spurious effects or loading to the sensor, requiring least components close to the sensor. The other reason in favour of this approach is borrowed from the fact that CT PAMPs achieve lower noise for the same power budget if compared to the discrete-time approaches [27]. The voltage modulation in the above approach takes place over the total capacitance of the structure ( $C_T = C_0 + C_M + C_{p2} + C_{P,IN}$ ), i.e. the readout voltage  $V_0$  is a function of the ratio between capacitive variation ( $C_M$ ) and the total capacitance ( $C_T$ ), as expressed in figure 2-5. Since  $C_M$  is orders-of-magnitude smaller than the total capacitance of the structure (typical  $C_M \sim \text{fF/Pa}$ , while  $C_T \sim \text{pF}$ ), the readout voltage

signal is very weak, in other words, the readout sensitivity is very low. These parasitic capacitors might also exhibit dielectric relaxation and offer different impedance to different frequencies in the audio band. Figure 2-6a shows the dielectric relaxation over the acoustic band for the parasitic at the moving-membrane for two different generations of the IRST MCM [20]. It can be seen that the first-generation MCM suffered from considerable variations in parasitic values. This was due to a thin air-gap at the contact-points for moving-membrane and substrate [20]. The air-gap was very thin and as the signal frequency increased, charge leaked through the air-gap bringing down the parasitic capacitor. This effect is mitigated for the second-generation of IRST MCM as shown in figure 2-6b by providing better insulation at the contact points for MM and substrate and is explained in detail elsewhere [20].



**Figure 2-6 : Dielectric Relaxation of the Parasitic Capacitors ( $C_{P2}$ ) at the Moving-Membrane for two different generations of IRST MCM, (a) first-generation, (b) second-generation with improved insulation at the contact points of MM and Substrate**

Bootstrapping [28-31] has been shown to minimize the effect of interconnect or stray parasitic capacitances, by shielding the capacitance and tying it to the output of unity gain PAMP, minimizing effective voltage swing across the parasitics. Similar approach can be extended to the MCM parasitics, as briefly shown in figure 2-7a and is analyzed in detail in chapter 3. The other approach is to connect the MEMS sensor to a virtual ground node, such as at the input of a high-gain OTA, in a capacitive feedback configuration [32,33], as shown in figure 2-7b. This reduces the swing across the parasitics  $C_{p1}$  and  $C_0$  by the gain of OTA thus minimizing their impact. However, this approach requires connecting the MEMS directly to a capacitive gain stage which, due to the mismatch between MEMS capacitances and PAMP-capacitances, can cause an uncontrolled gain at the output of the PAMP; this approach is analyzed in detail in chapter 4.



**Figure 2-7 : Conceptual Representation of Parasitic Minimization Schemes employed in PAMP for MCM**

The other issue is about dc biasing of the PAMP's sensing node. The PAMP should provide a high-impedance input port to MCM signal and low dc-impedance to establish a stable dc point at the sensing node. The biasing component could either be a resistor or a switch periodically charging the node to a fixed dc value. Since the acoustic band extends down to low-frequencies such as 20Hz, the biasing network should offer high-impedance till 20Hz and low-impedance at dc. This translates into a value above  $G\Omega$  for the bias resistor.

For continuous-time (CT) PAMPs, zero-biased diodes [32], transistors biased in sub-threshold [34] and pseudo PMOS resistors [33] have been employed. Discrete-time (DT) approaches include periodic resetting of the input node to the required reference voltage [27]. These approaches have their respective pros and cons. Zero-biased diodes, sub-threshold transistors and pseudo-PMOS resistors exhibit variable resistance depending on the signal-swing across them [33]. Therefore, for larger signals the resistance is smaller and causes signal clipping and distortion. This can result in an inefficient utilization of the PAMP's DR. The discrete-time approach of periodic resetting causes spurious charge-injection and a certain drift depending on the resetting period [36]. Active charge cancellation techniques can be used to compensate for this charge injection at the input of the PAMP; however, if noise and power budgets are tight, an active charge cancellation scheme must be critically thought out [35]. The reset noise reduction schemes in [36] also include a feedback loop that either cancels the reset noise, or reduces the bandwidth of the noise or controls the reset process itself so that the resetting is itself less random and contributes to a fixed dc offset. However, it incurs overhead of power and the stability. [37] uses a positive feedback to modulate the bias voltage of a subthreshold transistor to increase keep the transistor in high-resistance region for larger swings around it by increasing the body-effect. This reduces the distortion due to this resistance for larger input swing. The subsequent chapters of this thesis describe the application of zero-biased diodes, pseudo-PMOS resistors and utilization of miller effect to achieve the low-frequency pole using  $M\Omega$  resistor.

The above-mentioned readout schemes fall in the category of dc-readout, in which a readout-sensitivity is established by biasing the MCM and the ac signal is MCM capacitive variations [38]. PAMPs for other sensors also utilize a readout termed as ac-readout, in which a high-frequency carrier is

applied to the sensor and the capacitance change is detected as the change in the amplitude (or frequency) of the applied carrier. This is a common approach to readout MEMS capacitive accelerometers [38-40]. However, accelerometers are structurally different from MEMS microphones. MEMS accelerometers have an in-plane fully-differential structure, i.e. two complementary capacitive variations are available at the output [38-40]. MEMS microphones, however, have been mostly based on a single-ended structure, due to the complications in processing a differential vertical out-of-plane structure. The ac-readout suits capacitive sensors with a differential structure since the applied carrier is rejected as a common mode signal by the differential structure before reaching the PAMP. Application of ac-readout to MEMS microphone is found in [33], although exact details about the structure of the sensor are not documented in the report. Therefore, simply put, the dc readout can be considered as structure-independent approach for MCMs.

The use of a dummy capacitive branch is suggested in [40] to mitigate the problem for ac readout by converting the single-ended sensor into a pseudo-differential sensor. The dummy branch can be adjusted to closely match the MEMS capacitive value. This adjustment can be made by filtering the output using a narrow-band low pass filter ( $f_c \leq 10\text{Hz}$ ), extracting the dc offset in the PAMP output, and then using it to adjust the dummy-capacitance. [8] motivates the idea of putting a dummy capacitive structure inside the MEMS sensor to convert it into a pseudo differential sensor, while [95] suggests using a dual-sensor system to achieve a differential topology. [41] suggests a fully differential transimpedance amplifier along with a dummy reference cap that has the same nominal cap as the MEMS. However, mismatching between MEMS and reference cap needs to be taken care of. This concept of dummy capacitive branch is utilized and discussed in the subsequent chapters of this thesis.

The above mentioned approaches implement a straightforward C-to-V buffer, which leaves the responsibility of configurability or controllability in the interface on the ADC that follows the PAMP. However, there can be some issues at the output of the PAMP, which if not corrected within the PAMP, can be difficult to contain later. For instance, any offset at the output of the PAMP, translates into an input offset for the following ADC. Typically, the ADC for audio applications is a SDM, as discussed in detail in the next subsection. The input offset for SDM defines the location of idle tone which, depending on the offset, might also fall inside the audio band. Therefore, it is useful to add offset control functionality inside the preamplifier. Moreover, having a controllable gain at the output of the PAMP can relax the design of the SDM by enabling it to use smaller capacitors for the required KTC noise, consequently, reducing the power consumption. At the same time, a filtering capability to remove unwanted low-frequency components can help in case of removing noise-hum. This low-freq hum can cause a saturation or inter-modulation with the voice signal or simply make the desired signal inaudible [42].

Correlated-double-sampling and Chopper-stabilization are two of the established techniques to remove low frequency flicker noise and offset of the OTAs [43] in switched PAMPs. However, most likely due to their switched nature they have not been applied to MEMS microphone PAMPs so far in the available literature. The main issues in the application of switched techniques are as follows. First, the

gain is not well controlled since the matching between the capacitive gain caps and the MEMS cap is not well-controlled. Second, the spurious charge-injection from the switches around the MEMS sensor can deteriorate the linearity of the readout.

Chapter 5 of this thesis suggests a two-stage chopper-stabilized PAMP to implement a switched PAMP for MEMS microphone and avoiding the above mentioned problems. The motivation of a two-stage PAMP for microphone can also be derived from [44] in which an ECM microphone is buffered using an NMOS in constant-charge current-readout mode, feeding the resulting current into a transimpedance amplifier. It also uses an active low-frequency feedback loop to subtract the dc component of the sensor's current, which helps in better utilization of the DR. Similar approach is presented in chapter 5 for controlling the offset at the output of PAMP as an extra functionality as mentioned above. Differential difference amplifier is used in [32] to implement a PAMP for microphone. The advantage achieved from using a DDA is that two separate feedbacks can be applied independent of each other. One input pair of the DDA can be used to connect the sensor, just like a capacitive gain stage. The other input pair of the DDA can be used to implement the dc feedback. The presented two-stage PAMP in chapter 5 uses an OTA topology similar to DDA.

[45] implements a PAMP for an ECM using only CMOS OTAs. The high-value bias resistor is implemented using a low-gm grounded unit-gain-OTA. The bias capacitance of the sensor in [45] is 30pF, therefore, a bias resistance of 100M $\Omega$  is required to achieve a flat response in the audio-band. However, for a smaller nominal cap of the MEMS sensor, e.g. around 1pF, it is difficult to achieve the required value of the resistance using grounded OTA resistance, since further lowering the gm requires reduction in bias current of OTA, which ultimately violates the noise specifications.

Some PAMP approaches that directly place the MEMS sensor inside a sigma-delta loop; however, these approaches can be power-hungry due to the periodic charging (and discharging) of MCM parasitic capacitors [46,47]. It is discussed in the next sub-section that some approaches employ hybrid SDMs in which the first-stage of the SDM is continuous-time (CT) and subsequent stages are discrete-time (DT) [53,88]. These approaches utilize the first CT stage as a PAMP for the sensor.

The frequency-modulated readout for MCM is also an established approach in the literature. [16,41]. The MCM is used as the timing capacitance of an oscillator, and the frequency of the oscillator is modulated because of the variable MEMS capacitance. This approach also does not require high dc-bias inside the MEMS sensor for establishing the required sensitivity and an ADC is also not needed in the RI. This readout scheme also demonstrates a lower sensitivity to the power-supply variations, which is critical for battery-operated system. However, this approach requires a high-frequency carrier and the subsequent charging (and discharging) of the MCM parasitics can make it power-hungry. It also suffers from relatively higher noise floor as compared to dc-readout due to the jitter coming from inverters, oscillator's resistor and the MCM parasitic capacitors [50].

Table 2-2 lists the SNR and power consumption of some commercial MEMS microphone, along with a PAMP, to develop a benchmark of the expected performance from the PAMP. It can be noticed

that the analog output of the MCMs with embedded PAMPs reaches sensitivity around -40dBV and targeted SNR for a 1Pa/1kHz acoustic signal is 60dB a-weighted.

**Table 2-2 : Commercially Available MEMS Capacitive Microphones with embedded Preamplifier**

<b>Commercially Available MEMS Capacitive Microphones with embedded PAMP<sup>1</sup></b>			
Company	Total Current $\mu\text{A}$	SNR (A-weighted) @ 1Pa,1kHz dBA	Sensitivity dBV
Akustica AKU1126	150	59	-42
Infineon SMM 310 E6433	70	59	-42
Knowles Mini SiSonic	100	58	-42
Wolfson Microelectronics	150	59	-42
Pulse Engineering SiMic	330	61	-40

### 2.2.2 Sigma-Delta Modulators for Audio-Applications

Typically, a Sigma-Delta Modulator is used as an ADC for audio applications. SDMs utilize over-sampling and noise-shaping to achieve high-resolution analog-to-digital conversion without requiring highly-precise analog components; however, they need digital post-processing by a decimation filter [51]. The audio applications do not require very large bandwidth and an adequate oversampling ratio (OSR) for the SDM can be achieved for moderate sampling frequencies. This enables SDMs to reach the required DR without opting for very high-order modulators for audio applications. SDMs are a vast research area and their topologies differ greatly depending on the underlying application. The parameters that control their performance are their order, the over-sampling ratio and the quantizer resolution [51]. There exists a trade-off between achievable DR and the power consumption that is governed by above mentioned control threads. Therefore, it is necessary that SDM be carefully designed for the targeted application.

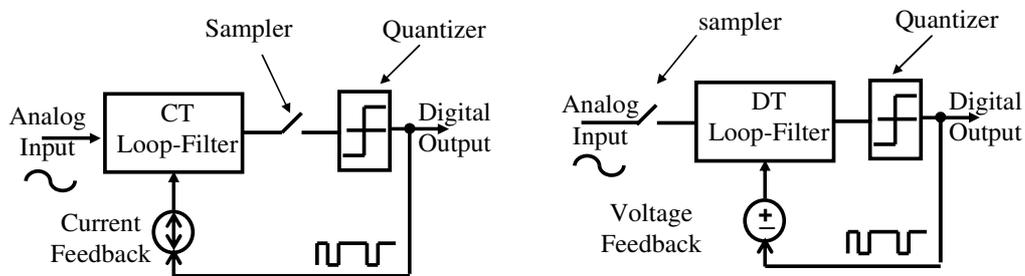
For audio applications, one major classification of SDMs is between discrete-time (DT) and continuous-time (CT) SDMs. The DT SDMs for audio applications have been the preferred choice for quite some time for the reasons mentioned below, while the CT SDMs have recently attracted vast attention exhibiting major improvements in power consumption for audio application over their DT counterparts [52,53].

The loop-filter coefficients in DT SDMs depend on the ratio of the sampling and the integrating capacitors of the DT integrators. In CMOS, the ratio between two similar caps can be controlled accurately, implying that the NTF and STF of DT SDMs are well-controlled. However, the OTAs that are used to implement the integrators need to have higher UGBW than the sampling frequency, to achieve the required settling accuracy [53]. This is due to the fact that OTAs are required to settle according to one of

<sup>1</sup> Refer to the relevant product data-sheets for more details on the product features

the two reference feedback voltages every integration cycle. This consumes extra power as compared to the CT counterparts. Another advantage of DT SDMs is that CDS and CHS techniques can be applied directly to them due to their inherent switched nature of operation [53].

CT SDMs, since they employ a CT loop-filter, do not require fast settling behaviour from OTAs, therefore, the required UGBW is lower than that in their DT counterparts. This leads to less power consumption in OTAs. Moreover, CT modulators inherently offer anti-aliasing filter function since there is no sampling of the signal at the input. Unlike a DT modulator, in which the first integrator samples the input signals outside the noise-shaping loop, the signal sampler is at the quantizer in a CT modulator, which is inside the noise-shaping loop. Thus, the sampling error is suppressed similarly as the quantization error in the CT modulators [48]. However, the major issues with CT SDMs is the unmatched spread in resistors and capacitors that are used to implement the loop filters, furthermore, the sensitivity to the clock jitter becomes a bottleneck. Since the feedback is not a continuous-time addition/subtraction based on the digital feedback, non-uniformity in feedback due to clock-jitter can directly affect the performance of the CT SDMs. DT SDMs do not suffer from this problem since the jitter effect is mostly diffused by the sampling in the integrators. CT SDMs show higher sensitivity to process, temperature, and supply voltage variations, therefore, they should be carefully tuned and optimized at the operating frequency; moreover, the stability of high-order CT SDMs is critical due to the inherent loop delay of the quantizers and the DACs. [48]. However, CT SDMs are compatible with low-voltage technologies since there is no need to bootstrap switches [53]. A conceptual representation of DT and CT SDMs is shown in figure 2-8.



**Figure 2-8 : Conceptual representation of CT and DT SDMs**

It has been demonstrated in [54] that an optimal set of filter coefficients exists for every SDM, which maximizes DR and the SNR. A second-order modulator, with optimal coefficients and a single-bit quantizer, achieves DR of 57dB and 74dB for OSRs of 32 and 64 respectively. Similarly, a third order modulator for its optimal set of coefficients achieves a DR of 65dB and 86dB for OSRs of 32 and 64, respectively. Using different coefficients either increases the quantization noise floor or makes the overload-effect dominate earlier, thereby achieving the same effective DR [54]. Therefore, according to the underlying requirement of audio analog-to-digital conversion, to achieve a DR above 80dB for OSR around 60, one must either use a second-order modulator with multibit quantizer, or third-order modulator

with a single bit quantizer [54-56]. Multi-loop topologies can also be used, as discussed below. This fact is used as the motivation behind the selected SDM topologies in the readout interfaces during this work.

Based on the reviewed literature, the SDMs for audio utilize both single-loop and cascade/MASH structures. In the single-loop topology, modulator has a single-quantizer and order of the modulator is determined by integrators in this loop. There can be multiple internal loops but there is a single datapath from input to output. Single loop topology is simple, robust and insensitive to component matching. In cascaded topology, there are multiple datapaths in the modulator, often of different orders, and their output is combined at the final output. The cascaded topology has several advantages over single-loop topology, which includes better stability and higher resolution. However, matching between multiple datapaths is critical for achieving the optimal performance for multi-loop structures [57,58].

OTAs in an SDM are the major source of power consumption. Therefore, OTA design should strongly correspond to the required specifications to avoid over-design. [59] demonstrates that OTA gain of above 30dB is enough to achieve a DR above 85dB with a third order modulator. [59] suggests that for achieving an SNR around 100dB with OSR of 80, the power consumption by two-stage class AB OTA, Two-stage class A OTA and a single-stage folded-cascode OTA are almost equal for supply voltages above 1.5V. The power consumption of a folded-cascode OTA remains nearly constant for an increase in the OSR as compared to class A or AB OTA, unless the OSR goes above 100 [59]. Besides, implementing the CMFB control for a two-stage OTA requires a sign inversion, which is typically implemented using a current mirror and it consumes considerable power for not compromising the stability. Therefore, a single-stage OTA with moderate gain, unity-gain-bandwidth (UGBW) and driving-strength is adequate for the targeted DR. These facts are behind the selection of OTA topologies for the design SDMs in this work.

To reduce power consumption in SDMs, swing at the output of OTAs can be reduced using feed-forward topology [60]. The feed-forward topology makes only the quantization error flow through the chain of integrators, i.e. the signal does not flow through the integrators, therefore, OTAs can have relaxed settling, reducing the power consumption. However, for a single-bit quantizer, the maximum swing of the quantization error is larger than multibit quantizer (two-bit or higher). Therefore, a feed-forward topology is fully-utilized from power consumption aspect with a multi-bit quantizer. Using multibit quantizer requires dithering in the feedback path, to randomize the mismatch error in the multibit DAC. Therefore, the increase in power due the extra components along with feed-forward topology must be carefully evaluated from power-consumption aspect [59].

For low-voltage audio SDMs (below 1V), bootstrapped switches [61], switched-opamp [63] and switched-RC [62] approaches are used. In switched-RC approach [62], the input switch is replaced by a resistor which removes the necessity of driving the main input switch, improving linearity and dynamic range for low-voltage. In switched-opamp technique [63], the switches at the output of the opamps, since they have to see the full signal swing, are removed and instead the OTA is switched-off internally.

Hybrid SDMs, utilizing a combination of DT and CT loop-filter, are reported in [53,88]. The first continuous time integrator stage can also be directly interfaced to the sensor as a PAMP [88]. This allows the first stage of the SDM to act as a PAMP and also take part in the noise shaping at the cost of a high performance ADC with low-noise input stage.

There are three performance gauging parameters for an SDM, dynamic range, conversion bandwidth and power consumption. The figure of merit for SDMs is defined as [56],

$$FOM = \frac{4 \cdot K \cdot T \cdot DR \cdot f_B}{P}$$

where K is boltzmann constant, T is the temperature, DR is the dynamic range

of the SDM,  $f_B$  is the conversion bandwidth and P is the total power consumption. Figure 2-9 plots the FOM for state-of-the-art SDMs for audio application, highlighting the region which most of the SDMs target for audio application, and it is used as a benchmark in the design of SDMs during this work.

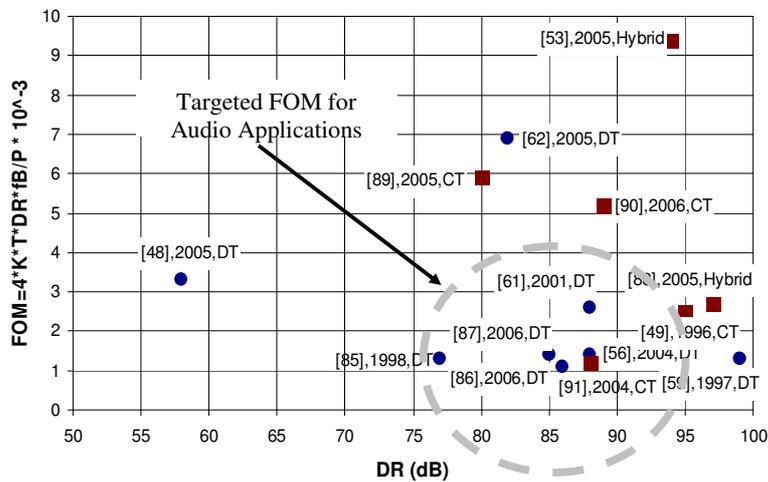


Figure 2-9 : The Figure-of-Merit for the above mentioned SDMs, highlighting the targeted FOM for audio applications

### 2.2.3 Force-Feedback for MEMS Capacitive Sensors

Force-Feedback (FFB) has been commonly employed to minimize the impact of mechanical imperfections and inherent non-linearities in MEMS capacitive sensors [64-67]. FFB is also termed as force-balancing and it refers to enclosing the MEMS sensor in an electro-mechanical feedback loop to affect the properties of the sensor through the feedback. The capacitive variations from the sensor are readout by the interface and the output; either analog or digital, is fed back to the sensor as an electrostatic force which counter balances the incident force. The counter-balancing feedback reduces the movement of the mobile electrode, thereby, reducing the secondary effects that might arise due to exaggerated movements, as discussed below. Furthermore, FFB can also be used to improve stability and reduce the impact of drift in the mechanical features of the sensor [65].

The MEMS capacitive microphone is approximated as a second order electro-mechanical system, whose pressure-sensitive capacitive-variations are dependent on the inter-electrode gap. The moving-

membrane's displacement; however, is a non-linear function of the net-force inside the MEMS structure.

The major forces inside the MCM are as follows:

- The incident acoustic force ( $F_{ac}$ ), which is the incident acoustic pressure multiplied by the total effective area of the moving membrane.
- The mechanical restoration force ( $F_m$ ) of the suspension spring.
- The electrostatic force ( $F_e$ ) between the two electrodes because of the applied dc-bias voltage across them.
- A damping force that provides an inertial friction to the moving electrode because of the air trapped between electrodes. And another inertial force, which is related to the mass of the moving electrode.

The generic expression describing the dynamics of the MEMS is as follows:

$$m\ddot{x}_t + b\dot{x}_t + k \cdot (x_t - x_0) = \frac{\epsilon \cdot A \cdot V^2}{2 \cdot x_t^2} \quad (\text{Eq. 2-1})$$

Where  $x_t$  is the instantaneous displacement of the moving membrane,  $x_0$  is the initial inter-electrode gap biased at the required sensitivity,  $m$  is the mass of the moving membrane,  $b$  is the damping coefficient and  $k$  is the stiffness coefficient of the spring and  $V$  is the voltage across the two electrodes. The above eq. 2-1 reduces to eq. 2-2 in equilibrium, i.e. when the incident acoustic force is zero and the moving membrane is stationary:

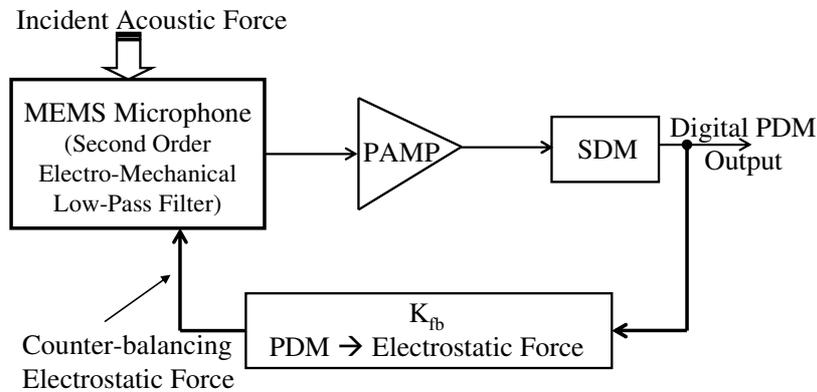
$$k \cdot (x_t - x_0) = \frac{\epsilon \cdot A \cdot V^2}{2 \cdot x_t^2} \quad (\text{Eq. 2-2})$$

As shown in eq. 2-1, the balance of forces which governs the displacement of the moving membrane depends quadratically on the displacement, which signifies that there is a range of displacement after which the higher order terms are not negligible in the response. In other words, for larger displacements, the higher order terms in the resulting capacitive variations are considerably large to distort the output. Moreover, under large acoustic inputs, the mechanical system is stretched beyond its optimal range of operation, causing secondary issues such as membrane bending. Large and low-frequency displacements also increase the possibility of pull-in. Force-balancing can be used as a stabilizing control for the microphone moving membrane against pull-in [65]. Additionally, enclosing the non-linear MEMS sensor into a high-gain loop, implemented in electronics, the output of the complete acoustic system can be made to depend only on the electrical feedback network [64]. Therefore, minimizing the impact of drift in mechanical properties of the sensor. A force-balancing loop can also relax the noise specifications of the readout interface. The margin gained by reduction in the amplitude for large inputs can be used to place the smaller inputs higher in the full-scale range.

Force-balancing for MEMS capacitive accelerometers is an established practice [64,66,67]. MEMS accelerometers usually have a fully-differential mechanical structure and their readout is based on ac-readout, partitioned into several phases. Typically, sensing and force-feedback are performed in separated phases [39,67,68]. The counter-balancing electrostatic force is applied in the form of voltage pulses.

For a MEMS microphone with a single-ended structure the sensing and feedback should be performed together. To generate the counterbalancing electrostatic force, the backplate node can be used, since the moving membrane is used as the sensing node. The readout interface converts  $\Delta C$  into  $\Delta V$ , which is consequently converted to a corresponding electrostatic force and applied back to the MEMS. However, as eq. 2-1 suggests, the electrostatic force has quadratic relation with both voltage and the inter-electrode distance. So, such a feedback is conditionally linear and is termed as ‘analog force-feedback’. MEMS sensors (accelerometers) utilize analog force-feedback [65, 69, 70] by making use of the symmetry in their micro-mechanical structure.

Force-Feedback can be linearized by using a time-referenced representation of the signal instead of an amplitude-referenced representation [66]. Time-referenced representations of the signal include a pulse-density or pulse-width modulated outputs, in which the amplitude information of the signal is represented either by the width of the pulse or by the density of pulses. In this case, the amplitude of the applied feedback is always the same. Since the MEMS microphone is a second order electro-mechanical low-pass filter, the counter balancing electrostatic force applied as PDM or PWM would be automatically regenerated by the sensor internally. Therefore, this paves the way of application of a PDM output (such as the output of a sigma-delta modulator) directly as a force-feedback to the MEMS and it is termed as digital force-feedback. Figure 2-10 shows the common approach employed for digital force-balancing in MEMS capacitive sensors [65-68][39].



**Figure 2-10 : Conceptual Representation of the Digital Force-Feedback Scheme for MCM**

In figure 2-10, PA, SDM and the force-feedback logic along with the transfer function of MCM make the loop filter for the force-balancing loop. Some approaches utilize only MEMS sensor’s second-order transfer function as the loop filter for the electro-mechanical SDM loop [69][71]. However, these approaches suffer from the low dc gain of the MEMS, which causes high quantization noise in the band [68]. Moreover, the loop might need an extra lead-filter to compensate for the low phase-margin since the MEMS sensor could be under-damped causing potential stability problems. State-of-the-art techniques use higher order SD loops, to achieve better noise shaping and enhance the stability of the closed-loop system [66-68]. Force-balanced MEMS microphone can be found in [65] and [69]. A more recent application of force-balancing to MEMS microphone comes from [72]. All of the approaches are analog force-

feedbacks, mainly due to the single-ended structure of the MEMS microphone. In some approaches [65], two electrodes are implanted over the moving membrane, one for sensing and the other for feedback, which is also found in accelerometers [68][39].

However, in the available literature detailed results are not available on the application of force feedback to MEMS microphone. Chapter 5 of this dissertation discusses a readout interface to apply digital FFB to MCM, giving details of the issues that arise and suggesting few viable solutions.

# Chapter 3

## Readout Interface – I

### 3.1. Introduction

This chapter presents design details and measurement results of the first integrated readout interface for MEMS Capacitive Microphone designed under this research activity. This readout interface consists of a preamplifier, a sigma-delta modulator, integrated biasing and digital control, converting the capacitive variations of MCM into an over-sampled digital bitstream. The preamplifier of this interface employs a modified bootstrapping scheme to achieve a parasitic-insensitive readout. The single-ended input of the MCM is converted into a pseudo-differential output by the preamplifier through the use of a dummy-branch. The sigma-delta modulator converts the analog output of the preamplifier into an oversampled digital bitstream. This interface has integrated on-chip biasing; therefore, it requires minimal external control. The major blocks of the interface are shown in figure 3-1.

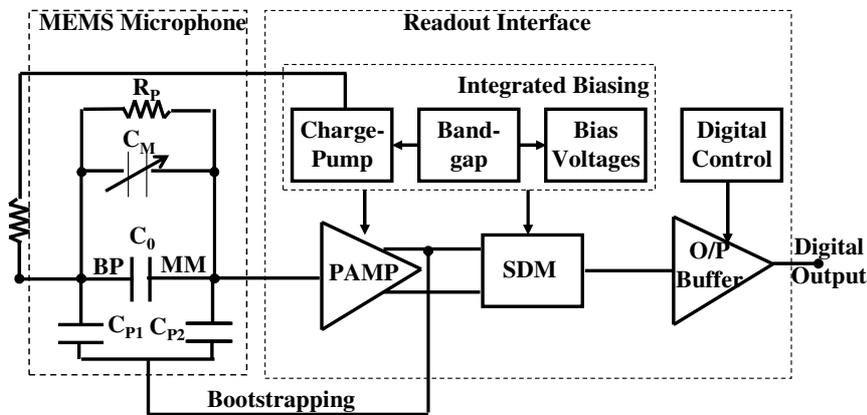


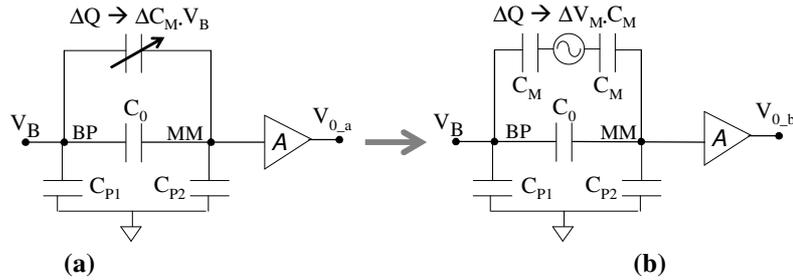
Figure 3-1 : The major blocks of the Readout Interface

### 3.2. Behavioral Description and Simulations of the Readout Interface

#### 3.2.1 Model of the MEMS Microphone

The main simulations of the readout interface can be divided in two categories. First, to check the functional behaviour of the interface. Second, to have an accurate estimate of the noise and distortion of the whole system along with the sensor. This necessitates the development of two different models for the MCM. First model should simply deliver the equivalent capacitive variations with the specified sensitivity. The other accurate model should mimic the electro-mechanical structure of sensor closely, including

the dynamics and the non-linear nature of the forces inside the MEMS. The following text discusses both models in detail. Figure 3-2a shows the simplified electrical model of the sensor with  $C_M$  representing the pressure-sensitive variable capacitance. The product of  $C_M$  and the voltage across it represents the charge-induced by the pressure-sensitive capacitive variations. The same source of charge can be represented by using a fixed value of capacitor with a variable voltage source as shown in figure 3-2b. The output voltages for both cases are expressed in eq. 3-1, showing a direct correspondence between the models.



**Figure 3-2 : Simplistic Model for Capacitive Variations in MCM, replacing  $C_M$  with a voltage-source  $V_M$**

$$\Delta V_{0\_a} = \frac{(V_{BP} - V_{MM}) \cdot \Delta C_M}{C_0 + C_{P2}} \quad (\text{Eq. 3-1})$$

$$\Delta V_{0\_b} = \frac{\Delta V_M \cdot C_M}{C_0 + C_{P2}} \quad (\text{Eq. 3-2})$$

The capacitive variations in the MEMS and the resulting voltage change are inversely related. This is due to the fact that the total charge is conserved over the total capacitive structure. Therefore, an increase in the capacitance of the MCM correspondingly brings down the voltage across it. This inverse relation raises questions about the linearity of the simplistic voltage-source model, shown in figure 3-2b, in which  $\Delta C$  is replaced by  $\Delta V$ . This can be explained by highlighting the fact that the charge redistribution due to  $C_M$  is residing over a bias charge, which is orders-of-magnitude larger than charge induced by  $C_M$ . This bias charge exists due to the nominal dc-bias capacitance  $C_0$  and the parasitic capacitor  $C_{P2}$ . Therefore, due to this bias charge, although  $\Delta V$  and  $\Delta C$  have an inverse relation, the resulting voltage-source based model remains linear but  $180^\circ$  out-of-phase. The voltage source is contained within capacitors from both sides so that the driving capability of the ideal source does not disturb the transient simulations [73]. The sensitivity of the voltage model is normalized based on eq. 3-1 and eq. 3-2.

However, the voltage-source model, shown in figure 3-2b, cannot account for the dynamics and the non-linear nature of forces inside the MCM. As mentioned in the previous section, MCM is approximated as a second-order system, in which the displacement of the moving membrane is governed by a balance of acoustic, electrostatic and mechanical forces, along with the inertial forces due to mass of the moving membrane. This balance of forces itself depends quadratically on the inter-electrode gap. Therefore for large displacements of the moving membrane, the higher-order terms in the expression defining

the dynamics of the electro-mechanical system, are not negligible. Furthermore, for higher acoustic inputs, the mechanical system could be stretch beyond its optimal range of mechanical operation and secondary issues, such as membrane bending, may arise. The viscous damping inside the sensor is also a variable force, which increases considerably for larger acoustic inputs given the fact that the displacement of the membrane is larger and the air-trapped between the electrodes does not find a faster way to escape, thereby resisting the membrane’s movement. The parasitics in the sensor, as mentioned above, are not constant throughout the audio-band due to dielectric relaxation, and this implies that overall sensitivity of the sensor is variable.

Figure 3-3 shows the lumped-element representation of the MCM using electro-mechanical analogy [9], where each mechanical element is replaced by corresponding electrical impedance. The inertial components such as mass are replaced by inductors in the lumped model.  $C_{SP}$  represents the mechanical compliance of the spring, which is the inverse of the effective spring-constant under the applied bias. Back-chamber compliance represents the resistance offered to the movement of diaphragm by the air-trapped in the back-chamber. Here, diaphragm refers to the moving membrane of the MCM. Acoustic hole impedance represents the backplate’s degree of rigidity to the acoustic pressure. The current through this RLC network represents the velocity with which the diaphragm is moving and the displacement is computed by integrating this current. The input voltage represents the incident acoustic force, i.e.  $F_{ac}$ .

To simplify the lumped-element model, following assumptions are made. The Radiation impedance can be neglected considering that the major frictional and inertial effect of air-damping comes from the air-trapped within the electrodes, represented by air-gap impedance. The acoustic holes impedance effect can be neglected considering that the back-plate is absolutely insensitive to the incident pressure. Furthermore, considering a sufficient back-chamber volume, the damping effect of backchamber’s mechanical compliance can also be ignored. Therefore, in the simplified electro-acoustic model, diaphragm and the air-gap resistance define the major characteristics of the MEMS. The diaphragm impedance is partitioned into two major components; the inertial components due to the mass of the diaphragm and the compliance of the suspension springs which is related to the spring’s effective stiffness.

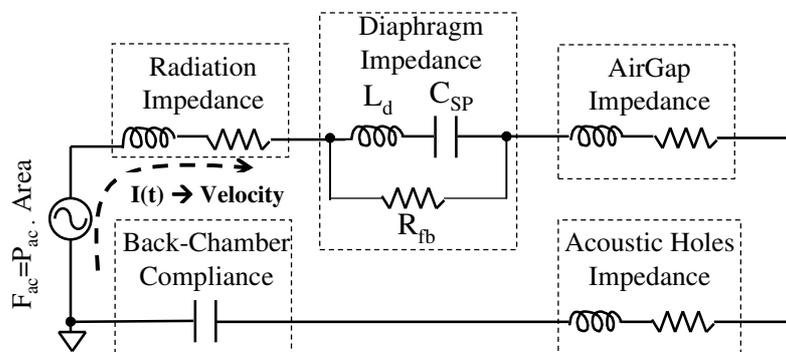


Figure 3-3 : Lumped Element model for the MCM based on electro-mechanical analogy

The implemented accurate model perceives the operation of electro-mechanical system as an act of striking a balance between mechanical, electrostatic and inertial forces present inside the sensor and finding an equilibrium point within the moveable range of the moving membrane. These forces can be seen as pull-up forces and pull-down forces. The pull-down forces corresponds to the attractive electrostatic force that decreases the effective the compliance of the spring. The pull-up force includes the mechanical restoration force of the spring. While the dynamics are governed by the inertial components of the force and the damping offered by the airgap. This model is implemented in VerilogA. Figure 3-4 shows a conceptual representation of the accurate model. This model assumes that the moving membrane is mechanically structured in the micro-structure to approximate an ideal piston-like movement [9]; therefore, it ignores the second-order effects that arise because of the membrane bending. The simulation results using both models are shown in sub-section 3.2.2 along with the description of preamplifier.

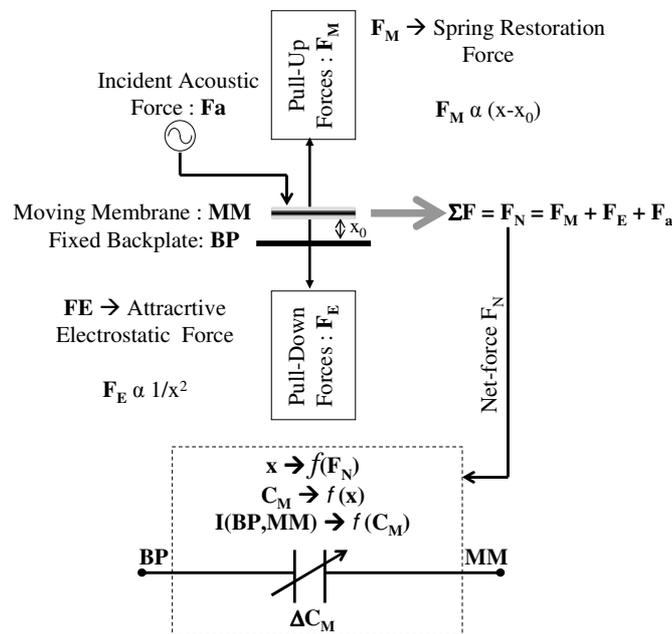


Figure 3-4 : Simplified representation of the accurate-model based on electro-mechanical analogy

### 3.2.2 The Preamplifier

The PAMP is a source-follower buffer based on constant-charge voltage-readout, which achieves a parasitic insensitive-readout by bootstrapping the MEMS sensor. The CT PAMPs achieve lower noise for a certain power-budget since they do not incur charge-injection and fold-over noise components [27]. Furthermore, a source-follower buffer provides a simple and robust interface to the sensor with minimal components close to the sensor, thereby reducing the chances of spurious loading of the MEMS.

The readout voltage  $V_{0\_NOBS}$  of the source-follower buffer without bootstrapping in figure 3-5a is expressed in eq. 3-3.  $R_B$  represents the high-value resistor to establish the operating point at sensing node MM.  $C_0$ ,  $C_{P1}$  and  $C_{P2}$  represent the above-mentioned parasitic capacitors of the MEMS while  $C_{P\_IN}$  repre-

sents the parasitic capacitance at the input of PAMP due to the input-device of the source-follower and the interconnect parasitic between sensor and PAMP. For simplifying the expression, A is considered as unity and  $R_B$  very large.  $V_N$  represents the input referred noise of the source-follower. The parasitic capacitors ( $C_0$ ,  $C_{P2}$  and  $C_{P,IN}$ ) deteriorate the readout sensitivity since the voltage modulation due to the capacitive variation  $C_M$  takes place over the total capacitance of the structure ( $C_T \sim C_0 + C_{P2} + C_{P,IN}$ ), as shown in eq. 3-3. As mentioned above,  $C_T$  is orders-of-magnitude larger than the  $C_M$ .

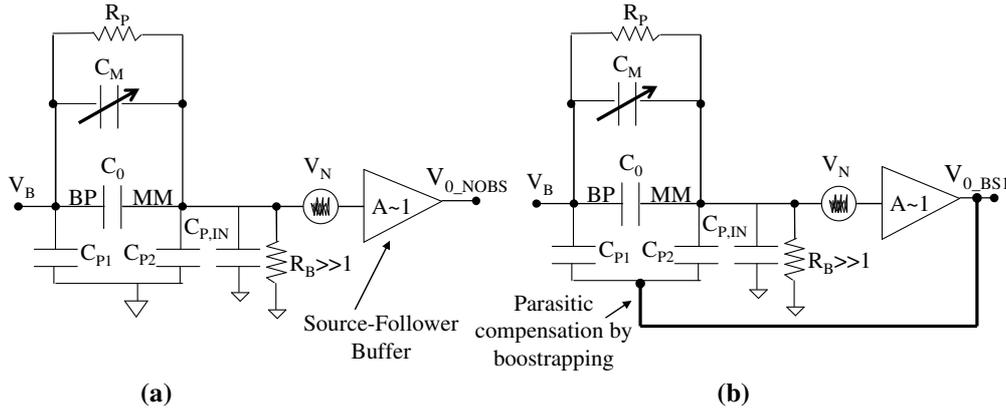


Figure 3-5 : (a) Typical Constant-Charge Voltage-Readout, (b) Constant-Charge Voltage-Readout with Single-Terminal Bootstrapping Scheme

$$V_{0\_NOBS} = \frac{C_M \cdot V_B}{(C_0 + C_{P2} + C_{P,IN} + C_M)} + V_N \sim \frac{C_M \cdot V_B}{(C_0 + C_{P2} + C_{P,IN})} + V_N \quad (\text{Eq. 3-3})$$

The MCM sensor can be bootstrapped to the PAMP by tying its substrate to the output of the source-follower buffer, as shown in figure 3-5b. Since the input and output signals are in-phase, this positive feedback reduces the effective signal-swing across  $C_{P2}$ , therefore, reducing its effect on the voltage modulation. This bootstrapping topology is termed as single-terminal bootstrapping (BS1) later in this text. This name refers to the fact that bootstrapping in the above scheme affects the MCM through one capacitor, i.e.  $C_{P2}$ . The readout voltage  $V_{0\_BS1}$  is expressed in eq. 3-4 showing that  $C_{P2}$  is multiplied by the factor  $(1-A)$  and the signal is boosted.

$$V_{0\_BS1} = \frac{C_M \cdot V_B + (C_0 + C_{P2} + C_{P,IN} + C_M) \cdot V_N}{(C_0 + (1-A) \cdot C_{P2} + C_{P,IN} + C_M)} \quad (\text{Eq. 3-4})$$

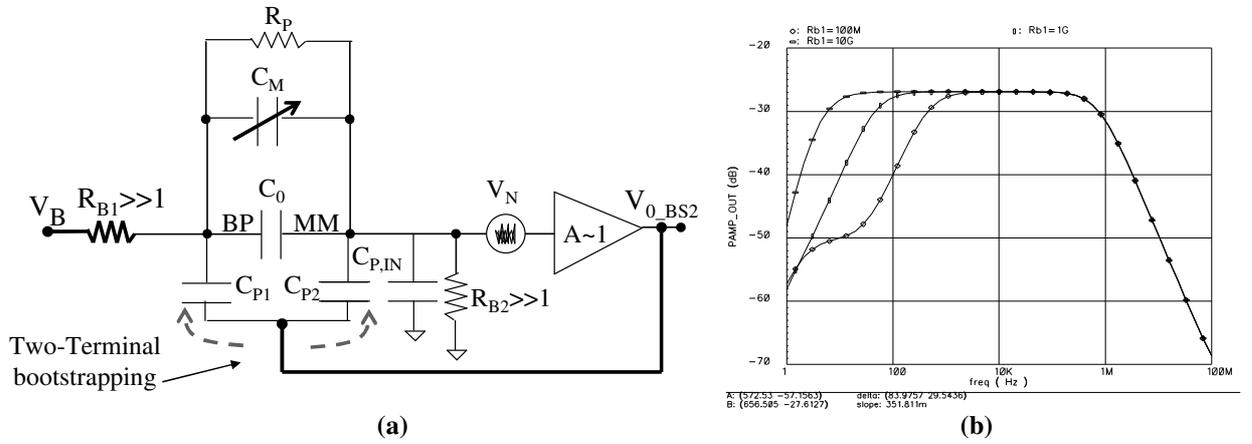
The signal-boost achieved through ST boosting is expressed in eq. 3-5, assuming that  $A=1$  and  $C_M \ll C_{T2}$ , where  $C_{T2} \sim C_0 + C_{P,IN}$ .

$$\text{Signal - Boost}_{ST1} = 20 \cdot \log\left(1 + \frac{C_{P2}}{C_{T2}}\right) \quad (\text{Eq. 3-5})$$

However, the noise  $V_N$  also gets multiplied with the same boosting factor, which is expressed in eq. 3-6. The intuitive explanation for the noise boosting is the re-cycling of the noise through the bootstrapped parasitic capacitor  $C_{P2}$  due to the positive feedback.

$$\text{Noise} - \text{Boost}_{ST1} = 20 \cdot \log\left(1 + \frac{C_{P2}}{C_{T2}}\right) \quad (\text{Eq. 3-6})$$

Single-terminal bootstrapping does not affect the parasitic nominal bias capacitance  $C_0$  since the node BP is a low-impedance node, connected directly to the bias  $V_B$ . The bootstrapped parasitic  $C_{P1}$  can be used to reduce the effective signal swing across  $C_0$  by making node BP a high-impedance node for ac-signal and, at the same time, keeping a proper dc-bias established there for proper polarization of the sensor. This can be done by connecting a high-value resistance  $R_{B1}$  between the bias source and the node BP, as shown in figure 3-6a. This topology is termed as two-terminal bootstrapping later in this text since it operates on the MCM through both parasitic capacitors. The readout voltage  $V_{0\_BS2}$  is expressed in eq. 3-7, assuming that  $A=1$  and  $R_{B1}, R_{B2} \gg 1$ .



**Figure 3-6 : (a) Two-Terminal Bootstrapping Scheme, (b) Frequency Response of the Bootstrapped PAMP for different values of bias resistor  $R_{B2}$**

$$V_{0\_BS2} = \frac{C_M \cdot V_B}{C_{P,IN} + C_M} + \left(1 + \frac{C_0 \cdot C_{P2} + C_{P1} \cdot C_{P2} + C_0 \cdot C_{P1}}{(C_M + C_{P,IN}) \cdot (C_0 + C_{P1})}\right) \cdot V_N \quad (\text{Eq. 3-7})$$

The signal-boost achieved through two-terminal boosting is expressed in eq. 3-8, assuming that  $A=1$  and  $C_{P1} \gg C_0$ ,

$$\text{Signal} - \text{Boost}_{ST2} = 20 \cdot \log\left(1 + \frac{C_0 + C_{P2}}{C_{P,IN}}\right) \quad (\text{Eq. 3-8})$$

Eq. 3-8 suggests that the signal boost can be controlled by controlling  $C_{P,IN}$ , which is contributed by the PAMP and the bonding-wires. Therefore, the size of input stage can be controlled to adjust the signal boost. However, as noise receives the same boost due to re-cycling, there is no SNR gain at the output of the bootstrapped PAMP. This signal boost; however, relaxes some of the design aspects of the subsequent SDM as discussed later.

To keep the extra pole caused by the resistance  $R_{B1}$  out of the audio band, its value should be above  $G\Omega$ . Figure 3-6b plots the response of the bootstrapped PAMP for different values of  $R_{B1}$ . At the same time, this extra resistor also makes the sensor operate in a charge-controlled manner, reducing the risk of dynamic pull-in for large low-frequency signals. For the sake of PAMP's stability, the gain of the PAMP should remain below unity, which is ensured by the source-follower topology.

The parasitic capacitors ( $C_{P1}$  and  $C_{P2}$ ) of the MEMS are not only difficult to estimate accurately but these parasitics might also exhibit variable values within audio-band due to dielectric relaxation. Therefore, relying on  $C_{P2}$  for providing a consistent signal-boost using two-terminal bootstrapping must be carefully evaluated. However, if  $C_0$  and  $C_{P2}$  are comparable, which is typically the case in MCM, the spread in the signal boost is not considerably large.

Figure 3-7a shows the output swing of the two-terminal bootstrapping scheme for 1Pa of input signal for both above-mentioned models of the microphone. It can be seen that both models predict a swing of  $\sim 40mV_{pp}$  for 1Pa of equivalent input. Figure 3-7b shows the SNDR at the output of the bootstrapped PAMP using both models again. The integrated output noise of the PAMP is assumed to be  $-100dB$ . The signal peak is at  $-34dB$  for a 1Pa signal, therefore, SNDR at 1Pa is  $66dB$ . This plot shows that the non-linearities in the MCM start dominating after 1Pa ( $94dB_{SPL}$ ).

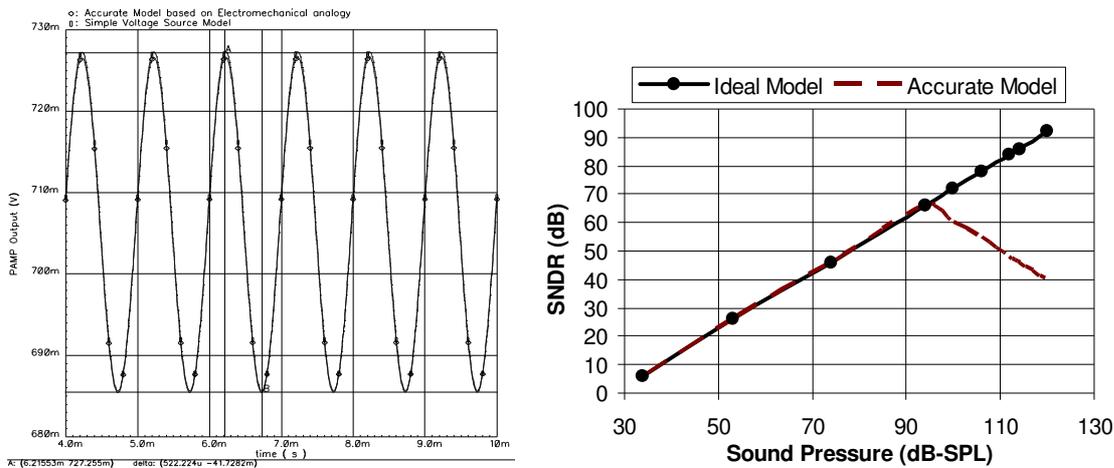


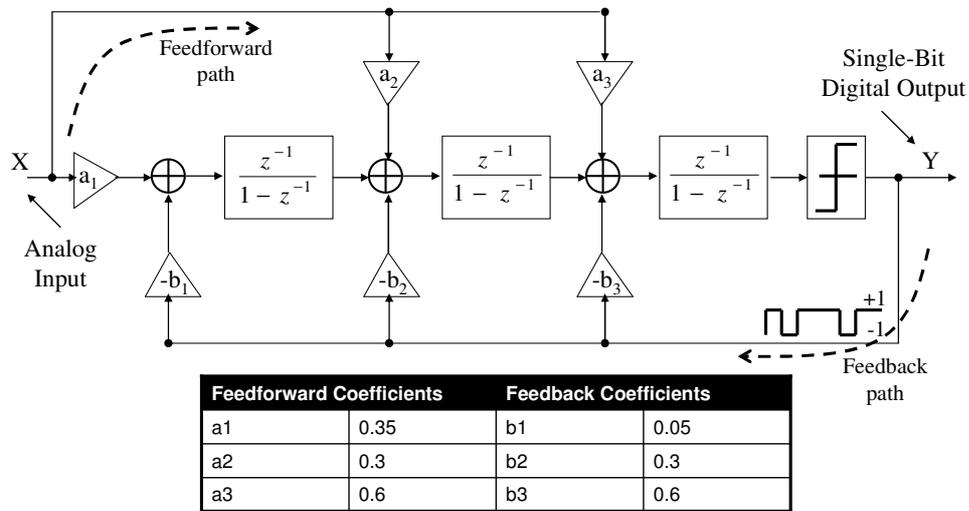
Figure 3-7 : Simulation Results of the Two-Terminal Bootstrapped PAMP for above-mentioned MCM Models, (a) Output Swing of the PAMP at 1Pa for both models, (b) SNDR predicted by both models

### 3.2.3 The Sigma-Delta Modulator

The targeted dynamic range for the under-consideration SDM is  $80dB-90dB$ . This corresponds to reading sound-pressure levels from  $1mPa$  ( $34dB_{SPL}$ ) up to  $20Pa$  ( $120dB_{SPL}$ ). The reference point, i.e.  $1Pa$ , is placed at  $-20dB_{FS}$ . Figure 3-8 shows the selected third order single-loop feed-forward SDM with single-bit quantizer. The targeted sampling frequency is around  $2.5MHz$ , giving an OSR of around 60 for the audio band (Bandwidth  $\sim 20kHz$ ). As mentioned above that for the desired OSR, a second-order modulator would require a multibit quantizer (4-bit) to achieve the required DR. Therefore, dithering

logic would be needed to randomize the nonlinearity of multibit second-order modulator's DAC into white-noise, which can be power-hungry. However, a third-order modulator can achieve the targeted DR with a single-bit quantizer, which is inherently non-linear and does not require dithering. A third-order modulator would need an extra OTA, consuming extra power. However, in a third-order modulator, the noise and imperfections of the second and third OTA are filtered by the first integrator; therefore, a weaker and less power-hungry OTA can be used for them. Thus, a third-order single-bit topology is preferred over second-order multibit topology in this case.

Feed-forward (FF) topology minimizes the signal swing at the output of the OTAs because it removes the signal from the integration path and only the quantization error flows through the chain. Furthermore, a distributed feedback along with FF topology provides the liberty of having an STF independent of the NTF. To reduce power consumption, the FF path to the quantizer is removed to save an extra analog adder. This alters the STF and now it is not unity but a low-pass function; however, within the audio band, it is 1, which is adequate for the requirements, with the savings of one OTA. The SDM is simulated in Simulink using the SD-toolbox [74] along with the listed practical constraints in figure 3-9b, which also shows the DR achieved by the SDMF. Figure 3-9a shows the noise floor of the SDM along with the induced constraints. NTF and STF of the SDM are shown in eq. 3-9 and eq.3-10.



**Figure 3-8 : Third-order, feed-forward single-loop single-bit SDM**

$$STF = \frac{0.6(z^2 - 1.5z + 1.08)}{(z - 0.77) \cdot (z^2 - 1.63z + 0.84)} \quad (\text{Eq. 3-9})$$

$$NTF = \frac{(z - 1)^3}{(z - 0.77) \cdot (z^2 - 1.63z + 0.84)} \quad (\text{Eq. 3-10})$$

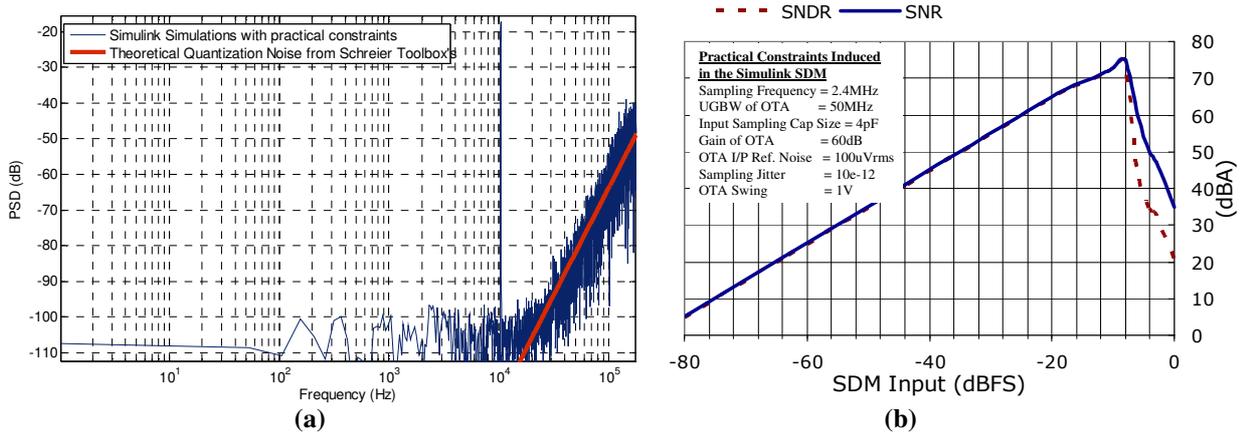


Figure 3-9 : (a) SDM Noise Floor and Signal Amplitude for 1Pa input with induced constraints, (b) DR achieved by the SDM

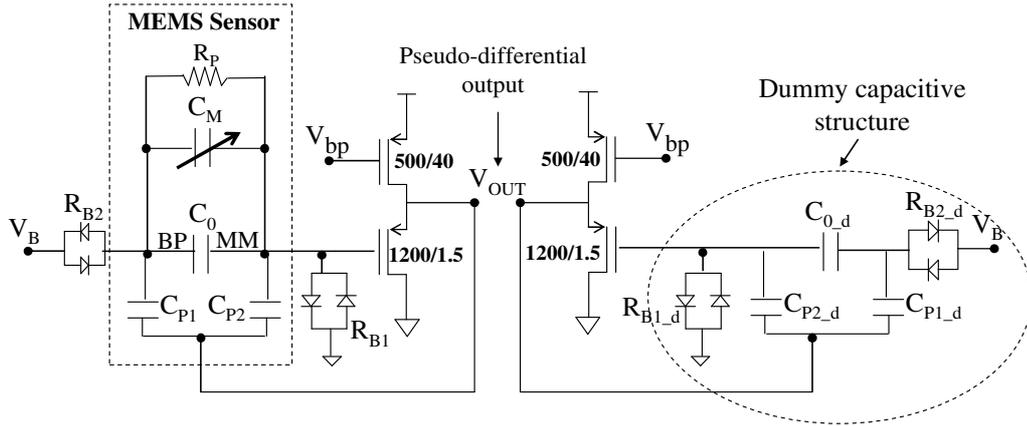
### 3.3. CMOS Design Details

This interface is designed in 0.35 $\mu$ m 2P/4M (double-poly quad-metal) CMOS technology with twin-well process. The targeted power-supply voltage is 1.8V. The circuit-level simulations of the system are performed using Eldo in Cadence design environment.

#### 3.3.1 The Preamplifier

The constant-charge voltage-readout scheme based on two-terminal bootstrapped topology using a source-follower buffer is shown in figure 3-10 and its CMOS design details are discussed in the following text. The source-follower has a PMOS input-device and PMOS current-source as active load. The SDM that follows the PAMP is fully-differential and the MCM is single-ended, therefore, the PAMP converts a single-ended input from the MEMS into a pseudo-differential output by employing a dummy-branch, which replicates the capacitive structure of the MCM along with a dummy source-follower buffer [75].

The theoretical sensitivity of the under-consideration IRST MCM in this case is 5fF/Pa @ 1kHz, which along with parasitic capacitors of the sensor (listed in table 2-1) translates into 4.5mV<sub>pp</sub>/Pa (or -53dBV/Pa), for a bias voltage of 7V. To achieve the standard 60dBA (@1Pa,1kHz) of SNR at the output of the PAMP, the integrated input referred noise (for a band of 20-20kHz, a-weighted) of the pre-amplifier must lie below 1.6uVrms (-116dB).



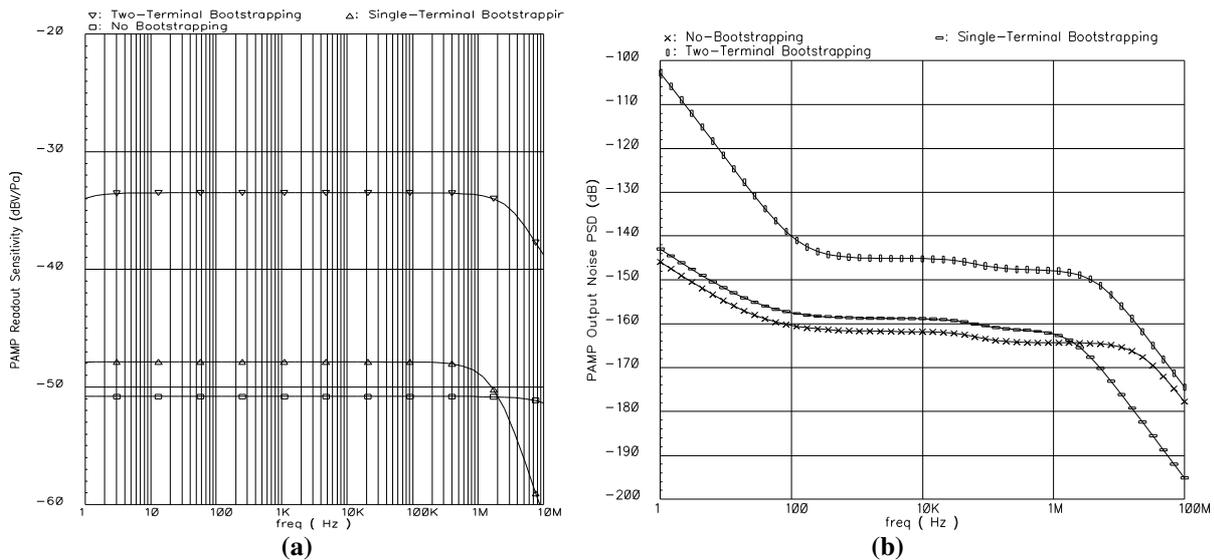
**Figure 3-10 : Source-Follower PAMP with two-terminal bootstrapping, along with the dummy capacitive structure and dummy buffer**

Since the audio-band extends down to 20Hz, the flicker noise of the devices can become a bottleneck. To minimize the flicker noise, a large device area is utilized for the input PMOS. The  $g_m$  of the input device should also be higher to have a low input-referred noise, unlike the PMOS current sources that should have low  $g_m$  to have lower thermal noise. Therefore, the length of the input PMOS is kept lower while increasing its width to increase the area. However, as the device dimensions of the input PMOS increase, the parasitic capacitance at the sensing node ( $C_{P,IN}$ ) also increases, decreasing the readout sensitivity. Therefore, a trade-off exists giving rise to an optimal size that maximizes the SNR [27,32]. Through several iterations, the device dimensions of  $1200\mu\text{m}/1.5\mu\text{m}$  are set to achieve a balance between flicker noise and parasitic capacitor for the targeted sensitivity. To reduce PMOS current-mirror flicker noise, their lengths are increased since it is better to have a reduced- $g_m$  for them. The size of the PMOS current source is  $500\mu\text{m}/40\mu\text{m}$  and it carries a current of  $40\mu\text{A}$  per branch.

Figure 3-11a and 3-11b show the simulated signal and noise, respectively, at the output of the PAMP for all three configurations; i.e. no-bootstrapping, single-terminal bootstrapping and two-terminal bootstrapping. The signal boost achieved through two-terminal bootstrapping is  $\sim 18\text{dB}$ , considering  $1\text{pF}$  of extra grounded parasitic capacitor due to the bonding wire. The expected sensitivity at the output of the PAMP is  $-34\text{dBV/PA}$ , as shown in figure 3-11a. The simulated noise of the PAMP with all three bootstrapping configurations is listed in table 3-1.

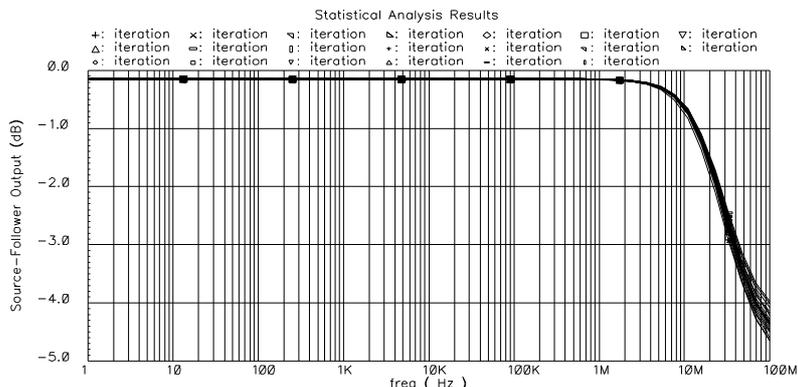
**Table 3-1 : Noise of the Preamplifier for all configurations of the Bootstrapping**

Noise Of the PAMP for all configurations of bootstrapping		
Configuration	Integrated Output Noise (A-weighted)	Major Contributors
No-bootstrapping	750nV <sub>rms</sub>	Input pairs thermal noise (80%)
1T-bootstrapping	1.6uV <sub>rms</sub>	Input pairs thermal noise (80%)
2T bootstrapping	7uV <sub>rms</sub>	Input pairs thermal noise (80%)



**Figure 3-11 : (a) Signal-Amplitude at the output of PAMP for all bootstrapping configurations, (b) Noise of the PAMP for all bootstrapping configurations**

Zero-biased diodes are used to implement the bias resistor  $R_{B1}$ . The size of these diodes at sensing node also affects the total noise of the PAMP [32]. Smaller diode offers lower leakage current and higher resistance, hence a lower cut-off corner for the diode-induced noise. Furthermore, a large size of these diodes can reduce the readout sensitivity by causing increased parasitic capacitances at the sensing node. However, a critical point to note is that there is a parasitic resistor (3TOhms) between backplate and the moving membrane of the sensor [20]. As a result, a dc current ( $\sim 2.5\text{pA}$ ) flows from backplate down to the ground, passing through the sensing node. The biasing diodes are kept large enough to sink this dc current while maintaining the sensing node below 10mV otherwise the node would ramp up to a higher value disturbing the operating point of the PAMP. These diodes are implemented using NPN bipolar transistors by shorting their base and collector terminals. This is done intentionally to utilize the large size of the collector to implement a large diode utilizing smaller devices. This also helps to minimize substrate-coupled noise reaching the diodes, where n-well serves as isolation. The active parasitic compensation through bootstrapping and the stability of the PAMP depends on the gain of the source-follower. Figure 3-12 shows the spread of gain in SF for different process variations and mismatch.



**Figure 3-12 : Spread in the gain of the Source-Follower for corner cases**

### 3.3.2 The Sigma-Delta Modulator

Figure 3-13 shows the switched-capacitor schematic for the third-order single-loop feed-forward SDM single-loop single-bit SDM. The feed-forward and feedback paths are implemented using separate capacitors and MIM capacitors are used to implement the capacitors in the structure. This relaxes the settling requirements of the OTA since the larger input sampling capacitors do not have to switch back and forth between the reference voltages, and the feedback caps. The sampling capacitors in feed-forward paths are larger than feedback capacitors to have low KTC noise. The feedback path contains an extra switch, to select between positive and negative feedback reference ( $V_{R+}/V_{R-}$ ); therefore, slightly larger device sizes are used in feedback path switches. The switches are transmission gate switches, with a peak resistance of  $4k\Omega$  to achieve a timing constant which is 10-times smaller than sampling period to achieve the required settling accuracy.

The feedback reference voltage of the sigma-delta modulator are reduced to  $\pm 0.5V$  (across mid-rail, i.e.  $900mV$  for a power supply of  $1.8V$ ), and the feedback capacitors are rescaled according to get a feedback of  $\pm 1V$ . The bootstrapped PAMP gives  $20mVp$  swing at  $1Pa$ . To translate the output of PAMP@ $1Pa$  to  $-20dB-FS$  ( $100mVp$ ) of the SDM, the required gain factor is achieved by increasing  $C_{S1}$  by 7-times, which also helps in lowering their KTC noise. Without bootstrapping in the PAMP, the translation factor would have been 50, giving rise to very large sampling capacitors and therefore, more power consumption in the first stage of SDM. Same OTA is used for all three stages in the SDM. First integrator has reduced output swing but the capacitors around it are large to keep the KTC noise low. The third integrator has smaller capacitors but the output swing is large. Therefore, all the integrators have almost the same settling requirements for the OTA.

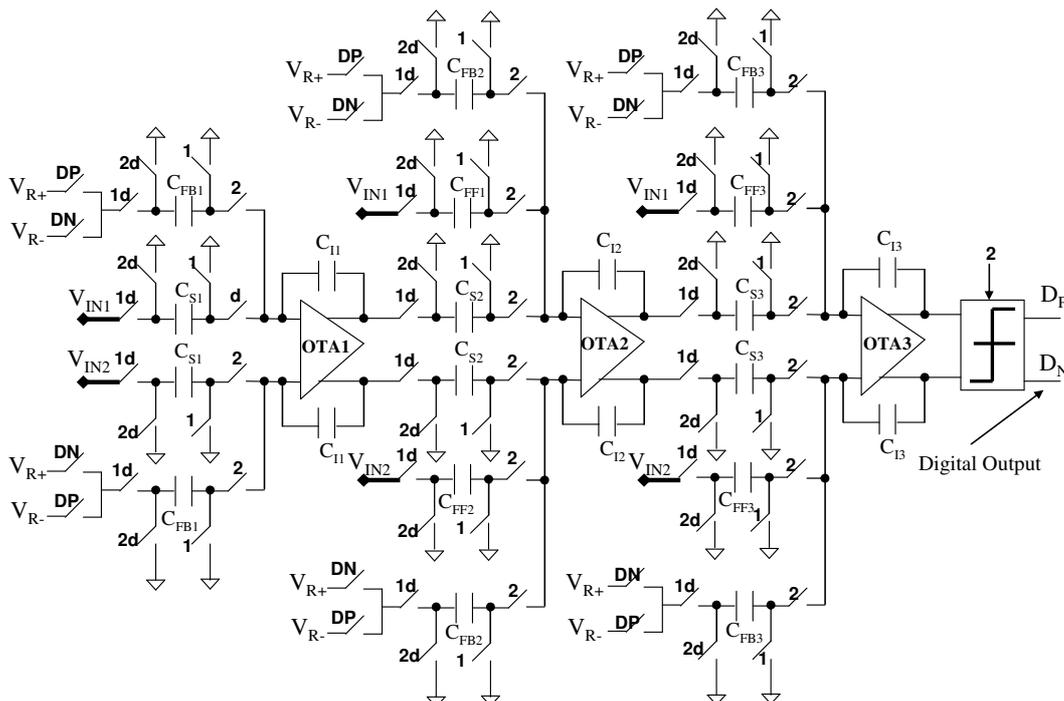


Figure 3-13 : Schematic of the Switched-Capacitor third-order SDM

Delayed clocking scheme is used in SDM to minimize the distortion due to charge-injection from switches. The switches connected to the virtual-ground node switch between the analog-ground and the virtual-ground, therefore, injecting a fixed-amount of charge every cycle, causing a dc-offset. However, the sampling switches can cause signal-dependent charge-injection and therefore distortion. The sampling switches are delayed, so when they switch-off, the other switch completing the sampling path had already been turned-off. Thus, the injected charge sees a high-impedance path towards the sampling capacitance and is mostly absorbed by the other low-impedance side that is either connected to analog-ground or to the output of the PAMP [92].

### The Telescopic OTA for SDM

A fully-differential output swing of more than 1V, gain above 40dB, UGBW above 50MHz and slew-rate above  $2V/\mu s$  are required to achieve the targeted dynamic range, as suggested by the Simulink simulations shown above. The technology under use has a threshold-voltage ( $V_T$ ) of around 500mV-600mV for both NMOS and PMOS. A telescopic OTA, shown in figure 3-14a, achieves a differential-swing of 2V for a power supply of 1.8V. The current-sources are allocated an overdrive of 200mV, while cascodes operate with 100mV of overdrive. The OTA is biased by a total current of 20uA, i.e. 10uA flows in each branch. The resulting differential gain is 74dB and the phase margin is  $60^\circ$ , the slew rate is  $3V/\mu s$  and the unity-gain-bandwidth (UGBW) is 100MHz. The UGBW is kept slightly higher since the OTA would be loaded by sampling capacitors of the subsequent stage in the SDM. The OTA uses a switched-capacitor common-mode feedback (CMFB) circuit since it is compatible with the inherent switched nature of the SDM and it does not incur swing and stability problems which arise in a CT-CMFB. Minimum-sized switches are used in CMFB to reduce their charge injection. The sizes for capacitors of the CMFB are decided based on minimizing the CMFB KTC noise without seriously loading the OTA [93]. The gain and phase of OTA are shown in figure 3-14b. Figure 3-15 shows the swing and the slew-rate of the OTA.

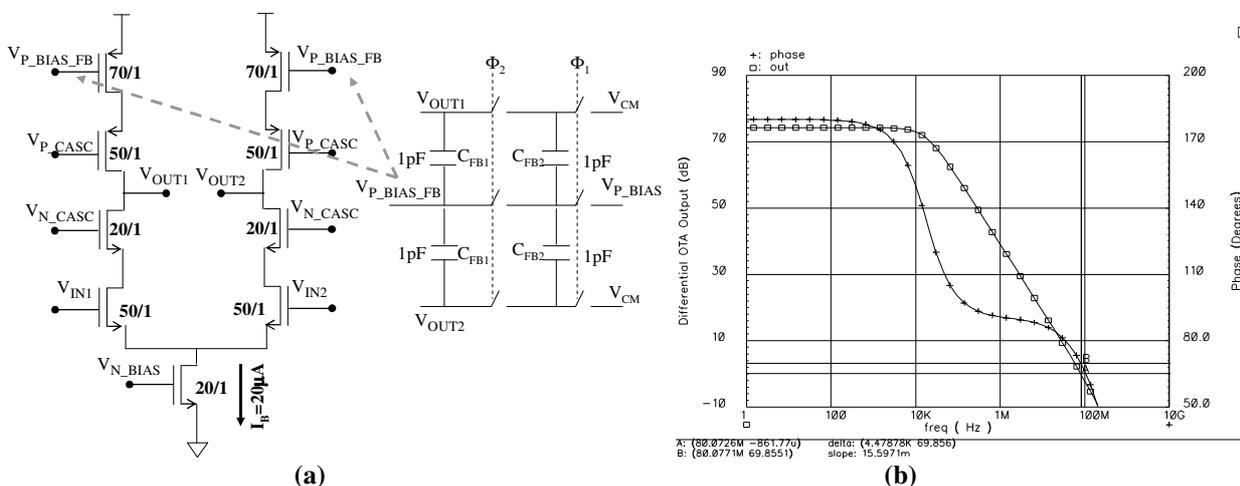


Figure 3-14 : (a) Telescopic OTA with SC-CMFB for SDM, (b) Gain and Phase of SDM OTA

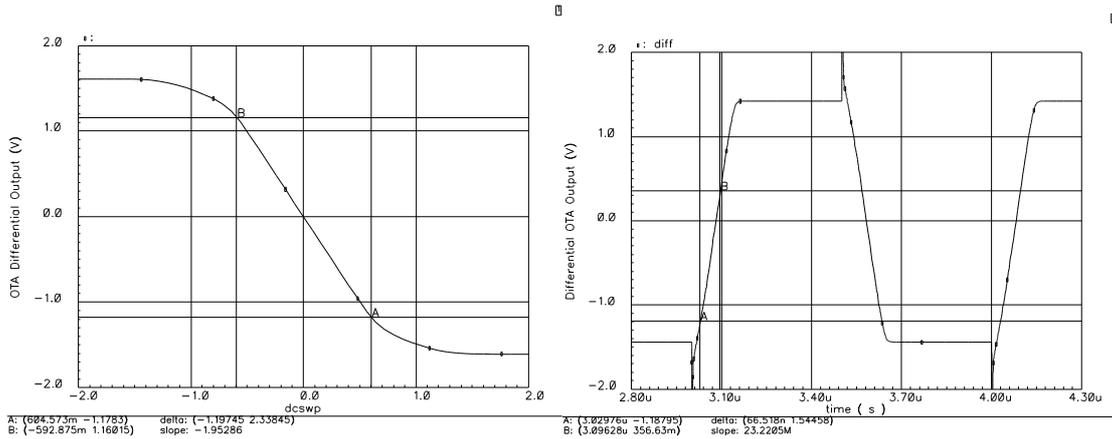


Figure 3-15 : Output swing and Slew-rate of the OTA

### Comparator for the SDM

The clocked comparator for the SDM is shown in figure 3-16 and it offers three main advantages. First, the static power consumption is minimal. Second, it requires single phase of clock. Third, the offset is dominated by the offset of the input pairs instead of cross-coupled regenerative loads since the input is substantially amplified before the regenerative gain comes into play [76].

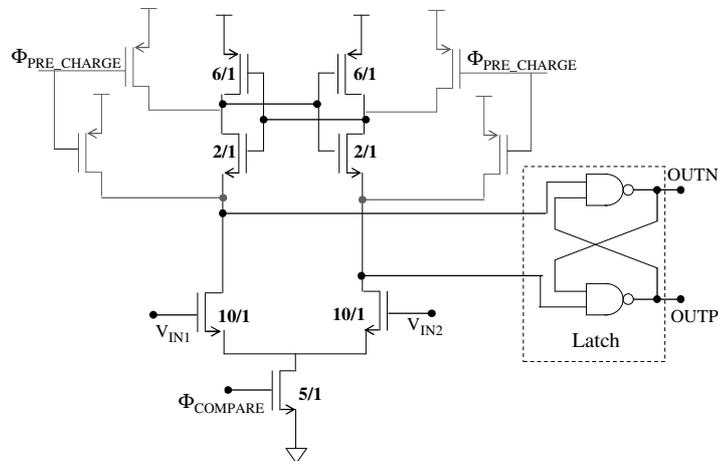


Figure 3-16 : Clocked-Comparator for SDM

### 3.3.3 The Bias Block

This block, shown in figure 3-17, generates all the required reference voltages in the ASIC, which include feedback references for the SDM, the mid-rail analog-ground reference, common-mode reference for the OTAs and the charge-pumping reference voltage for the charge-pump. A non-inverting amplifier controls the voltage at the top of a resistor-ladder. A current of 60μA is flowing through the resistor ladder. The resistive partitioning produces the required reference voltages. Large capacitors ( $C_{L1}, C_{L2} \sim 50\text{pF}$ )

are used to load the generated references to improve their impulsive-current drive, reducing voltage glitches when switching occurs in the SDM.

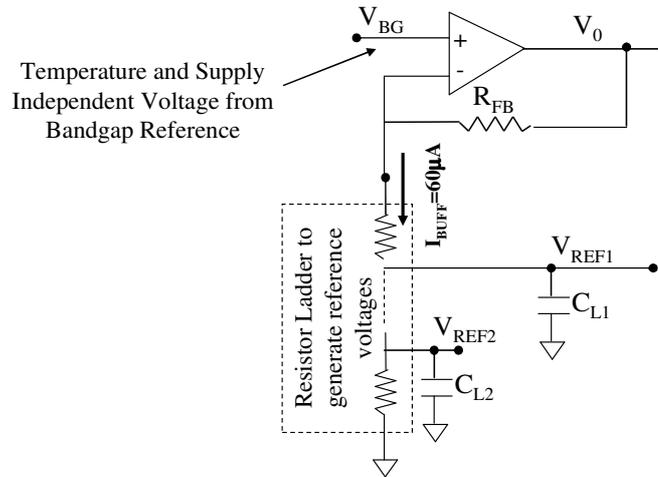


Figure 3-17 : Bias Voltage Generation

### 3.3.4 The Charge-Pump

The charge-pump (CP) comprises of six cascaded stages based on cross-coupled static charge-transfer-switches, as shown in figure 3-18. This scheme of charge-pump alleviates the problem of reduced pumping-gain that is commonly found in Dickson chargepump. It is also suited for low-voltage technologies since it does not create high-voltage stress across successive stages which can raise reliability issues [77]. The CP is clocked at a rate four-times lower than the SDM frequency. This is done to avoid overlapping of the sampling phase of SDM with the CP switching, keeping the switching noise from entering the signal path. A large capacitor (~30pF) at the output of the CP is integrated onchip to reduce the switching glitches. At the same time, the large parasitic at the back-plate of the sensor is expected to further dampen the high-frequency switching glitch. The size of the capacitors inside the CP is traded-off with a higher pumping frequency, therefore, reducing the overall area. Figure 3-19 shows the simulated output of the CP ramping-up to final value ~7V, which is the required bias for the under-consideration MCM.

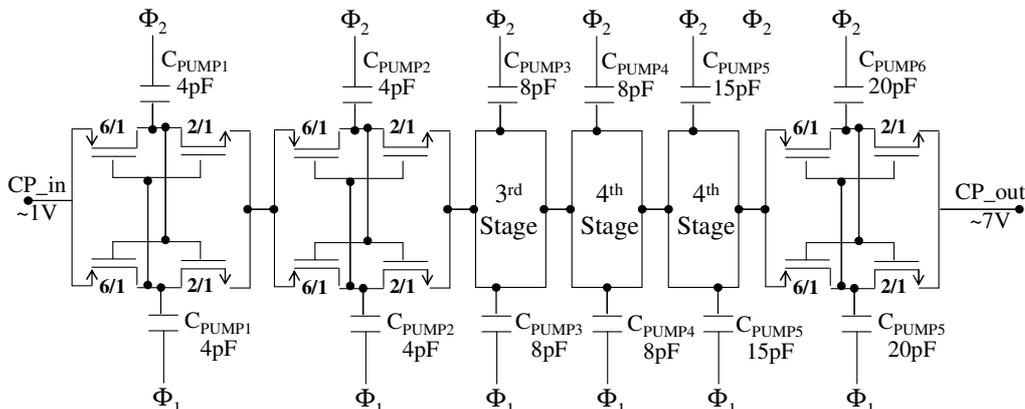


Figure 3-18 : Charge-Pump using six cascaded stages of cross-coupled static charge-transfer-switches

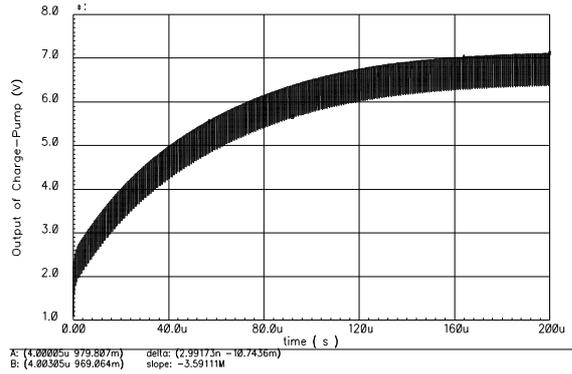


Figure 3-19 : Simulated Output Voltage of the Charge-Pump

### 3.3.5 The Bandgap Reference

The bandgap block (BG) generates a temperature and supply -independent voltage reference. BG block is based on error-amplifier closed-loop topology, as shown in figure 3-20. The negative temperature coefficient is provided by the  $V_{BE}$  of the bipolar transistor while the positive temperature coefficient comes from the difference of the base-emitter voltage of two branches. The self-biased error amplifier attempts to keep the nodes amp\_in1 and amp\_in2 at the same voltage. This balance results in a temperature independent reference voltage  $V_{REF}$ , according to eq. 3-11 and eq. 3-12.

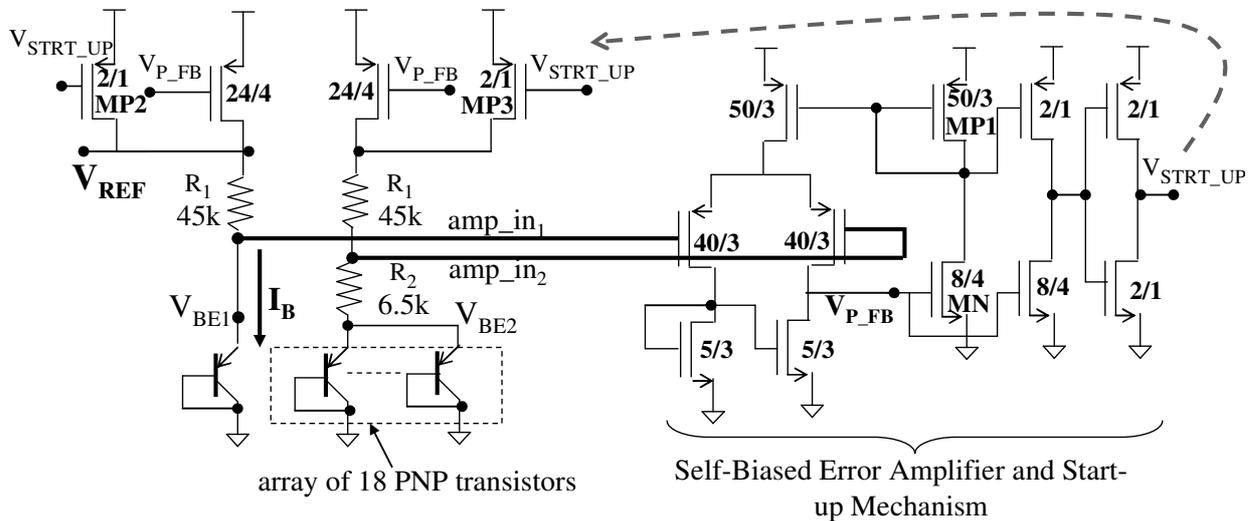


Figure 3-20 : BandGap based on Self-Biased Error-Amplifier Scheme

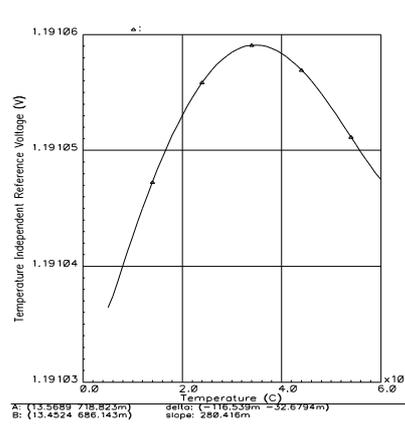


Figure 3-21 : Simulated Response of the Bandgap Reference

$$V_{REF} = V_{BE1} + V_{R1}, V_{R1} = I_B \cdot R_1, I_B = \frac{(amp\_in1 - V_{BE2})}{R_2}, \quad (\text{Eq. 3-11})$$

$$\Rightarrow V_{REF} = \underbrace{V_{BE1}}_{\text{Negative Temperature Coefficient}} + \underbrace{\frac{R_1 \cdot (V_{BE1} - V_{BE2})}{R_2}}_{\text{Positive Temperature Coefficient}} \quad (\text{Eq. 3-12})$$

The positive temperature coefficient is smaller than the negative coefficient and depends logarithmically on the number of BJTs used in the second branch. Hence to match both the coefficients, an array of BJTs is used in the second branch. The positive temperature can also be boosted by ratio between  $R_1$  and  $R_2$ . However, the size of these resistors define the bias current in the branches, therefore, it is important that the resistors do not limit the current so much that the control loop fails. The error amplifier is a self-biased amplifier carrying a bias current of  $8\mu\text{A}$ . When the power supply is turned on,  $V_{P\_FB}$  gradually ramps up, turning on MN, which turns on MP. MP mirrors bias current in error-amplifier and the loop eventually stabilizes itself and the amplifier transistors enter saturation. However, at the same time, it is necessary that inputs of the amplifier i.e.  $amp\_in1/2$  reach a reasonable value, for the amplifier to stabilize. This is done by adding MP2 and MP3 in parallel with PMOS current sources of the bandgap circuit. At power-up MP2 and MP3 are on, gradually pushing  $amp\_in1/2$  high, and eventually turn-off once the whole circuit has stabilized. The interface has a sleep-mode in which all the components are powered-off; however, bandgap is not turned off in the sleep mode. This is done not to disturb the start-up sequence of the bandgap. The curvature of the reference voltage temperature is centred between  $30^\circ\text{C}$  and  $40^\circ\text{C}$  since the internal temperature of the ASIC is typically higher than room temperature, as shown in figure 3-21.

### 3.3.6 Output Buffer and Power-Down Logic

The output buffer is a tri-state buffer which drives the output only in one of the selected phases of the system clock. This is done to have the possibility of multiplexing left/right channel multiplexing on a single output line. The power-down logic monitors the clock frequency. If frequency goes down below 50kHz, it places the ASIC under sleep-mode. The power down block uses the positive-edges of the system clock to charge an RC network, as shown in figure 3-22. If the edges are frequent-enough, the RC circuit is charged up and maintained there. Otherwise, low-frequency clock would cause the RC circuit to discharge asserting the SLEEP signal. In the sleep mode, the main voltage reference generated by the bandgap is disconnected from rest of the ASIC, therefore, turning the ASIC off, apart from the bandgap. The bandgap is not forced to sleep mode not to disturb its power-up sequence.

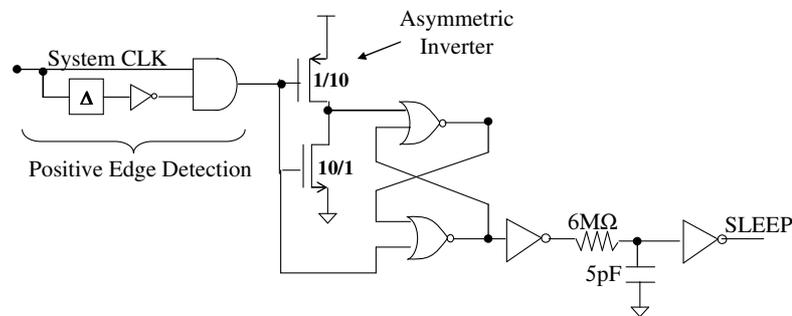


Figure 3-22 : Power-Down Logic based on the detection of Clock-Frequency

## 3.4. Measurement Results

### 3.4.1 Measurement Setup

Figure 3-23a shows the microphotograph of the ASIC with dimensions of 750μm x 1400μm. The power-supply and the clock are provided by on-board regulators and oscillators respectively, which is shown in figure 3-23b. The measurement setup is depicted in figure 3-24. The analog output of the PAMP is fed to an instrumentation amplifier; INA111. The output of INA111 is fed to the sound-card of PC through line-in and its spectrum is analyzed and post-processed in software SpectraLab. The INA111 serves two purposes here. First, it converts the differential output into a single-ended output. Second, it serves as a buffer to the ASIC. The sound-card line-in has an input impedance of around 1kΩ, which can severely load the output of the ASIC. Therefore, INA111 takes on the responsibility of driving the sound-card. The digital over-sampled PDM output of the SDM is sampled using Agilent 1670G Logic-Analyzer and is post-processed in Matlab.

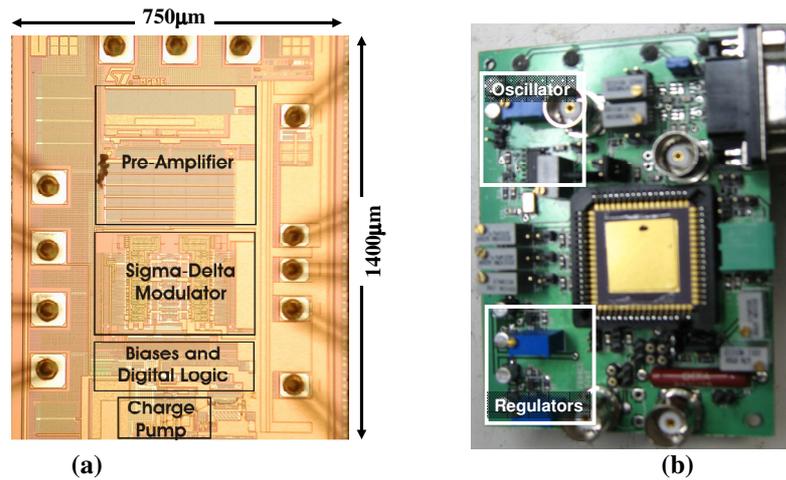


Figure 3-23 : (a) Microphotograph of the Readout Interface ASIC, (b) ASIC mounted on the

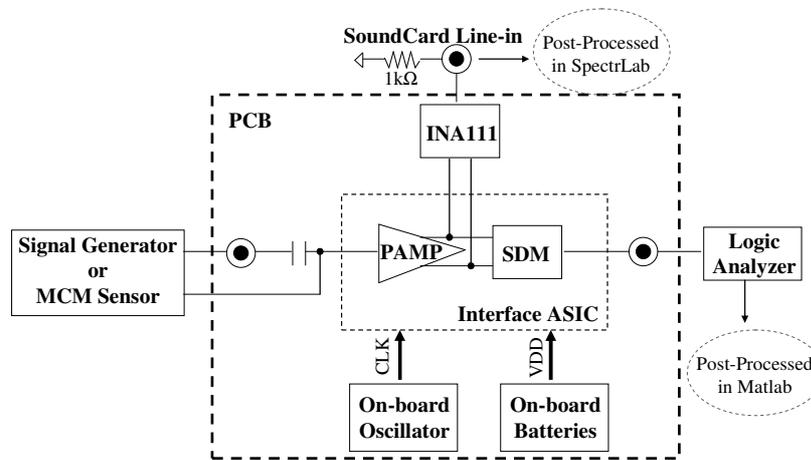
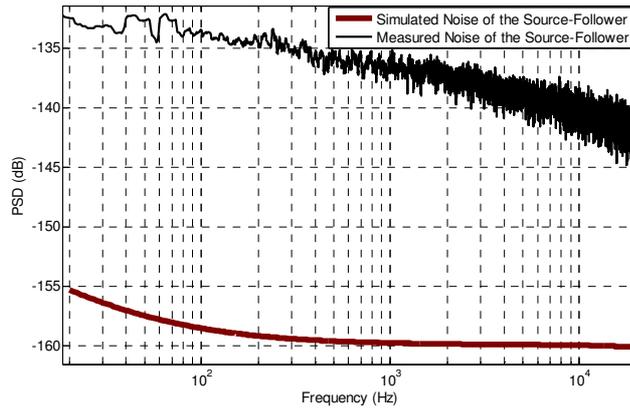


Figure 3-24 : The Measurement Setup

### 3.4.2 Electrical Measurement Results

#### Standalone Preamplifier

Figure 3-25 plots the measured noise of the source-follower PAMP when its input is connected to ground through a 5pF capacitor. It must be noted that in this measurement the instrumentation is hitting its measurement limits. The sound-card employs 16-bit sampling. The INA111 amplifier is used to amplify the output of the SF, to bring it to the dynamic-range of the PC’s sound card. The INA111 itself has a flicker noise corner of 1kHz starting at 500nVrms/ $\sqrt{\text{Hz}}$  (-126dB) and settling down to thermal noise of 80nVrms/rtHz (-140dB). The INA111 provides a gain of 40dB to the output of PAMP, which is normalized back to its original value in Matlab.



**Figure 3-25 : Measured and Simulated Noise at the output of the Source-Follower PAMP**

The noise spectra in figure 3-25 starts off as flicker noise, with a slope of 10dB/decade; however, the PAMP's flicker corner is around 1kHz, similar to the instrumentation amplifier, therefore, a decrease in the slanting slope is evident after 1kHz. However, instead of becoming completely flat after 1kHz at a certain thermal noise level, the output noise of the SF keeps slanting down slowly, i.e. 5dB/decade. The reason for this could be either the loading of the SF by the SDM sampling or the SDM kickback effect, limiting the bandwidth of the SF, the other reason could be the loading of the instrumentation amplifier by the sound card giving a slight attenuation for higher frequencies. To check the first reason, the SDM clock is externally reduced; however, this does not cause any considerable change in the noise spectrum. The clock frequency can only be reduced till 50kHz and SDM cannot be shut down completely since the chip would enter sleep mode below that frequency and the SF would also turn off. However, inspection of the loading effect of the instrumentation amplifier by the PC's sound card reveals that this slow slope is due to that loading. As mentioned, -140dB is the measurement limit of the instrumentation amplifier, therefore, even if the SF settles below that, it is not possible to measure it with this setup.

To test bootstrapping, discrete capacitors are used to emulate the MEMS sensor. To minimize the impact of board parasitics on the bootstrapping, the external capacitors are kept two-times higher than the values in the original sensor; however, maintaining the same ratio among the capacitors. Figure 3-26 shows the effect of single- and two-terminal bootstrapping on the output noise of the PAMP. Figure 3-27 shows the boosting of the noise due to the bootstrapping. The values of external capacitors used to emulate the MCM are kept close to twice of the actual sensor capacitors listed in table 2-1. It can be seen that the bootstrapping boosts the noise due to the noise re-cycling, as explained above, by the same factor as the signal boost. The exact factor of noise boosting again depends on the capacitor ratios and the uncompensated parasitic capacitor at the sensing node.

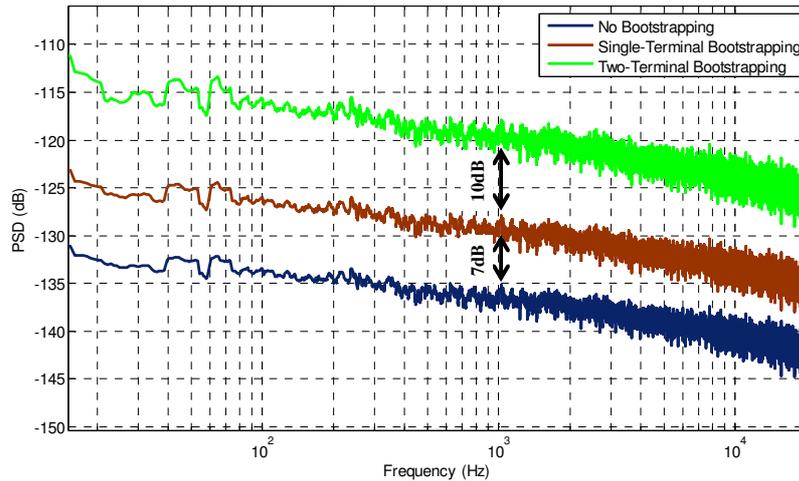


Figure 3-26 : Measured noise at the output of the PAMP for different bootstrapping configurations

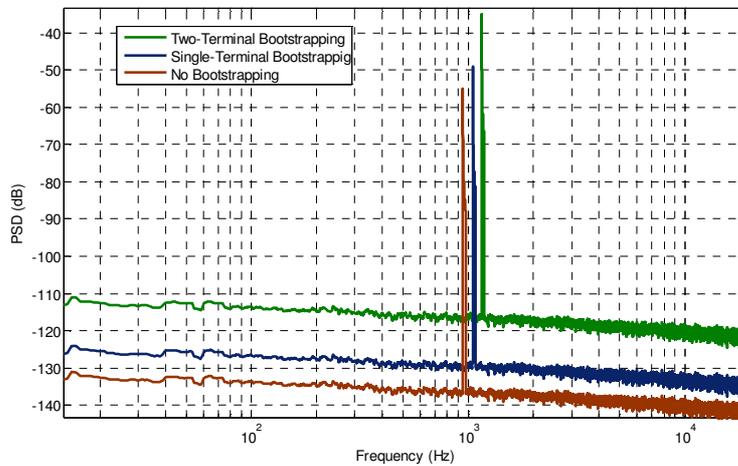
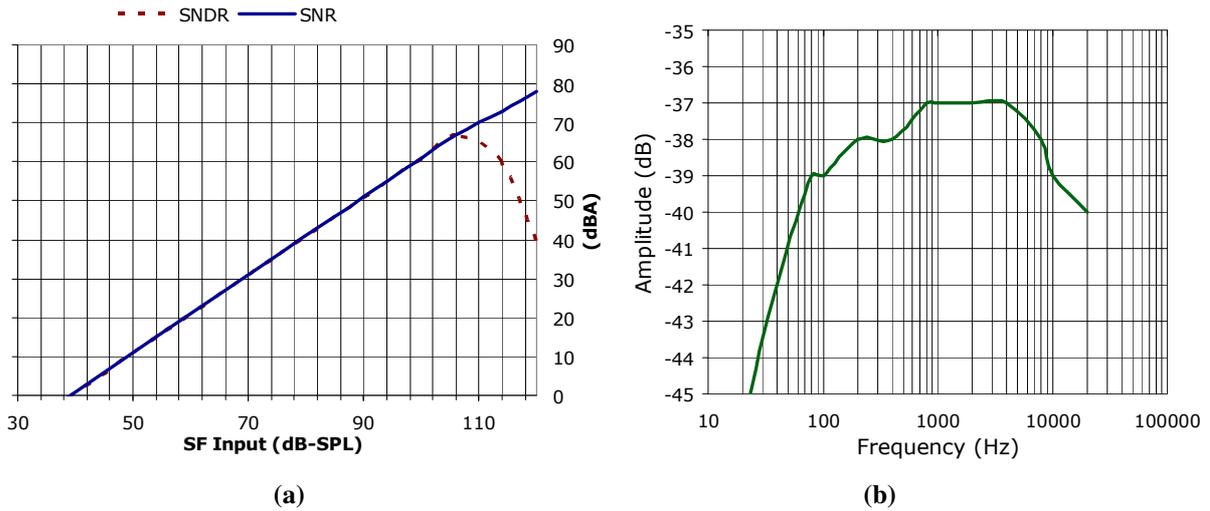


Figure 3-27 : Signal-Boost at the output of the PAMP for different bootstrapping configurations

Table 3-2 : Measured Signal Boost with emulated Sensor for different Bootstrapping Configurations

Measured Signal Boost with emulated Sensor for different Bootstrapping Configurations		
Configuration	Signal Amplitude (dB)	Signal Boost (dB)
No-bootstrapping	-55	0
1T-bootstrapping	-49	~6
2T bootstrapping	-37	~17

The SNR and SNDR at the analog output of the SF, with bootstrapped capacitive structure, are shown in figure 3-28a, against the corresponding sound-pressure-level, where 1Pa (94dB-SPL) represents 4.5mVpp at the input of the SF for the under-consideration MCM. The distortion at the output of the SF is mainly due the zero-biased diode at the input node, which basically is a dynamic resistor and exhibits lower resistance if the signal swing across it increases. Since the swing at the input of the source follower reaches around 400mV for 114dB-SPL (10Pa), this resistor causes signal clipping and therefore causes distortion at the output. Figure 3-28b shows the frequency response of the PAMP.



**Figure 3-28 : (a) DR of the PAMP, (b) Frequency-Response of the PAMP**

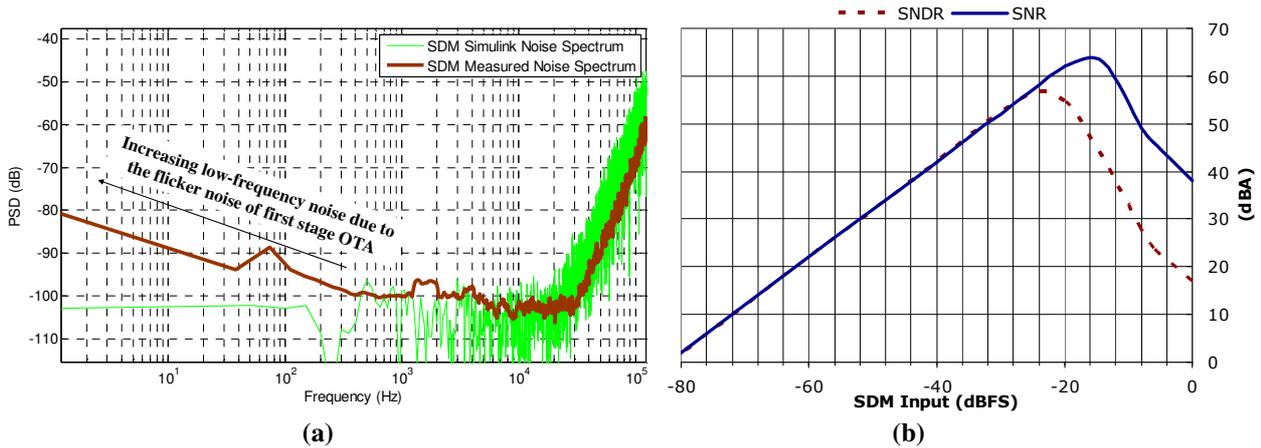
The pseudo-differential output of the PAMP has a dc offset as shown in table 3-3. The dummy branch of the PAMP is bootstrapped inside the chip using MIM capacitors, as explained above. These MIM capacitors have a certain leakage profile and which can cause a slightly different dc level at the input of the dummy branch. Another factor could be the passage of the CP switching noise through the dummy noise nominal dc-bias capacitance, which can also cause a dc mismatch between two branches.

**Table 3-3 : DC Offset at the Output of Pseudo-Differential Preamplifier**

Sample	Mismatch at the analog output of the PAMP
1	5mV
2	2.5mV
3	2mV

## Standalone Sigma-Delta Modulator

The SDM is tested stand-alone for the following results, i.e. the electrical input is directly provided to the SDM, bypassing the PAMP. Figure 3-29a plots the measured noise of the SDM along with the simulated noise. The measured integrated noise in audio-band is -79dBA, 6dB higher than expected. It can be seen that for frequencies below 4kHz, the measured noise of the SDM is higher than expected. This can be attributed to the flicker noise of the first OTA that is used to implement the first integrator in the SDM. The corner of this flicker noise is around 4kHz. Figure 3-29b plots SNR and SNDR against the input for SDM, highlighting 80dB dynamic range. The measured FOM of the sigma-delta is  $0.57 \times 10^{-3}$  [56].



**Figure 3-29 : (a) Measured and Simulated Noise of the standalone SDM, (b) Measured SNR and SNDR of the standalone SDM**

### The Complete Interface

Figure 3-30a plots the SNR and SNDR of the digital output of interface with the electrical input applied to the PAMP, which subsequently drives the SDM. Figure 3-30b compares the results of 3-30a with the expected results. The first thing to observe is that the distortion starts dominating much earlier than expected, lowering the SNDR from -20dBFS onwards. The simulated results predict domination of distortion mainly due to overload effect and the limited output swing of the SDM OTAs after -12dBFS. One reason of increased distortion in the measured results could be due to the fact that the bias voltages of the OTA cascade devices are higher than expected and are limiting the swing. This is checked by lowering the current consumption of the OTAs externally, which would ultimately lower the cascode biases.; however, this does not affect the distortion. Inspection of the FFT plots reveals that second-harmonics are the dominant source of distortion in the measured results. This points to imperfect matching in the fully-differential structure of the SDM and can be attributed to the way layout is performed. The capacitors inside the SDM structures are not properly matched and are placed far away from each other, making them prone to cross-chip gradients. At the same time, the input pairs and the current loads for OTA are not inter-digitated. Therefore, this distortion is highly likely due to mismatch in the layout and not because of the limited OTA swings or PAMP.

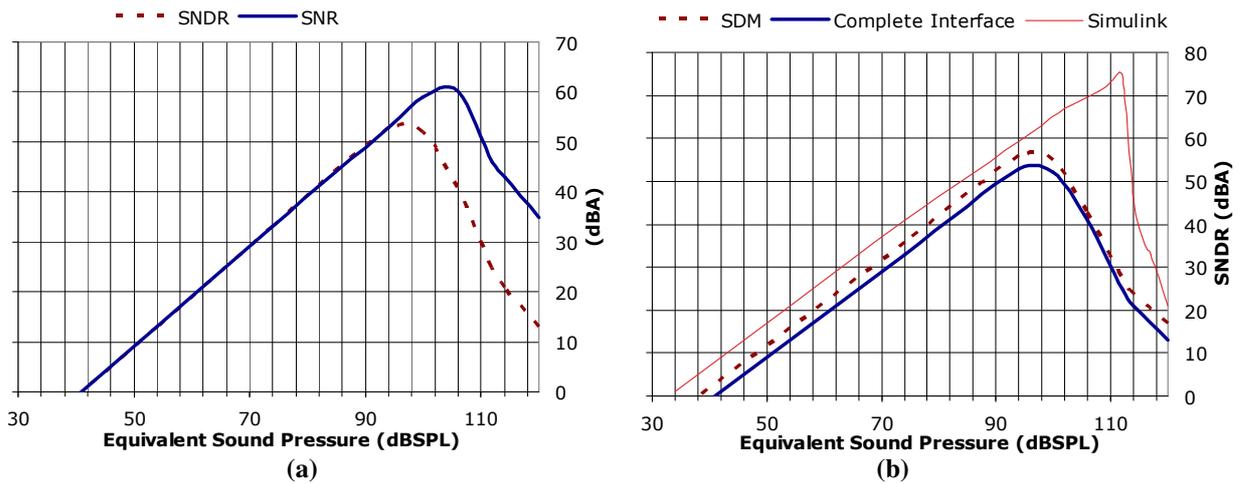


Figure 3-30 : (a) Measured SNR and SNDR for the complete interface, (b) Comparison among simulated and measured SNDR for the complete interface

## The Charge-Pump

The output of the charge-pump is measured through the INA111 amplifier and oscilloscope since a normal-voltage probe would load the charge-pump. Figure 3-31a shows the voltage level reached by the CP, i.e. 5.8V, which is  $\sim 1.2V$  less than expected. Figure 3-31b zooms in to the CP output to check if there are high-frequency switching spurs. The loss in the output voltage of CP can be attributed to two factors. First, the non-overlapping period between the two complementary boosting signals of the CP is not large enough and the  $V_{TH}$  of the MOS transistors could be higher, resulting in a decreased charge-pumping gain per stage. Second, the spread and mismatch in the CP capacitors might also give rise to a reduced charge-pumping gain per stage since no particular schemes were employed to match the CP capacitors. It can be noted that the high-frequency glitches are not considerable; therefore, the switching noise of the CP has been successfully attenuated by the internal loading capacitors.

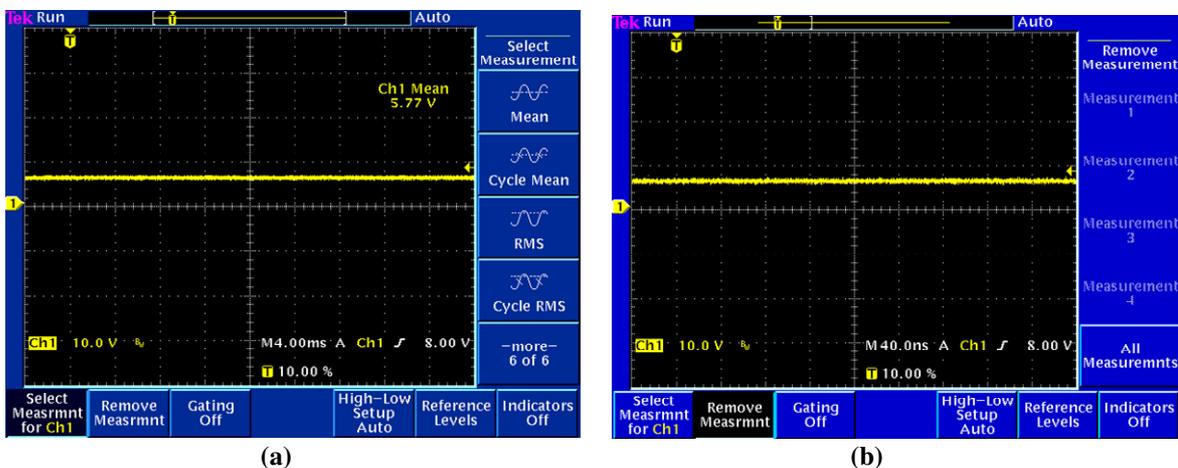


Figure 3-31 : (a) Measured CP output  $\sim 6V$ , (b) Zooming in to the CP output to check switching-noise

### 3.4.3 Acoustic Measurement Results

The initial acoustic tests for the readout interface are performed using Knowles-SiSonic analog MEMS microphone. This test is not performed in an anechoic room; however, an adequate degree of acoustic shielding is achieved by enclosing the setup in a box. The acoustic input is provided through a speaker driven by Audio Precision instrument under near-field assumptions. The audio signal is calibrated using a reference microphone from Bruel&Kjaer (B&K), which is attached close to the MEMS, as shown in figure 3-32a. The Knowles-SiSonic analog MEMS microphone has a sensitivity of  $-42\text{dBV/Pa}$ . Figure 3-33 compares the PSD of the digital output for an input signal of  $1\text{Pa}@1\text{kHz}$  for acoustic and electric results.

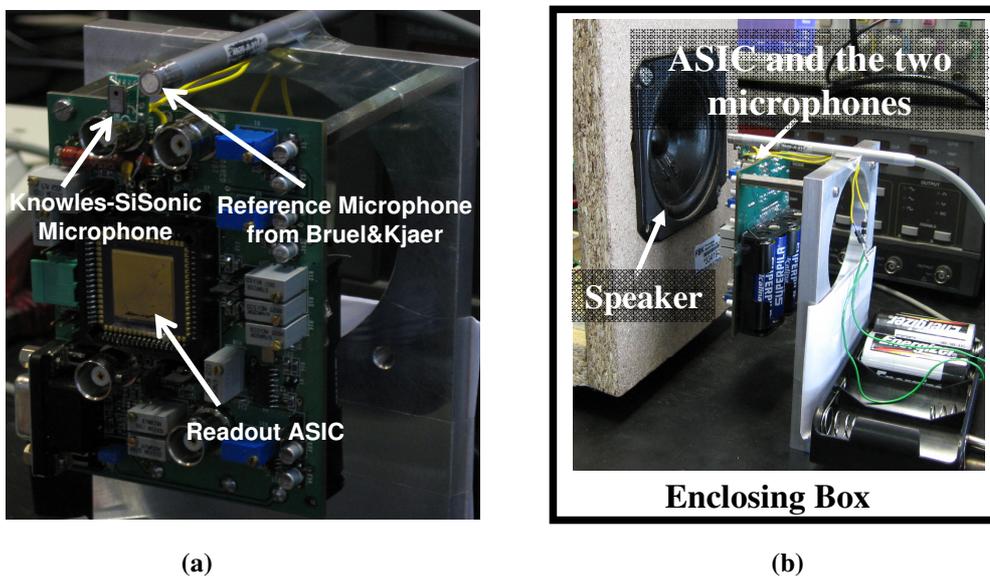


Figure 3-32 : (a) Reference and Knowles Microphones, (b) Acoustic Testing Setup

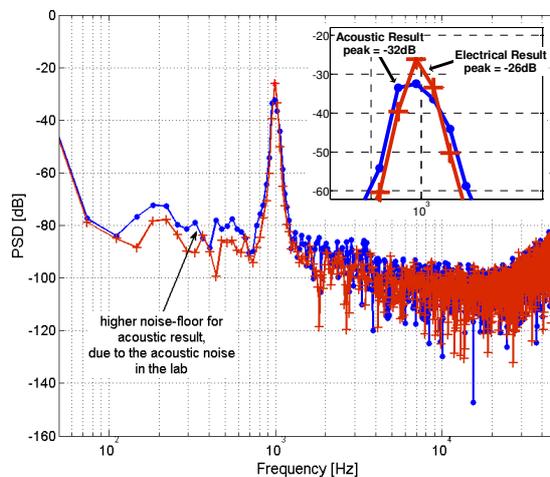
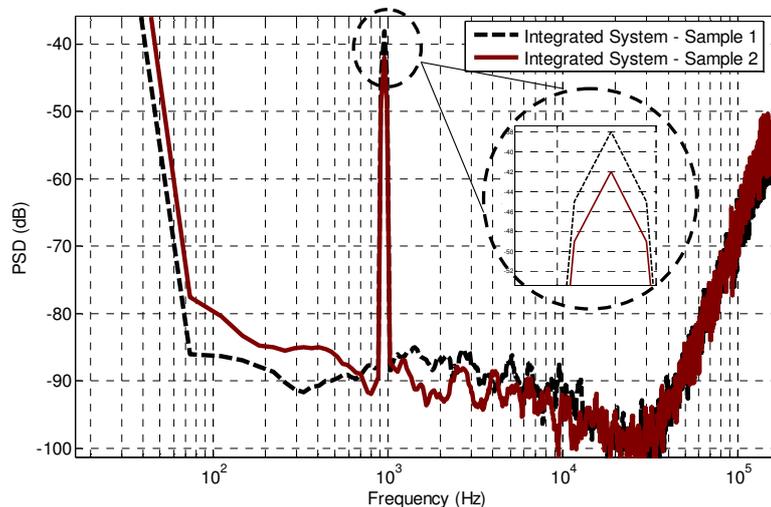


Figure 3-33 : Measured output of the Interface for  $1\text{Pa}$ ,  $1\text{kHz}$  Signal for both Acoustic (with Knowles Microphone) and Electric Measurements

First observation is that the signal amplitude for the acoustic results is 6dB lower in figure 3-33. The interface expects a sensitivity of -34dBFS/Pa due to the two-terminal bootstrapping. Whereas, the under-test SiSonic microphone has a sensitivity of -42dBFS/Pa, hence the loss of ~6dB. Nevertheless, the close resemblance between electrical and acoustic results validates the compatibility of the interface with standard microphone specifications. Second observation is the increased low-frequency noise floor, which can be attributed to higher acoustic noise around the test-setup because the sensor is not fully shielded.

Figure 3-34 shows the PSD of the digital output of the integrated system with the IRST MCM integrated in a single package with the readout. The MCM is bootstrapped inside the package following the above-mentioned two-terminal bootstrapping topology. The acoustic input is 1Pa, calibrated using the B&K reference microphone. It can be seen in figure 3-34 that two different samples display almost the same noise floor and high frequency quantization noise spectra; however, the signal-peaks have slightly different amplitudes. The peak amplitude for 1Pa for sample1 is -38dB while it is -42dB for sample2.

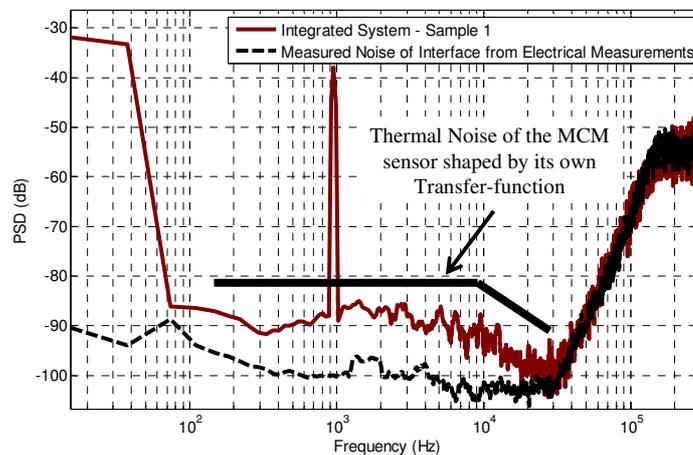


**Figure 3-34 : Acoustic Testing Results for 1Pa,1kHz Signal for Integrated IRST Microphone with Readout Interface in a Single-Package**

Figure 3-35 compares the acoustic results of the integrated system with the electrical results of the ASIC. The equivalent input for electrical measurements is also 1Pa. It can be seen that the sensitivity of the integrated acoustic system is ~14dB less than expected value (expected sensitivity = -26dBFS/Pa). This can be attributed to three factors:

- The sensitivity of the MEMS sensor could be lower than expected (expected sensitivity = 4.5mVpp/Pa or -53dBV/Pa).
- The two-terminal bootstrapping might not be boosting the signal as much as expected (expected boosting ~20dB).
- The parasitic capacitance at the sensing node, which includes input parasitic of the PAMP and the bonding parasitic capacitance, could be higher than expected and it could be attenuating the signal coming from the MEMS sensor.

The other observation from figure 3-35 is that the noise-floor in acoustic measurements is higher within the audio band than the noise floor in electrical measurements. The noise floor in acoustic measurements also exhibits a low-pass shape with a corner around 10kHz. This behavior can be ascribed to the thermal noise of the MCM, which is shaped by its own low-pass transfer function with the corner at 10kHz. This low-pass shape of the noise spectra within the audio-band in the acoustic measurements also implies that the mechanical resonance is not inside the audio-band as expected [20]. This points to structural anomalies in the MCM such as higher spring-constant and higher air-damping resistance arising due to the fabrication process [20], which could be the main reason of a considerably reduced sensitivity. The measured SNDR for acoustic measurements of the integrated system is 33dBA/Pa and the reduction in SNDR can be ascribed mainly to the reduced sensitivity and higher thermal noise floor shown by the MCM sensor.



**Figure 3-35 : Comparison of Acoustic Results for Integrated Acoustic System with Electrical Results for a signal of 1Pa,1kHz**

Figure 3-36 shows the frequency response of the integrated system throughout the audio band. This characterization is performed under the near-field assumptions and the sound-source (speaker) is placed 10-cm away from the microphones. MCM, the reference microphone and the speaker are placed inside a wooden box, which is internally matted with cotton to minimize reflections of sound-waves. In other words, this characterization is not performed in an anechoic chamber; therefore, the MCM under-test is prone to considerable artifacts due to constructive and destructive interference of acoustic reflections. To avoid artifacts due to sound reflections, several measurements are performed by changing the location of MCM in front of the speaker, which are subsequently averaged to achieve the final frequency response. It can be observed from figure 3-36 that the sensitivity of the MCM remains relatively flat around -40dB/Pa from 500Hz to 9kHz. The frequency response shows a resonance peak above 9kHz, which is most likely due to the Helmholtz resonance of the package, as we have already inferred from figure 3-35 that MCM mechanical resonance is outside the audio-band. With the given package dimensions, the theoretical Helmholtz resonance is expected to be around 16kHz, which is close to the measured behavior. Al-

though the exact value of the resonance peak in these measurement results is not fully-reliable due to the current acoustic testing setup; nevertheless, the measured results demonstrate that the frequency response of MCM is considerably affected by Helmholtz resonance above 10kHz. The downward slope in figure 3-36 for low frequencies below 500Hz can be attributed to two factors: (1) The air equilibration through the gap between diaphragm and the substrate, termed as flow-by slot, which is used as a vent for the compressed air to normalize the increased internal pressure, details can be found elsewhere [20]. (2) Or, the pole due to the diode-based resistance between chargepump and the backplate of the MCM in the two-terminal bootstrapped PAMP topology is not below 20Hz. This implies that the parasitic resistor between backplate and moving-membrane of the MCM has much lower-value than expected and there exists a dc-path between the two-terminals, which does not allow the diodes to operate as zero-biased resistors.

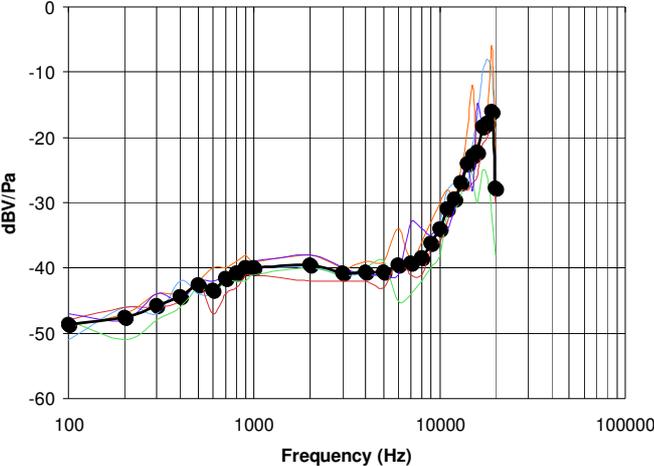


Figure 3-36 : Frequency Response of the Integrated Acoustic System

### 3.4.4 Power Consumption

Table 3-4 shows the breakage of power consumption inside the readout interface. It can be observed that a considerable amount of power is consumed by the bias generation. In the sleep mode, the total power consumption of the readout-interface comes down to 54μW.

Table 3-4 : Power Consumption per Components inside the Readout Interface

Power Consumption per Component inside the Readout Interface	
Total Device	828μW @ 1.8V of power-supply
Pre-Amplifier	198 μW
Sigma-Delta Modulator	180 μW - Internal Biases for OTA → 72 μW - Integrators → 108 μW
Bandgap Reference	198 μW
Bias Generation	252 μW

### 3.5. Conclusion

Design details and measurement results of an integrated readout interface for MEMS Capacitive Microphone in CMOS technology were presented in this chapter. This interface consisted of a preamplifier, a sigma-delta modulator, integrated biasing and digital control, demonstrating the feasibility of a low-power, low-noise integrated readout interface for MCM [94]. This interface demonstrated a source-follower PAMP topology that bootstraps the MCM to minimize the impact of MCM parasitic capacitors. The two-terminal bootstrapping scheme boosts the MCM signal by  $\sim 17$ dB. The noise of the PAMP was also boosted by the same factor; therefore, SNR remains unaffected. However, bootstrapping makes the readout immune to the variations in the parasitics of MCM and, due to the signal-boost, relaxes the size of sampling capacitors of the SDM. The PAMP achieved low flicker noise by using large-area input devices and the single-ended input from the MCM was converted into a pseudo-differential output by using a dummy branch which mimics the capacitive structure of the MCM. However, this approach to convert the PAMP output into a pseudo-differential output is relatively area and power hungry. Other approaches presented in the subsequent chapters employ more area and power efficient schemes for single-ended to differential conversion. The demonstrated third-order single-loop single-bit SDM suffered from flicker noise of OTA in the first integrator since the SDM does not employ CDS or CHS approaches to minimize offset and flicker noise. This interface employed on-chip integrated biasing and the possibility to tweak different parameters (such as bias currents of OTA) was limited, which restricted the window to observe the effects of such parameters on the performance. The interfaces presented in subsequent chapters keep the biasing controllable externally to observe the effect of different parameters on the performance. The acoustic results with the Knowles microphone demonstrated compatibility of the interface with standard microphone specifications. The acoustic results of the integrated single-package system demonstrated a sensitivity for 1Pa 1kHz signal which was  $\sim 14$ dB less than the expected value and the measured SNDR was 33dBA/Pa. This reduction in SNDR can be attributed mainly to the reduced sensitivity and higher thermal noise floor shown by the MCM sensor. The integrated single-package system also exhibited a peculiar frequency response on the higher-frequency side of the audio-band due to the package, giving rise to Helmholtz-resonance, which is explained in detail elsewhere [20]. This interface was designed in  $0.35\mu\text{m}$  2P/4M CMOS technology and the total area of the readout ASIC was  $750\mu\text{m} \times 1400\mu\text{m}$ . It interface achieved a measured SNDR of 55dBA/Pa at the output of preamplifier and 80dBA of dynamic range at the digital output. The electrical and acoustic results of this interface demonstrated a reasonable compatibility with standard specifications for a MCM based acoustic system.

# Chapter 4

## Readout Interface - II

### 4.1. Introduction

This chapter presents the design details and measurement results of a readout interface for MCM with force-feedback (FFB) functionality. This interface consists of a PAMP, a SDM and force-feedback logic. The results achieved in the previous interface demonstrate that the response of the complete acoustic system is heavily dependent on the electro-acoustic-mechanical properties of the MCM sensor. FFB can be utilized to reduce the impact of mechanical imperfections and the inherent non-linear nature of the MCM by enclosing the sensor in an electro-mechanical loop, as shown in figure 4-1. In this interface, the digital PDM output of the SDM is used to modulate the bias voltage of MCM to apply the counterbalancing electrostatic force feedback. The PAMP achieves parasitic-insensitive readout through a high-gain OTA in a capacitive feedback configuration. This method of parasitic compensation does not recycle noise like the bootstrapping scheme; therefore, it improves the SNR and a gain-factor can also be achieved by adjusting the feedback capacitor  $C_{FB}$  in the PAMP. The PAMP employs a dummy capacitive branch to convert the single-ended input of the MCM into a differential output, which is area and power-efficient as compared to the previous scheme. This interface employs a dynamic matching logic to match the dummy capacitive-structure closely with the MCM, which is also required for the application of FFB to the single-ended MCM. SDM is a third-order single-loop single-bit modulator similar to the previous interface. The major components of this interface are shown in figure 4-1.

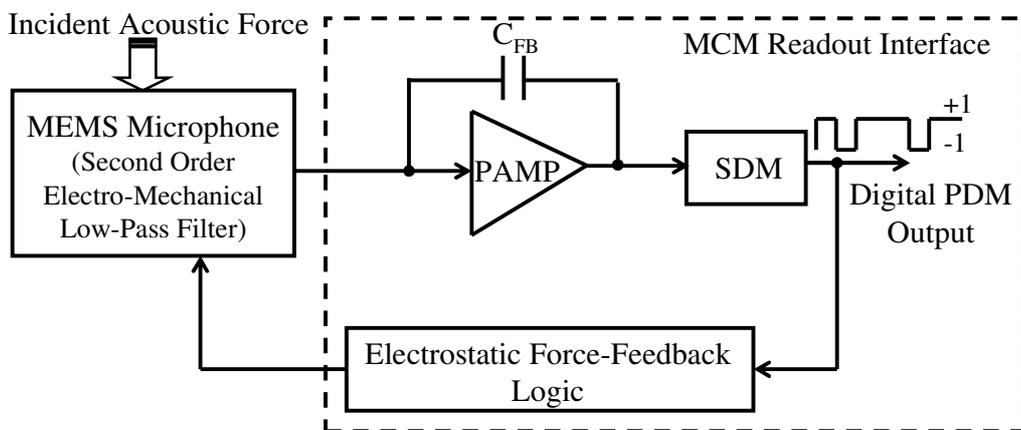


Figure 4-1 : Major Blocks of the Readout-Interface

## 4.2. Behavioral Description and Simulations of the Readout Interface

### 4.2.1 The Force-Balanced Microphone in Simulink

The behavioural simulations for the force-balanced MCM are performed in Simulink and the simulation setup is shown in figure 4-2. The preamplifier is replaced by a gain  $G_{PA}$ , which translates the capacitive variations into a corresponding voltage signal, which is fed to the third-order single-loop SDM. The output of SDM is used to perform bias voltage modulation of the MEMS microphone to induce the counter-balancing electrostatic force, where  $K_{FB}$  represents the gain applied to the output of the SDM to control the magnitude of the feedback electrostatic force.

The simplified representation of the MCM model for simulations in Simulink is shown in figure 4-3. It exploits the electro-mechanical analogy, i.e. the mass of the moving-membrane is represented by an equivalent inductor  $L_d$ , the damping coefficient by a variable resistor  $R_d$ , the compliance of the suspension spring by a capacitor  $C_{SP}$  and forces inside the system by corresponding voltage signals [78]. The current flowing through the RLC network represents the velocity of the moving membrane and the displacement of the membrane is computed by integrating the current, which in turn is used to compute the capacitive variations. The parameters for the targeted MCM model are listed in table 4-1 [20] and are extracted from C-V measurements and ANSYS simulations. Brownian noise of the sensor is also included in the model along with a  $1/f$  noise component [20]. Figure 4-4 shows the achieved frequency response of the MCM through the model. The presumption about the accuracy of this particular modelling scheme for MCM is based on the results achieved in [20], which presents a comparison between simulated and measured results for a MEMS microphone from Omron.

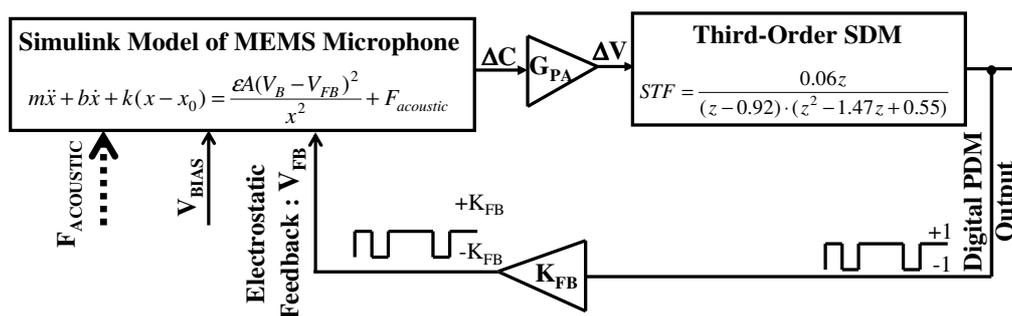
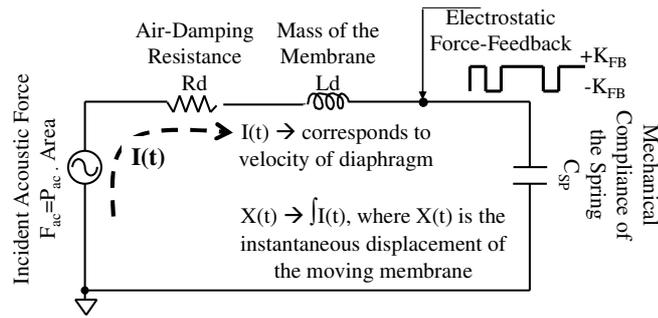
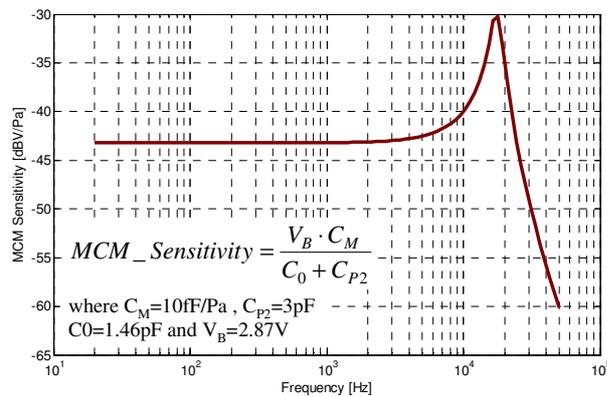


Figure 4-2 : The Simulink Simulation Setup for the Force-Balanced MCM



**Figure 4-3 : Simplified Representation of the MCM Model based on Electro-Mechanical Analogy used in Simulink Simulations**



**Figure 4-4 : Simulated Frequency Response of the MCM Model [20]**

**Table 4-1 : MCM Parameters used for the Simulink Model**

Parameter	Estimated Value from ANSYS or CV Measurements	Values Predicted by the Simulink Model
Effective Area of the Moving Membrane	0.25mm <sup>2</sup>	X
Spring Constant	27 N/m	X
Unbiased Electrode Gap	1.6 μm	X
Pull-in Voltage	4 V	X
Sensitivity @ 1KHz	10 fF/Pa	11fF/Pa
C <sub>p1</sub> , C <sub>p2</sub> , C <sub>0</sub>	21pF, 3pF, 1.7pF	21pF, 3pF, 1.46pF
Sensitivity @ 1kHz	-44dbV/Pa	-44dBV

Figure 4-5 plots the effect of force-feedback on the SNDR of the overall system for different values of  $K_{FB}$ , highlighting that an optimal value of  $K_{FB}$  exists which maximizes the SNDR. It must be noted that the SNDR of the open-loop system was limited by the nonlinearities of the MCM for higher acoustic inputs, which can be seen in figure 4-5 with  $K_{FB}=0$ . Figure 4-6 zooms into PSD of the output to highlight the behaviour of signal harmonics for three different values of  $K_{FB}$  (0.5,1 and 2). The following text discusses these results in detail.

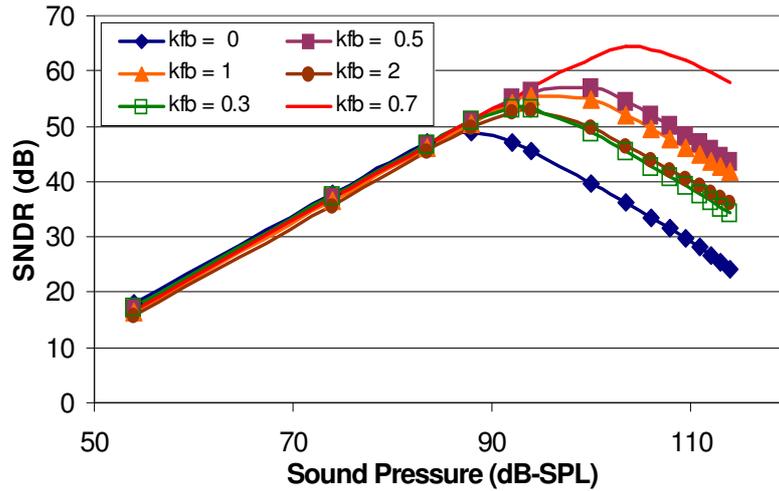


Figure 4-5 : Effect of force-balancing on the SNDR of the closed loop system, for different values of  $K_{FB}$

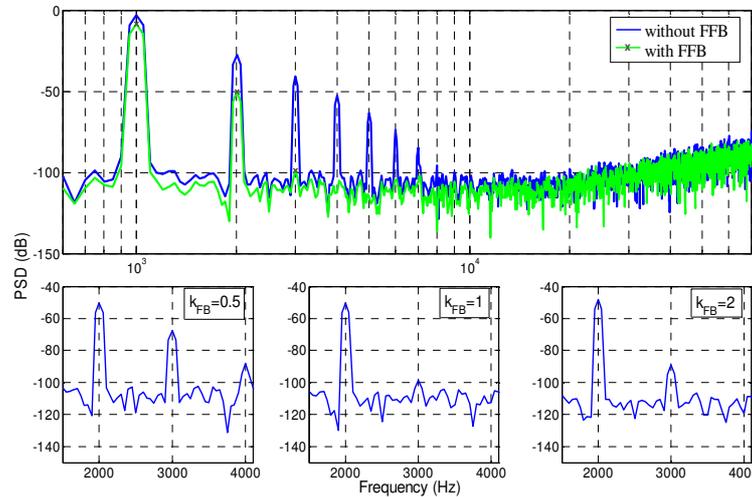


Figure 4-6 : Evaluation of the Signal Harmonics for input signal of 10Pa for different values of  $K_{FB}$

The bias voltage modulation causes an instantaneous change in the electrostatic force inside the MEMS as expressed in eq. 4-1. Because of the quadratic relation, the applied electrostatic force feedback has two components: one is always attractive ( $V_{fb}^2$ ), while the other ( $2V_{fb}V_{bias}$ ) either increases or decreases the attractive force depending on the polarity of the FFB pulse.

$$F_{el(inst)} = \frac{\epsilon A}{2(x_0 - x)^2} (V_{bias} - V_{fb})^2 = \frac{\epsilon A}{2(x_0 - x)^2} (V_{bias}^2 + V_{fb}^2 - 2V_{bias} V_{fb}) \quad (\text{Eq. 4-1})$$

The input acoustic pressure is 10Pa in figure 4-6, which is the acoustic overload and represents a high level of pressure where the response of MCMs are typically distorted. When a force feedback (FFB) of  $\pm 1V$  ( $K_{fb}=1$ ) is applied, the fundamental frequency amplitude is reduced by 6dB, while 2<sup>nd</sup> and the 3<sup>rd</sup> harmonics are reduced by  $\sim 23\text{dB}$  and  $\sim 57\text{dB}$  respectively. The reduction in harmonics can be attributed to the fact that the movement of the electrode is reduced due to the counter-balancing electrostatic force

generated by FFB; therefore the overload in both the sensor and the SDM is avoided. Eq. 4-2 along with figure 4-6 reveals the effect of  $K_{FB}$  on the feedback. In Eq. 4-2, feedback is considered as a sinusoidal signal, along with its harmonics, representing the MEMS response to input acoustic signal. For the sake of simplicity, only the first two harmonics are included in the expression and higher-order terms are neglected.

$$\begin{aligned} & \left[ V_{bias} - V_{fb}\alpha_1 \sin(\omega t) - V_{fb}\alpha_2 \sin(2\omega t) - V_{fb}\alpha_3 \sin(3\omega t) - \dots \right]^2 = \\ & V_{bias}^2 + V_{fb}^2\alpha_1^2 \frac{1 - \cos 2\omega t}{2} - 2V_{bias}V_{fb}\alpha_1 \sin\omega t - 2V_{bias}V_{fb}\alpha_2 \sin 2\omega t - \\ & 2V_{bias}V_{fb}\alpha_3 \sin 3\omega t + \dots O(V_{fb}^2) \end{aligned} \quad (\text{Eq. 4-2})$$

$\alpha_1$ ,  $\alpha_2$ , and  $\alpha_3$  are the amplitudes of the respective harmonics as compared to  $V_{fb}$ .

Unlike the odd harmonics in eq. 4-2, the even harmonics have an additive term ( $V_{fb}^2\alpha_1^2[1 - \cos 2\omega t]/2$ ). This term always contributes to an attractive force between the electrodes. The other terms, for both odd and even harmonics, increase or decrease depending on the polarity of FFB pulse, and are a multiple of  $V_{bias}$  and  $V_{fb}$ . For that reason, an optimal value of  $K_{fb}$  exists, after which if  $K_{fb}$  is further increased, it causes only a reduction in the odd harmonics. This is shown in figure 4-6, where the second harmonic for  $K_{fb}=0.5$  and  $K_{fb}=1$  have almost the same amplitude while the third harmonic has reduced by  $\sim 30\text{dB}$ . The optimal value of  $K_{fb}$  from the simulation is  $\sim 0.7$ .

However, if the value of  $K_{fb}$  is further increased to 2, as shown in figure 4-6, the third-harmonic is higher as compared to the case when  $K_{fb}=1$ , although the movement of the electrode has further reduced. This is due to the change in operating point of the MEMS because of the square-term ( $V_{fb}^2$ ) in eq. 4-1. This term, depending on the magnitude of the applied FFB pulse, causes further spring loosening, bringing the two electrodes closer than the original operating point and increasing the non-linearity associated with the electrostatic force [79,80]. However, these results signify that although the MM of the MCM is not made nearly-stationary due to the feedback, nevertheless, the reduction in the swing causes considerable reduction in distortion with small amplitude FFB pulses.

Figure 4-5 plots the SNDR of the system versus input acoustic pressure for different values of  $K_{FB}$ , where the over-sampling ratio (OSR) for the modulator is 63. Force-balancing can provide a maximum enhancement of 25dB in SNDR when  $K_{fb}=0.7$ , especially close to the acoustic overload. It also demonstrates that using low and CMOS-compatible voltage FFB, a considerable gain in the performance for MCM can be achieved.

The closed-loop system can be considered as a hybrid SDM, in which the MEMS microphone also serves as an extra second-order loop filter, therefore, adding two more zeros in the NTF of the SDM. Figure 4-7 shows the effect of the feedback on the noise in the Simulink model. The curve with only the sensor in the FFB loop shows that the noise shaping zeros inserted by the sensor are close to 10kHz, which corresponds to the resonance frequency of the MEMS. It also shows that the dc-gain of the sensor is quite low and thus the ditch in the NTF is not very strong, i.e. the extra zeros are far from the unit cir-

cle. When the third-order SDM is placed in front of the sensor, we can see that with the FFB loop, the quantization noise shaping is slightly different from third-order shaping from 10kHz to 20kHz. This is due to the extra zeros from the MCM. However, this shaping is not very strong and it disappears for frequencies above 30kHz, where the effect of the extra zeros is masked by the poles in the NTF. Thus with the real sensor, the noise performance of the closed-loop is not expected to change much and effective noise-shaping would be third-order due to the SDM.

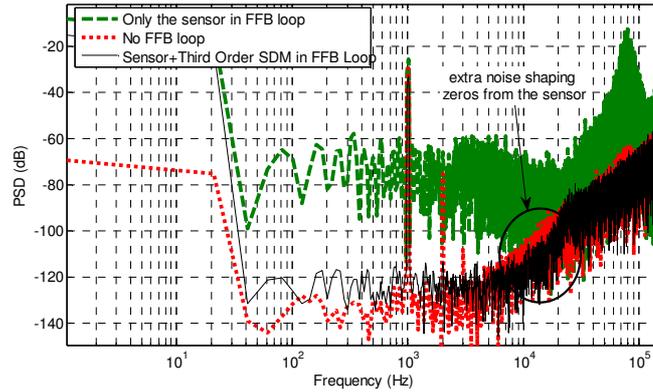


Figure 4-7 : Effect of force-feedback on the quantization noise of the SDM

### 4.2.2 The Sigma-Delta Modulator

SDM is a third-order single-bit quantizer feed-forward modulator similar to the SDM for the first interface. The schematic of the SDM is shown in figure 4-8 and eq. 4-3 and eq. 4-4 express the STF and NTF respectively. Figure 4-9 shows the noise floor and the achievable DR by the SDM with induced practical constraints in Simulink.

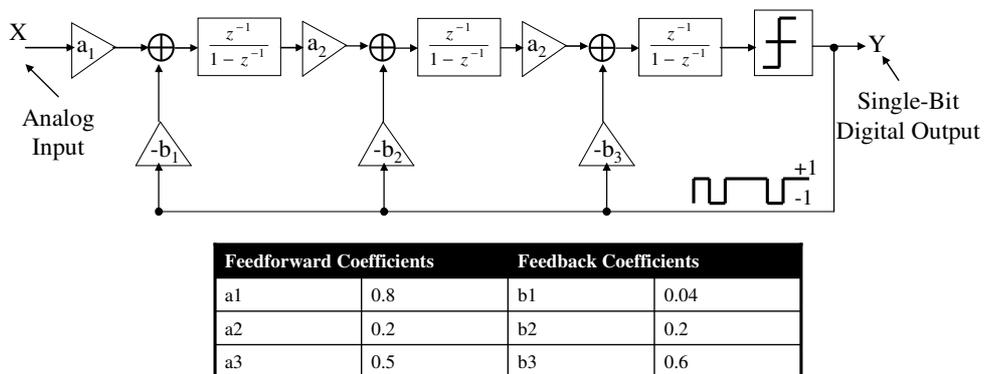
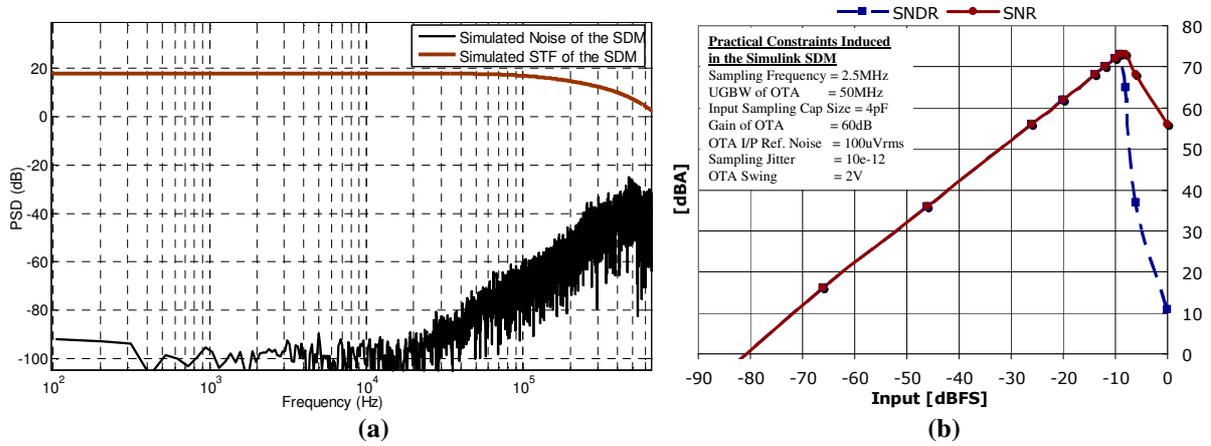


Figure 4-8 : Third-Order Single-Loop Single-Bit SDM

$$STF = \frac{0.06z}{(z - 0.92) \cdot (z^2 - 1.47 \cdot z + 0.55)} \tag{Eq. 4-3}$$

$$NTF = \frac{(z-1)^3}{(z-0.92) \cdot (z^2 - 1.47z + 0.55)} \quad (\text{Eq. 4-4})$$



**Figure 4-9 : (a) Noise Floor and STF of the Simulated SDM, (b) The Simulated SNR and SNDR of the SDM with the listed practical constraints**

### 4.2.3 Discussion on the Stability of Closed-Loop System

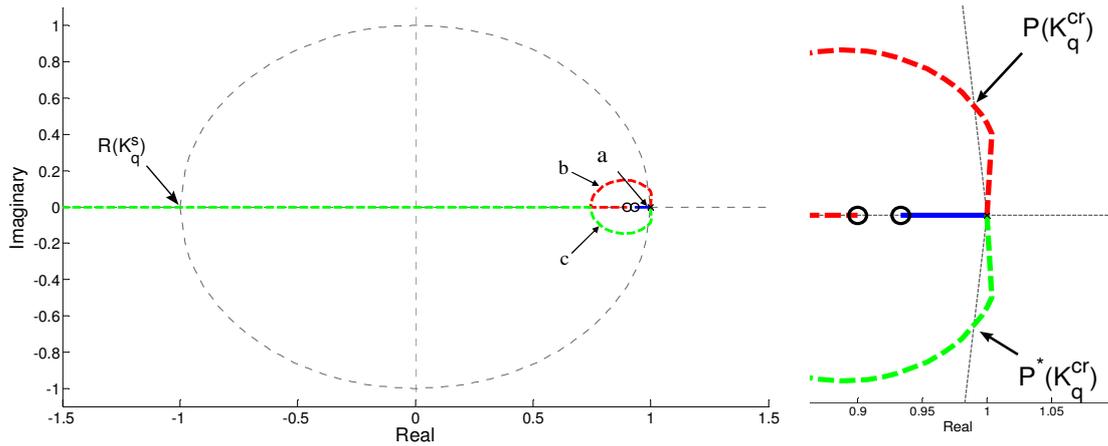
#### SDM Stability

The SDM is a non-linear system because of its quantizer, which has a time-varying non-linear gain. A common way to analyze the stability of an SDM is modelling the quantizer as a variable gain [96]. This gain ( $K_q$ ) can be defined as the ratio between the output signal ( $y_q$ ) of the quantizer and its input ( $x_q$ ), as expressed in eq. 4-5.

$$K_q = \frac{|y_q|}{|x_q|} \quad (\text{Eq. 4-5})$$

$K_q$  can swing between zero and infinity. With this approximation, linear methods can be applied to study SDM stability. The transfer function of the designed readout interface is given by eq. 4-6, where quantizer is replaced by a variable gain  $K_q$ .

$$\frac{Y(z)}{X(z)} = \frac{0.06 K_q}{z^3 - 3z^2 + 3z - 1 + K_q (0.6z^2 - 1.1z + 0.504)} \quad (\text{Eq. 4-6})$$



**Figure 4-10 : Root-Locus of the SDM for variable Quantizer Gain**

The root locus of eq. 4-6 is shown in figure 4-10 by varying the quantizer gain  $K_q$ . The root locus has three branches. Branch  $a$  lies entirely inside the unit circle, so it does not give rise to any limit cycle. Branches  $b$  and  $c$  cross the unit circle at  $P$  and  $P^*$  respectively, where the gain of quantizer is  $K_q^{cr}$ . If  $K_q$  is less than  $K_q^{cr}$ , on the symmetric points  $P$  and  $P^*$ , it means that  $x_q$  is high and the poles are outside the unit circle. In this situation,  $x_q$  tends to further increase, reducing the gain and keeping the poles outside the unit circle. This causes the integrators to saturate, establishing a low frequency oscillation. This process gives rise to a saturation limit cycle. In our case the critical gain  $K_q^{cr}$  is 0.083. The maximum sound pressure at the input of the microphone is considered to be 10Pa (114dB-SPL). From Simulink simulations of the SDM, the minimum value of  $K_q$  is 0.19 for an input signal of 10Pa, which is higher than the critical gain. Thus, the designed SDM does not have any limit cycle in the audio band for acoustic inputs as large as 10Pa (114dB-SPL).

### Stability of the Complete Closed-Loop System, i.e. Microphone + SDM

To analyze the complete closed-loop system, i.e. MCM Simulink model with the SDM in the FFB configuration, it is assumed that SDM alone does not have a saturation limit cycle and the quantizer gain  $K_q$  is set to 1. Consequently, the root locus of the closed-loop system is computed as a function of the feedback gain  $K_{FB}$ . The transfer function of the microphone has been simplified to a second order system and then discretized using the bilinear transformation. Due to this transformation, two zeros at  $F_s/2$  appear. On the root locus there are four points, symmetric two by two, where it goes out of the unit circle. However, they occur when the feedback gain  $K_{FB}$  is 31.9 and  $1.85 \times 10^7$  [20]. As highlighted in sub-section 4.2.1, there is an optimum value for  $K_{FB}$  (approx. 0.7) in order to improve the SNDR of the system, which is well below these critical values. This ensures the stability of the closed-loop system for the considered operating conditions.

### 4.3. CMOS Design Details

This interface is implemented in 0.35 $\mu\text{m}$  2P/4M CMOS technology and the targeted supply voltage is 3.3V. The circuit-level simulations are performed using Spectre in Cadence design environment. However, due to the unavailability of a detailed MCM model in VerilogA, such as the one in Simulink, the closed-loop system levels simulations are not performed at circuit level. The behavioral simulation results presented in previous section are used as the basis of expected performance of the complete closed-loop MCM system.

#### 4.3.1 The Preamplifier

The preamplifier is a capacitive gain-stage based on charge-amplifier topology, as shown in figure 4-11. For this readout interface, i.e. with the application of force-balancing to the MCM, it is advantageous to have the flexibility of controlled PAMP gain, to have another controlling parameter for the overall loop-gain. However, the gain is not well-controlled since the matching between MEMS capacitors and the poly-capacitors inside the interface is not well-controlled. The parasitic capacitors at the sensing node MM are compensated by the high gain OTA in capacitive feedback configuration by reducing the swing across the parasitic capacitors at the sensing node. The PAMP utilizes a dummy capacitive branch to convert the single-ended output of the MCM into a fully-differential output, as shown in figure 4-11. In this topology the mismatch between the MEMS capacitive structure and the dummy branch does not cause an offset at the output of the PAMP. However, this mismatch affects the expected gain.

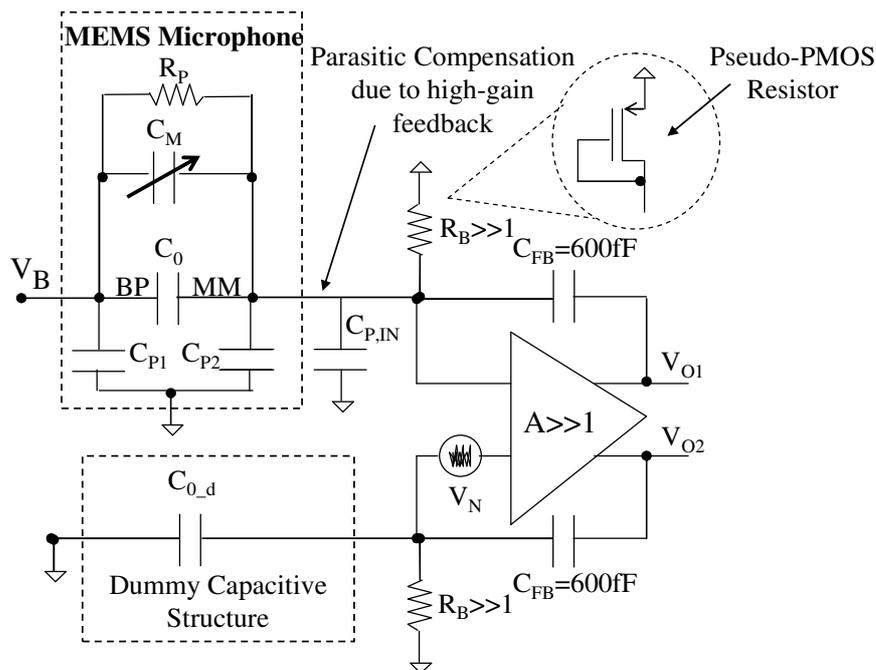


Figure 4-11 : PAMP based on charge-amplifier topology, utilizing a dummy capacitive-branch to convert the single-ended input to a fully-differential output

The charge injected by the MEMS sensor is integrated through the integrating capacitance CFB and converted into a voltage signal with a gain factor as expressed in eq. 4-7, which simplifies to a ratio between the MCM capacitive variation and the integrating capacitance if A is large, signifying a parasitic insensitive readout.

$$V_0 = V_{01} - V_{02} = \frac{-s \cdot A \cdot R_B \cdot C_M}{1 + s \cdot R_B \cdot (A \cdot C_{FB} + C_M + C_0 + C_{P2} + C_{FB})} \sim \frac{-C_M}{C_{FB}} \quad (\text{Eq. 4-7})$$

The dc-bias resistance  $R_B$  gives rise to a high-pass corner at lower frequency side of the acoustic band as expressed in eq. 4-8, which simplifies to a product of the OTA gain, bias resistance and the integrating capacitance if A is large.

$$HPF\_corner = \omega_{HPF} = \frac{1}{R_B \cdot (A \cdot C_{FB} + C_M + C_0 + C_{P2} + C_{FB})} \sim \frac{1}{A \cdot R_B \cdot C_{FB}} \quad (\text{Eq. 4-8})$$

Figure 4-12a shows the frequency response of PAMP for different values of bias resistor  $R_B$ . It can be seen that the high-pass corner frequency shifts higher for low values of bias resistor. It also shows that bias resistor of 100MΩ or above provides a flat band response throughout the audio band. However, as discussed later, that it is advantageous to have a larger bias resistor from the noise perspective. Figure 4-12b shows the readout-sensitivity for 1Pa signal at the output of the PAMP, with different values of parasitic capacitances. It can be seen that the sensitivity of the readout is not affected by the parasitics.

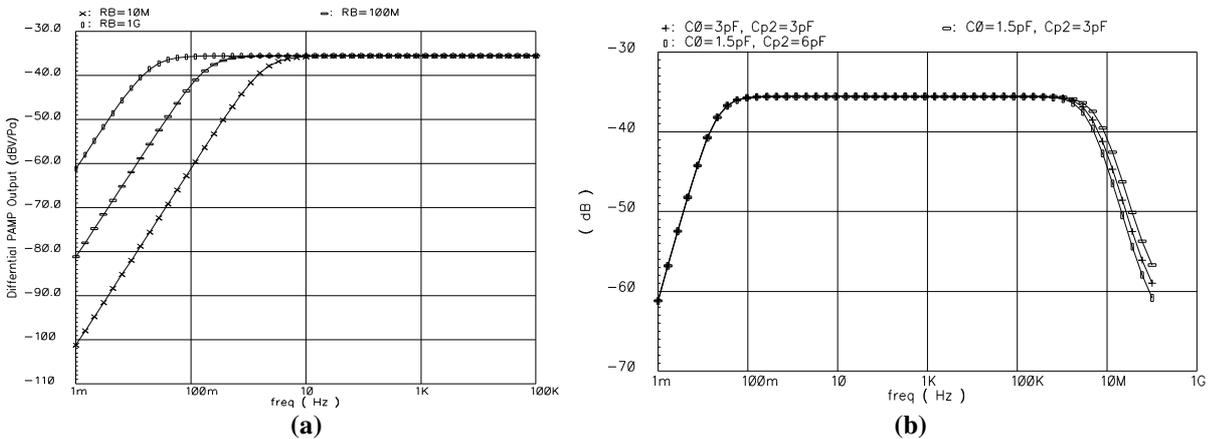


Figure 4-12 : (a) Frequency Response of the PAMP, (b) Sensitivity of the PAMP for different value of parasitic capacitors

The dc-biasing resistor  $R_B$  is implemented using pseudo PMOS resistors [33]. These resistors demonstrate incremental resistances of above GΩ if the voltage swing around them is below  $\pm 200\text{mV}$ . It is like having a diode-connected PMOS if the voltage swing at the sensing node is below ground, biased in sub-threshold, and having a zero biased diode-connected parasitic PNP if the swing goes above ground. Since the swing at the sensing node is small due to the capacitive feedback,  $R_B$  remains stable at very

high resistance values.  $R_B$  is not placed in the feedback since their resistance is dependent on the voltage swing around them; therefore, there is no dc feedback in the PAMP. This implies that the mismatch and low-frequency noise of the PAMP would appear at the output multiplied by the dc-gain of the OTA. Since both the virtual ground terminals are available externally as test pins for this chip, therefore, any probable offset can be nullified by creating a counter-balancing offset externally. However, to develop a fully-integrated system, either a dc feedback should be provided to minimize the offset at the output or other techniques such as chopper-stabilization and correlated double sampling be used to remove the offset.

### OTA of the PAMP

The designed current-mirror OTA topology is shown in figure 4-13. The targeted supply voltage is 3.3V; therefore, a single-stage OTA scheme can be employed without violating the output swing requirements. The PAMP OTA has to drive its own integrating capacitors ( $\sim 600\text{fF}$ ) and the sampling capacitors of the following SDM ( $\sim 4\text{pF}$ ), which does not require very strong drive strength. PMOS input pairs are used to achieve a lower flicker noise. This also brings about another advantage. Since the pseudo-PMOS resistors are used to dc-bias the input-pair, it is better for the pseudo-PMOS resistors to be biased close to ground, and a PMOS input pair allows that. The sizing of the input pair is done to minimize its flicker noise and at the same time keep them in saturation instead of weak inversion. The mismatch effect due to  $g_m$  maximization can be larger in weak inversion and input pair is kept in strong inversion just to avoid that. The sizing of the cascades is done keeping in mind that larger cascode devices would increase the gain; however they would bring the non-dominant pole closer, hence decreasing the phase margin. The PMOS current sources are sized in accordance with the common mode feedback to have the same UGBW for both differential and common-mode control. The gain and phase of the OTA are shown in figure 4-14a.

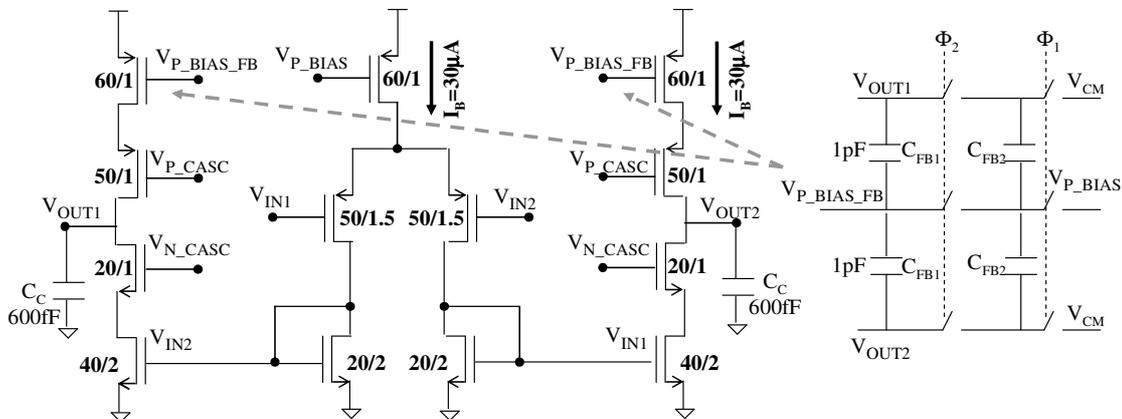
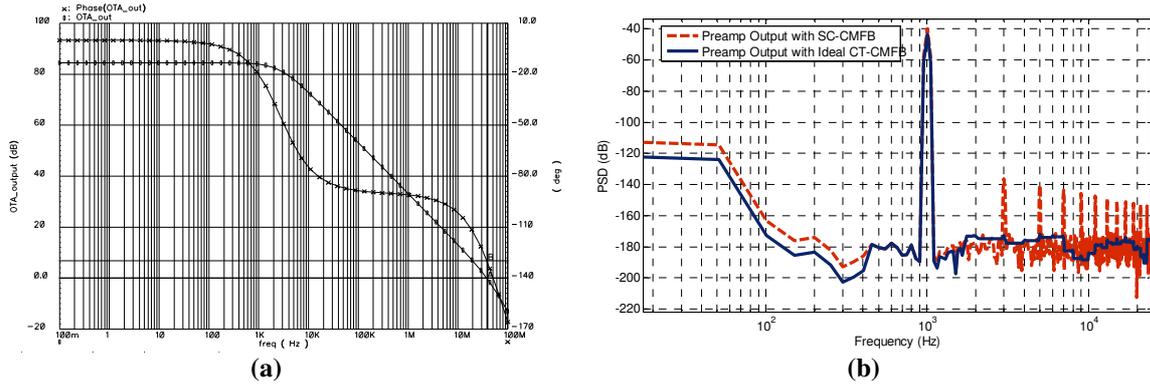


Figure 4-13 : Current-Mirror OTA for the PAMP along with SC-SC-CMFB



**Figure 4-14 : (a) Gain and Phase of the PAMP OTA, (b) The Effect of the SC-CMFB on the output of OTA**

Since the OTA is fully-differential, a CMFB circuit is needed to regulate the output common mode voltage. Although the preamplifier is a continuous-time charge amplifier and a CT CMFB would suit the topology naturally; however, CT CMFB circuits complicate the stability and swing specifications [93]. Hence, a SC CMFB is implemented for the OTA. Figure 4-14b shows the PSD of the output of the PAMP, for two different CMFB circuit, one ideal CT CMFB and the other SC-CMFB. It can be seen that signal-dependent charge-injection from the SC-CMFB causes signal harmonics higher than the CT CMFB; however, the distortion is not very high to disturb the targeted specifications. The other issue from the SC-CMFB circuit is the KTC thermal noise that it is going to inject directly at the output of the OTA. Proper sizing of the capacitors in SC-CMFB can keep the KTC noise below the required specifications.

### Noise Analysis of the PAMP

The major noise sources in the PAMP are as follows:

- Noise of the OTA, including flicker and thermal noise and KTC noise from CMFB
- Noise from the high-value bias resistors

The flicker and thermal noise from the OTA appears at the output with the following transfer function ( $NTF_{OTA}$ ), which is a low-pass shaped function, expressed in eq. 4-9. Since there is no dc-feedback in the PAMP, the low-pass shaped appears at the output multiplied with dc-gain of the OTA as shown in eq. 4-9.

$$NTF_{OTA} = \frac{A \cdot (1 + s \cdot R_B \cdot (C_M + C_0 + C_{P2} + C_{FB}))}{1 + s \cdot R_B \cdot (A \cdot C_{FB} + C_M + C_0 + C_{P2} + C_{FB})} \quad (\text{Eq. 4-9})$$

The switching in the CMFB can contribute to the following noise components at the output of preamplifier, which are expressed in eq. 4-10.

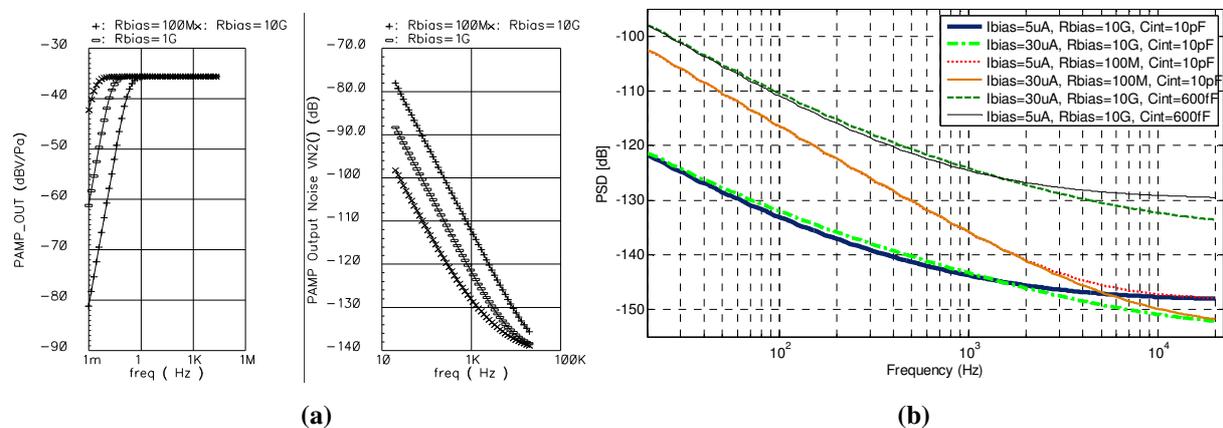
- Charge injection, dependent on the output signal swing of the PAMP.
- The clock feed-through, depending of the sizes of the switches.
- The KTC noise, depending on the effective load capacitance on the output node.

$$V_{N,CMFB} = \alpha \cdot \frac{C_{OVLP}}{C_{OVLP} + C_L} \cdot V_{swing} + \frac{Q_{INJ}}{C_L} + \sqrt{\frac{K \cdot T}{OSR \cdot C_L}} \quad (\text{Eq. 4-10})$$

$\alpha$  is the attenuation factor that caters for the portion of feed-through charge that has been sunk to the ground instead of coming to the output [43].  $C_{OVLP}$  is the capacitance between gate and source/drain of the MOS transistors due to overlapping of the gate-oxide with the junctions.  $C_L$  represents the effective load capacitance present at the output of the PAMP. This  $V_{N,CMFB}$  can appear either directly at the output or through the feedback loop, i.e. through the common-mode transfer function (CMTF). However, this noise appears as a common mode noise to the CMTF and is cancelled out unless there is some mismatch in the two output branches of the OTA. The other contribution directly at the output is not common-mode and thus affects the output.

The effective load capacitance for CMFB circuit includes the compensation capacitance, the integrating feedback capacitance, the input capacitance and finally the capacitance used in the CMFB network, i.e.  $C_L = C_C + C_{FB} + C_{CMFB} \sim 2\text{pF}$ . Therefore, a rough estimate of the KTC noise can be made, which is  $-105\text{dB}$ , for an OSR of 60, since the CMFB is operating at  $2.4\text{MHz}$  and the audio-band is  $\sim 20\text{kHz}$ .

The noise from the pseudo-PMOS resistor  $R_B$  also appears at the output with a low-pass shape. As the resistance increases, the thermal noise contribution of  $R_B$  increases; however, for very large resistance, most of the area of low-pass curve falls out of audio below  $20\text{Hz}$ . Figure 4-15a shows the effect of  $R_B$  on the output noise of the PAMP. Figure 4-15b plots a sample of table 4-2 which shows the output noise of the PAMP for different values of  $R_B$ , integrating capacitance and the bias current.



**Figure 4-15 : (a) STF and NTF of the PAMP for different values of bias resistor, (b) Noise at the output of PAMP for different values of feedback capacitors, bias resistor and bias current**

Table 4-2 shows the integrated noise (20Hz-20kHz) at the output of the PAMP for different values of feedback-capacitor of the PAMP, bias resistor  $R_B$  and bias current of OTA. It can be seen that altering bias current does not have much impact on the output since the noise is dominated either by the thermal noise of bias resistor or by the flicker noise of the OTA current sources. It also shows that, depending on the bias resistor value, the dominant noise source is either bias resistor noise or the flicker noise of the NMOS current sources.

**Table 4-2 : Preamplifier Noise for different values of Bias Resistor, Integrating Cap and  $I_{bias}$**

Preamp Noise for different values of Bias Resistor, Integrating Cap and $I_{bias}$				
Bias Resistor	Integrating Capacitance	$I_{bias}$	Integrated Noise	Dominant Component
100M $\Omega$	10p	30u	-103dBA	Bias resistors (70%)
	600f	30u	-80dBA	Bias resistors (96%)
	600f	5u	-80dBA	Bias resistors (96%)
	10p	5u	-102dBA	Bias resistors (66%)
1G $\Omega$	10p	5u	-108dBA	Bias resistors (25%) Thermal and flicker of NMOS current mirrors (40%)
	600f	5u	-89dBA	Bias resistors (72%)
	600f	30u	-90dBA	Bias resistors (80%)
	10p	30uA	-110dBA	Flicker noise of NMOS current mirrors (36%) Bias resistors (32%)
10G $\Omega$	10p	30u	-111dBA	Flicker of NMOS current mirror (70%)
	600f	30u	-95	Flicker of NMOS current sources (32%) Bias resistors (26%)
	600f	5u	-93	Bias resistors (20%) Thermal noise of NMOS current sources (20%)
	10p	5u	-110dBA	Thermal and flicker of NMOS current sources (20%)

### 4.3.2 The Sigma-Delta Modulator

The SDM design is similar to the one in previous interface in chapter 3. Figure 4-16 shows the SC schematic of the designed SDM. The capacitors for SDM are implemented using poly-poly capacitors for an area efficient layout.

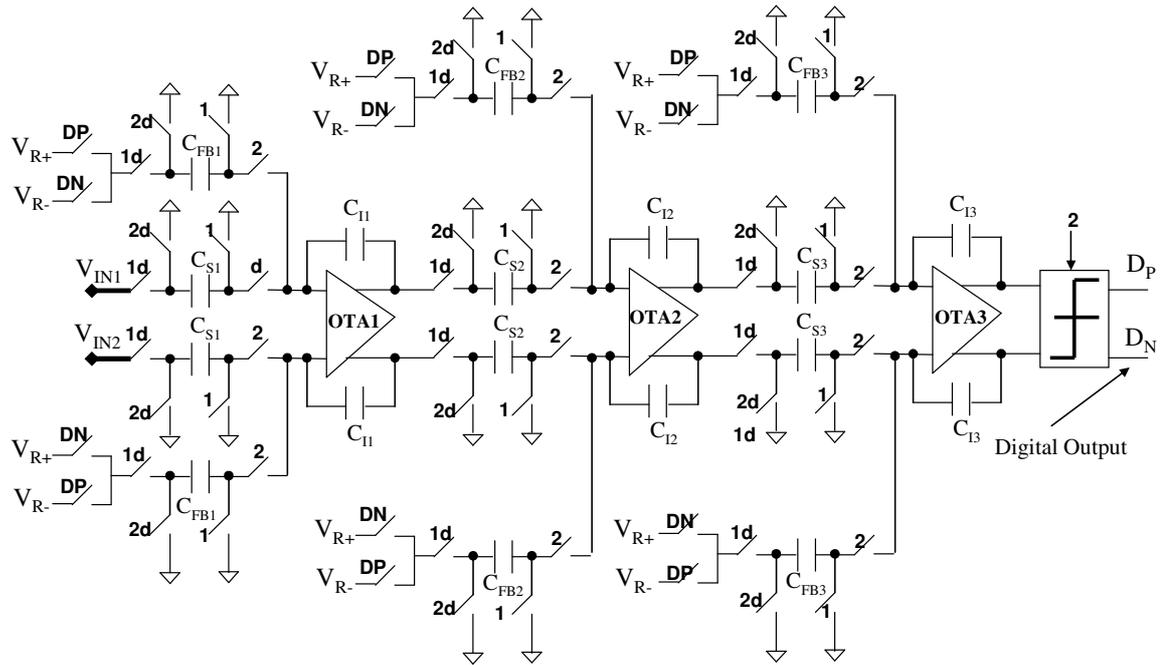


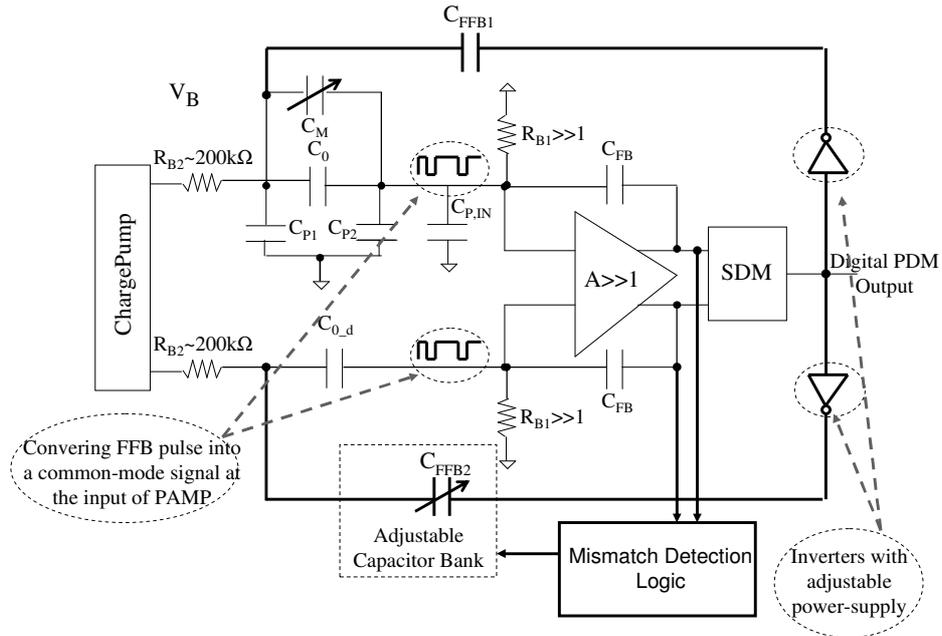
Figure 4-16 : Schematic of the Switched-Capacitor Third-Order Single-Loop Single-Bit SDM

### 4.3.3 The Force-Balancing Logic

As mentioned in section 4.2, the digital PDM output of SDM is applied to the back-plate of the MCM to modulate its bias voltage for electrostatic force-feedback. However, this raises following design issues at circuit-level:

- For the polarization of the sensor, a dc-bias is established at the backplate of the sensor through a charge-pump, which should not be disturbed by the FFB pulses.
- Since MCM is a single-ended sensor and there is a nominal bias capacitance ( $C_0$ ) between backplate and the moving membrane, therefore, the applied FFB pulse would traverse through the MCM and reach the input of the PAMP, causing an inefficient utilization of the PAMP's DR and might also overload the SDM.
- The backplate-to-substrate parasitic ( $C_{P1}$ ) effect should be taken into consideration to make sure the applied FFB pulse properly settles to the expected value.
- The force-feedback gain ( $K_{FB}$ ) required to completely counter-balance the incident acoustic force is limited by the fact that the applied pulse reaches the PAMP which has a limited common-mode range. This gain ( $K_{FB}$ ) can be partitioned into two portions. First, the gain of the readout interface, i.e. from the PAMP to the output of the SDM. Second, the amplitude of the feedback pulse.

Figure 4-17 shows the scheme used to apply the FFB to the MCM. Following text discusses the details how this approach solves the above mentioned issues.

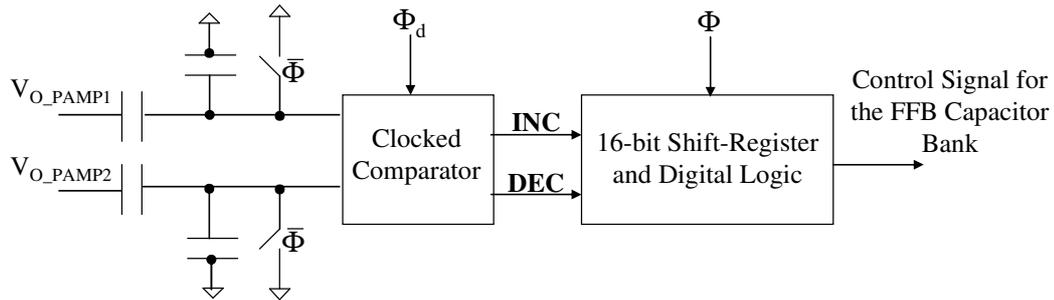


**Figure 4-17 : The Force-Feedback Logic, along with mismatch-minimization logic to match the dummy capacitors with MCM capacitance**

The output of sigma-delta modulator is applied to the backplate nodes of both sensor and the dummy branch using large feedback capacitors ( $C_{FFB1}$ ,  $C_{FFB2} \sim 20\text{pF}$ ). At the same time, charge-pump decoupling is provided by  $200\text{k}\Omega$  poly-resistances between the charge-pump and the backplate nodes of the MCM and the dummy branch. If the SDM output is less busy, i.e. less frequent zero-one transitions, the FFB pulse applied to the backplate would slowly discharge through this  $200\text{k}\Omega$  resistor. However, the FFB capacitors ( $C_{FFB1}$  and  $C_{FFB2}$ ) are large enough to accumulate enough charge to retain the FFB pulse above its 70% value for  $20\mu\text{s}$ , which represents a 50 cycle long pulse for a sampling frequency of  $2.5\text{MHz}$ .

The applied FFB pulses traverse through  $C_0$  and  $C_{0,d}$  and reach the input of the PAMP. To cancel this pulse as a common-mode signal at the input of the PAMP, the amplitude of the FFB pulse applied to the dummy branch can be controlled using a capacitor bank. This is done by mismatch minimization logic, which is shown in figure 4-18. The mismatch minimization logic consists of a high-pass filter and a 16-bit shift register. The output of the PAMP is fed to the comparator through a capacitive divider circuit. The input nodes of the comparator are reset to the analog-ground when the clock  $\Phi$  is low. When  $\Phi$  goes high, the comparator switches and asserts either increment (INC) or decrement (DEC) signal for the shift-register. The clock of the comparator is slightly delayed to allow the capacitive-divider circuit to settle to the required. The INC or DEC of the shift register depends on the polarity of the mismatch between the MEMS and dummy branch. An increment in the shift register causes an extra capacitor to be added in the  $C_{FFB2}$  capacitor bank. Simply put, this scheme turns the single-ended MCM into a pseudo-differential MCM.

The FFB pulses are applied through inverters which have externally adjustable power supply. This allows us to control the amplitude of the FFB pulse according to the sensor requirements to control the gain  $K_{FB}$ . Two separate inverters are used for regenerating the FFB pulse for MEMS and the dummy branch. This also allows us to minimize the mismatch between two branches beyond the matching resolution of the shift register based logic by manually adjusting the levels of FFB pulses applied to the two branches. These inverters are kept strong enough and force-feedback capacitors large enough that the settling of the applied FFB pulse is not affected by backplate-to-substrate parasitic capacitor ( $C_{P1}$ ) of the MCM.



**Figure 4-18 : The mismatch-minimization logic to match the dummy capacitors with MCM capacitance, using a comparator-based HPF and 16-bit Shift-Register**

## 4.4. Measurement Results

### 4.4.1 Measurement Setup

Figures 4-19a shows the microphotograph of the readout interface with dimension of  $1930\mu\text{m} \times 1630\mu\text{m}$  with the pad-ring. Figure 4-19b shows the ASIC mounted on bread-board. Figure 4-20 depicts the measurement setup. Power Supply, clock and the input signal are provided by external power supply and signal generators, respectively. The differential swing of the PAMP is converted into a single-ended swing using INA111BP instrumentation amplifier. The output of this amplifier is fed to the PC sound-card line-in. The PC sound card has input impedance  $\sim 1\text{k}\Omega$ . So, INA111 serves two purposes here. First, it converts the differential output of the PAMP into a single ended output. Second, it acts as a buffer driving the low-impedance input of the sound-card. Inside the PC, the analog signal is analyzed using software SpectraLab, using 16-bit sampling. The digital output of the SDM is sampled using a logic-analyzer and is post-processed in Matlab.

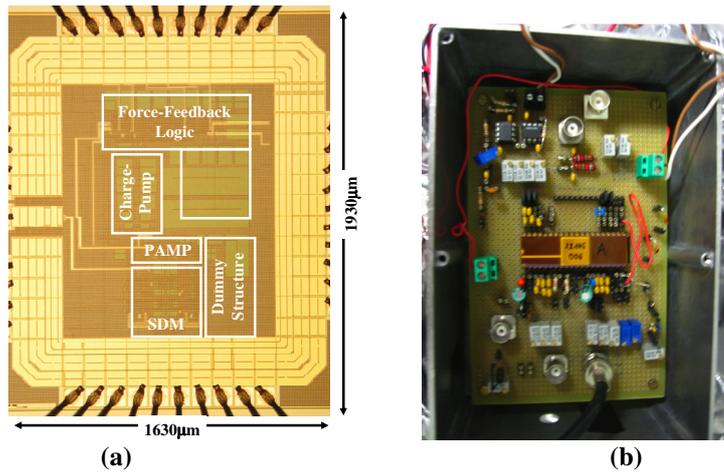


Figure 4-19 : (a) Microphotograph of the Readout ASIC, (b) Readout ASIC mounted on the bread-board

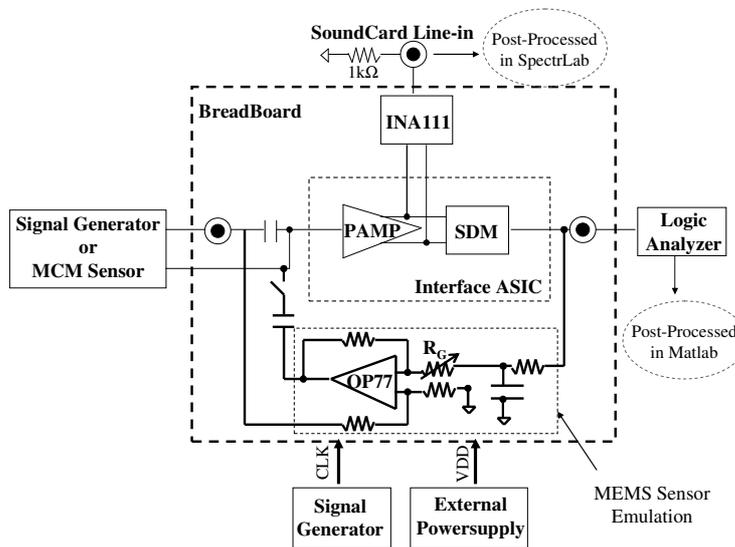
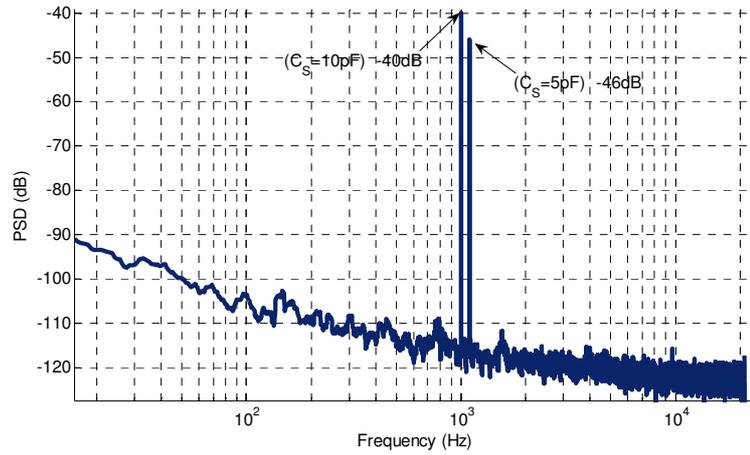


Figure 4-20 : Measurement Setup

#### 4.4.2 Stand-alone Preamplifier

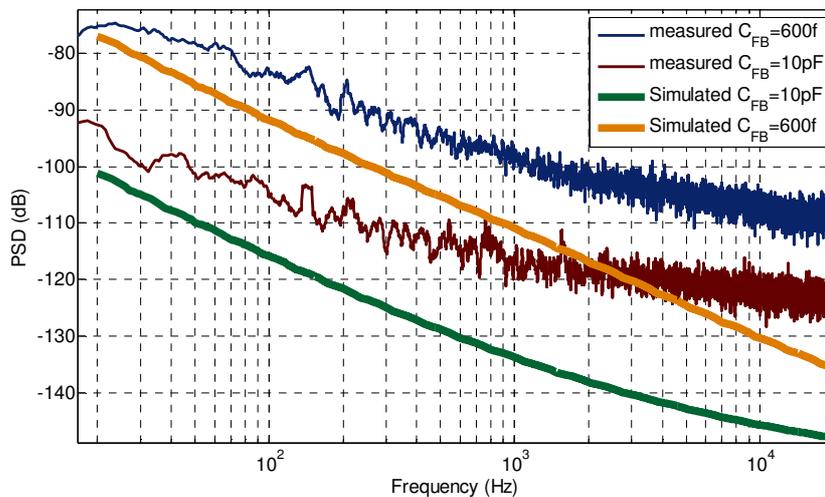
The preamplifier is biased with 30uA of current by adjusting its external resistor-based current bias source. The bias voltages for cascode devices are also set externally. The power supply voltage is 3.3V and common voltage is fixed at mid-rail, i.e. 1.65V. The clock for the SC-CMFB of the PAMP is 2.5MHz. The sigma-delta modulator is turned off by turning off its main bias current and bias voltages; however, the first-stage sampling in SDM at the output of PAMP is still active because of the clock.

To minimize the effect of bread board parasitics on the PAMP operation, 10pF of feedback caps are connected externally to the PAMP. The input signal is 20mVpp, which represents 1Pa for MCM with sensitivity of -40dBV/Pa. Figure 4-21 shows the output of the PAMP with two different input capacitors, i.e. 10pF and 5pF.



**Figure 4-21 : Measured Gain of the PAMP for two different input caps,  $C_S=5pF$ ,  $C_S=10pF$ , while  $C_{FB}=10pF$  in both cases**

The integrated noise in the audio band is -70dB and -80dBA. The flicker noise is the dominant noise as expected from the simulations, hence A-weighting achieves a 10dB improvement in SNDR. The THD is below 0.1% so the preamplifier for 1Pa does not cause considerable distortion. The output noise of the PAMP is inversely related to the integrating cap size. In this case, since we have connected 10pF as integrating cap to avoid any parasitics coming in from the board, the noise floor goes down by almost a factor of 26dB. The noise floor of the PAMP is shown in figure 4-22 with and without external 10pF capacitors, where the internal feedback capacitors are 600fF. However, in this case, where the noise gets a boost by 26dB, the input signal also gets a similar boost; therefore, SNR remains the same for the same input capacitance. In the case when the sensor would be connected to the PAMP, the value of the integrating capacitor would depend on the sensor capacitive variations and the swing we require at the output of PAMP for our reference point, i.e. 1Pa. For these results, the dc-bias at the input nodes of the PAMP is set by external resistors of 100M $\Omega$ . The dc-bias is controlled externally to nullify the offset at the output of PAMP as discussed later.



**Figure 4-22 : Simulated and Measured Noise for different values of feedback capacitance**

It can be seen from figure 4-22 that measured and simulation noises have a slope of 10dB/decade for low frequencies, i.e. below 3-4kHz, which signifies the dominance of the flicker noise in that band. However, for frequencies above 5kHz, the slope of the measured noise reduces. The measured noise with 10pF of feedback capacitor flattens around -120dB, which signifies the dominance of instrumentation noise. The measured noise with 600fF feedback capacitor has a higher slanting slope above 5kHz than the noise with 10pF of feedback capacitor, which signifies the noise of bias resistors shaped by the NTF of the PAMP.

The measured noise is compared with the simulated noise in figure 4-23 for two different values of external bias resistor. However, the integrated noise is -76dB and -85dBA respectively for the case when an external bias resistor of 1GΩ is used highlighting an increase of 6dB in the SNDR as compared to the case when the external bias resistor is 100MΩ.

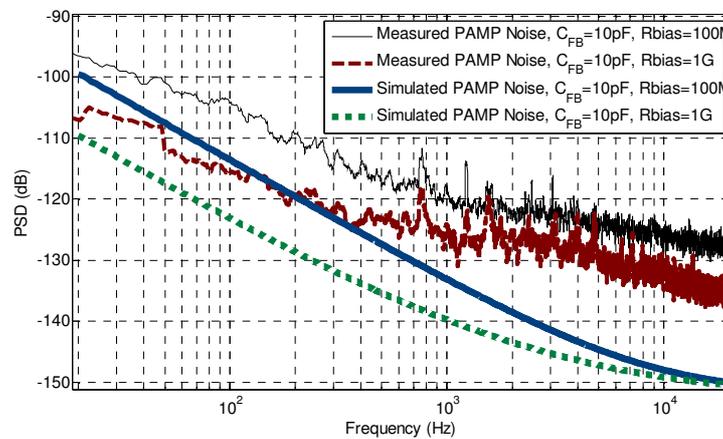


Figure 4-23 : Measured Noise of the PAMP for different values of external bias resistor  $R_B$  and feedback capacitance

Figure 4-24 plots the noise of the PAMP for two bias different currents. It can be seen that the noises are not very different. The reason is that flicker noise and the bias resistor dominates the total noise of the PAMP instead of the thermal noise. Thus the total noise is not affected by the increase in bias current.

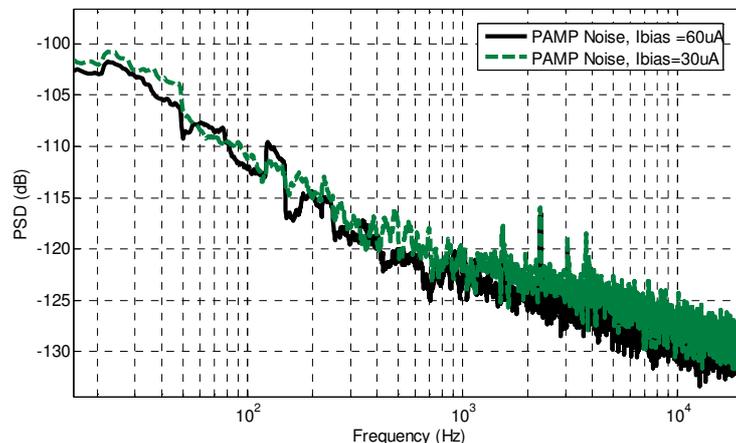
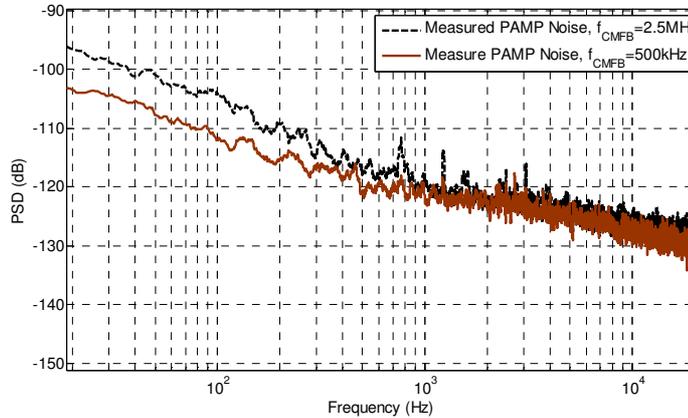


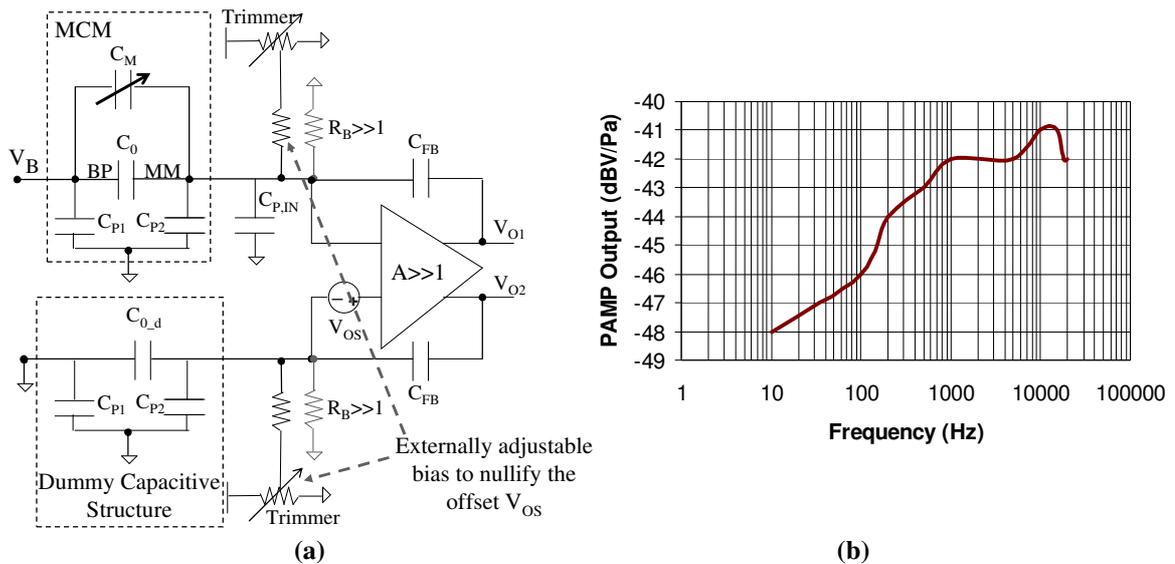
Figure 4-24 : Output Noise of the PAMP for different values of bias current

To check if the switching noises from the SC-CMFB of the PAMP has any effect on the total noise of the PAMP, the clock frequency is reduced down to 500kHz from 2.5MHz. Figure 4-25 plots noise for two cases, i.e. one with  $f_{CMFB}=2.5\text{MHz}$  and other  $f_{CMFB}=500\text{kHz}$ . It can be observed the reduction of CMFB clock frequency does not affect the noise floor considerably.



**Figure 4-25 : The effect of SC-CMFB of the PAMP on the output noise**

As mentioned above that the mismatch in the PAMP can cause considerable offset at the output of the PAMP since there is no dc-feedback, hence the offset appears at the output multiplied by the gain. To minimize this offset, adjustable voltage-references are connected through external  $100\text{M}\Omega$  resistors are connected to the virtual ground nodes of the PAMP. Using these voltage references, a counterbalancing offset can be created at the input of the PAMP, as shown in figure 4-26a. Figure 4-26b shows the frequency response of the PAMP for an equivalent input signal of  $1\text{Pa}$ .



**Figure 4-26 : (a) Offset zeroing through external bias resistors, (b) Frequency Response of the PAMP**

### 4.4.3 Stand-alone Sigma-Delta Modulator

Figure 4-27a plots the noise floor of the SDM when the PAMP is turned off and the dc-point at the inputs of SDM is setup by external high-value resistors. The SDM OTAs are biased at 30uA by externally adjusting the variable resistor based current source. The integrated inband noise is -67dB and a-weighted noise is -69dBA. There is no dominance of flicker noise for low-frequencies and it seems that the thermal noise from the first stage of the SDM is the dominant noise, till around 30kHz, from where the quantization noise starts dominating. From the Simulink simulation shown in the section 4.2.2, the expected integrated noise floor is -76dBA and the KTC noise of the first stage is the main bottleneck. To differentiate if this noise is due to the thermal noise of the OTA in the first stage of the KTC noise of the first-sampler, the bias current of the SDM OTA is adjusted externally. However, this does not affect the measured output noise; therefore, it is most likely the KTC noise of the first sampler. Figure 4-27b shows the measured SNDR versus the simulated SNDR. Due to the higher KTC noise in measured noise spectra, there is a loss of ~7dB in SNDR as compared to the expected value. Another observation is that the SNDR starts decreasing for higher-inputs before the expected overload of the SDM. The inspection of noise spectra reveals that it contains high even harmonics, which points to mismatch in the symmetry of the fully-differential SDM. This lack of symmetry is the reason that SNDR starts reducing earlier than expected. The measured FOM of the sigma-delta is  $0.142 \times 10^{-3}$  [56].

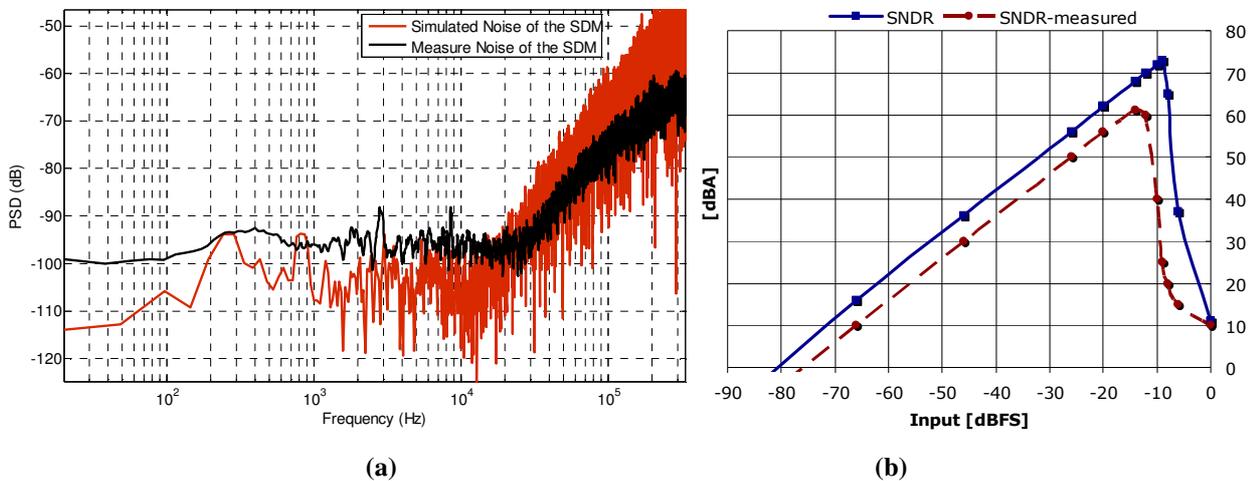


Figure 4-27 : (a) Measure Noise Floor of the Standalone SDM, (b) Measured SNR and SNDR of the stand-alone SDM

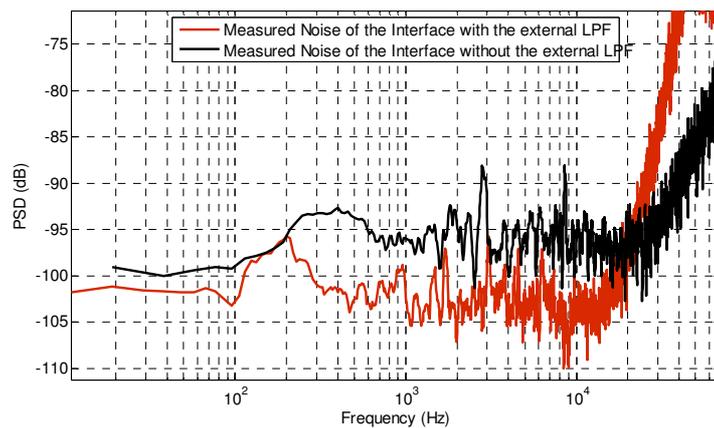
### 4.4.4 A Simplified Sensor Emulation and measurement results for a Closed-Loop System

Unfortunately, due to the unavailability of an MCM, the force-feedback functionality of this interface could not be tested with an actual MCM in the feedback loop. However, a simplified sensor emulation is performed by connecting the output of the SDM to a passive low-pass filter to roughly evaluate the

behavior of the closed-loop system with respect to noise. The external low-pass filter, as shown in figure 4-20, mimics the low-pass behavior of the MEMS microphone, with a corner frequency of 20kHz. This LPF regenerates the digital PDM output into an analog signal. A difference amplifier computes the difference between regenerated signal and the input from a signal generator. The difference is fed to the read-out interface, as shown in figure 4-20. The gain of the low-pass filter in audio-band can be controlled by adjusting the gain-resistor  $R_G$  in figure 4-20.

A complete reproduction of the electromechanical-analogy based model, shown in Simulink, is not done here. The inertial and damping behaviors of the sensor concern mostly the dynamics of the system, which is not the main concern of this emulation-based testing. This specific test primarily attempts to find out two things. First, to check if the complete interface is stable in the closed-loop configuration. Second, to understand the effect that a feedback would bring to the interface with respect to noise.

Figure 4-28 shows the output of the interface with the external LPF in a close-loop system against the open-loop output. The gain of the LPF is set to 2. Since the interface noise is inserted after the external low-pass filter, therefore, this filter acts as a high-pass filter for this noise. The zero induced by this external LPF is around 10kHz in the NTF of the cascaded CT+DT SDM. It can be seen that the quantization noise slope is different from the open loop configuration, after 10kHz, which signifies an extra pole in the NTF. However, these results show the effect of actual MCM on the noise of the interface in the force-feedback configuration would be negligible. This is because the dc-gain of MCM's frequency response is very low and the extra zeros, although are in the audio band, are far from the unit circuit, therefore, having negligible impact of noise of the interface. Another observation is that the closed-loop system is stable with the first-order simplified LPF in the feedback loop.



**Figure 4-28 : Measured noise at the digital output of Interface with and without the external LPF**

#### 4.4.5 Power Consumption

Table 4-3 shows the breakage of the power consumption inside the readout interface. The total current consumption is 300 $\mu$ A for a single power supply of 3.3V. Major part of the power consumption is consumed in force-feedback and digital control logic in driving the large force-feedback capacitors.

**Table 4-3 : Power Consumption per Components inside the Readout Interface**

<b>Power Consumption per Component inside the Readout Interface</b>	
Complete Device	990 $\mu$ W @ 3.3V of power-supply
Pre-Amplifier	330 $\mu$ W
Sigma-Delta Modulator	363 $\mu$ W - Internal Biases for OTA $\rightarrow$ 132 $\mu$ W - Integrators $\rightarrow$ 231 $\mu$ W
Force-Feedback Logic and Digital Controls	297 $\mu$ W

## 4.5. Conclusion

This chapter presented the design details and measurement results of a readout interface for MCM with force-feedback functionality. As mentioned above, FFB was employed in this interface to enhance the linearity of the MCM sensor to minimize the effect of drift in its mechanical parameters on the readout. The interface consisted of a PAMP, a SDM and force-feedback logic and it utilized the digital PDM output of SDM as the counter-balancing electrostatic force feedback. Unfortunately, due to the unavailability of MCM sensor, the interface could not be tested in with a MCM; however, the presented simulation and measurement results highlight the feasibility of FFB for a single-ended MCM, suggesting considerable improvements in the linearity and stability of the complete system. The PAMP in this interface achieved parasitic-insensitive readout by reducing the signal around the parasitics through a high-gain OTA in a capacitive feedback configuration. This method of parasitic compensation does not recycle noise like the previously-mentioned bootstrapping scheme. This PAMP performs conversion of the single-ended MCM input to a fully-differential output in a more area and power efficient way as compared to interface-I. This single-ended to differential conversion was also required for the application of FFB to the single-ended MCM sensor. To match the dummy branch closely to the MCM capacitance, the interface employed a dynamic matching logic. This dynamic matching scheme was relatively area and power-hungry since it used a capacitance-bank of large poly capacitors ( $\sim 5$ pF each) and it incurred charging (and discharging) of these capacitors at the rate of modulator clock. The PAMP in this interface suffered from considerable offset since there was no dc-feedback for the high-gain OTA; therefore, the device mismatches appeared at the output multiplied with the gain of OTA. The designed SDM was a third-order single-loop single-bit modulator, similar to previous interface, and achieved an FOM of  $0.142 \times 10^{-3}$ . This interface was designed in  $0.35\mu\text{m}$  CMOS technology and consumed a total current of  $300\mu\text{A}$  for a single supply of 3.3V. The total area of the readout ASIC was  $1930\mu\text{m} \times 1630\mu\text{m}$  including the pad-ring. The analog output of the PAMP achieved 40dBA/Pa of SNDR and 76dBA of DR at the digital output.

# Chapter 5

## Readout Interface – III

### 5.1. Introduction

This chapter presents the design details and measurement results for the third readout interface for MCM, which is a multi-function two-stage chopper-stabilized preamplifier, as shown in figure 5-1. The preamplifiers for the first two interfaces implemented a straightforward C-to-V conversion. The reason for keeping the MCM preamplifier simple was to achieve a robust low-noise translation of the MCM capacitive variations with minimal loading of the sensor. However, as mentioned above, the design of the preamplifier is strongly dependent on the characteristics of the MCM and subsequently, the design of the PAMP affects the backend design. The presented multifunction PAMP in this chapter demonstrates that embedding functionalities in the PAMP, such as controllable gain and offset, does eventually improve a complete integrated readout interface with respect to performance, area and cost. This PAMP also employs chopper-stabilization, which is not commonly used with MCM preamplifier due to its switched nature.

The first-stage of this two-stage PAMP is a source-follower (SF) buffer while the second-stage is a chopper-stabilized capacitive gain-stage with controllable gain. Since the MEMS sensor is buffered by the SF, the gain provided by the capacitive-gain stage is well-controlled and is independent of the MEMS capacitance. The PAMP implements a controllable high-pass filtering functionality to filter-out low-frequency noise signals below 100Hz, such as wind-hum. Furthermore, the PAMP controls its output offset through a feedback loop. A controlled offset can be used to modulate the idle-tones in the subsequent SDM out of the audio band. The PAMP employs chopper-stabilization in the second-stage to modulate offset and flicker noise out of the audio band and converts the single-ended input from MEMS microphone into a differential output. The expected sensitivity of MCM for this PAMP is close to  $-40\text{dBV/Pa}$  without considerable parasitic capacitors at the sensing node. This sensitivity is higher than that of the above-mentioned MCMs. Therefore, unlike the previous interfaces, the main objective of the first stage of the PAMP is to buffer the capacitive variations of the MCM into a voltage signal with minimal loading of the sensing node without employing parasitic compensation. The second-stage can be used to provide a digitally-controllable gain-factor to adjust the output of PAMP within the desired area of the subsequent SDM's dynamic range. The major components of this two-stage PAMP are shown in figure 5-1.

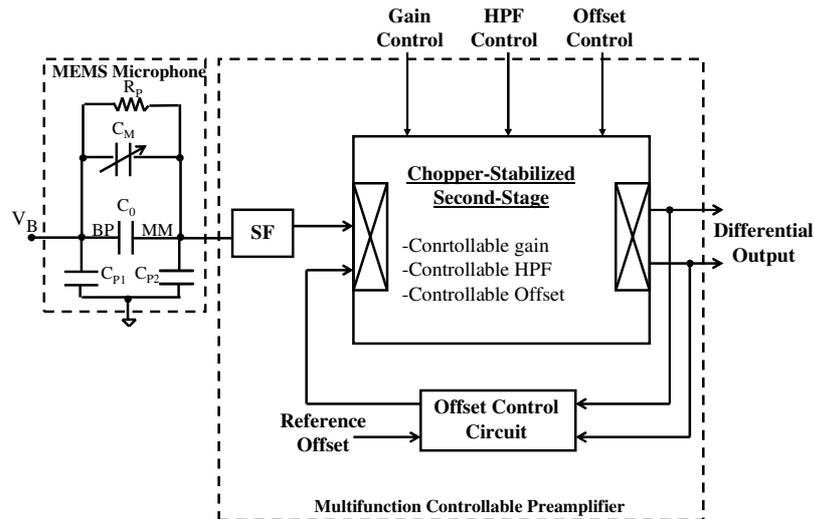


Figure 5-1 : Two-Stage Multifunction PAMP for MCM

## 5.2. Behavioral Description and Simulations of the Multifunction PAMP

### 5.2.1 Comparison between Correlated-Double-Sampling and Chopper-Stabilization for the PAMP

Switched techniques for the mitigation of offset and low-frequency noise problems, such as chopper-stabilization (CHS) and correlated-double-sampling (CDS), are commonly not employed for MCM PAMPs. The reason behind this is to avoid the spurious switching effects from affecting the MEMS structure. The lack of symmetry in the single-ended MCM structure further aggravates the effect of switching spurs such as charge-injection and clock-feedthrough. However, if the MCM is shielded from switching spurs through a source-follower buffer, used as the first stage of the PAMP, the second-stage can employ either CHS or CDS to improve noise and offset performance. In the following text, both techniques are qualitatively evaluated for a MEMS microphone PAMP. Ultimately, CHS is selected due to the reasons discussed below.

The CDS operation is typically partitioned into several-phases; one phase sampling the offset and the subsequent phase subtracting it from the output [43]. Therefore, the output of a PAMP employing CDS is not always available for pick-up by the subsequent components of the interface. If a DT-SDM follows the PAMP, the PAMP might need to run at the same clock as the SDM for synchronization. This can be power-hungry. A chopper-stabilized PAMP output is essentially continuous-time, therefore, no synchronization is needed and CHS based PAMP can run at lower clock-frequency than SDM.

Furthermore, the CDS approach samples the input signal for offset-cancellation while CHS modulates the signal to higher frequencies. Therefore, the fold-over noise in CDS can be considerably high depending on the sampling frequency. The fold-over factor in CDS would require the wide-band thermal noise of the first stage to be lowered by the same factor, which would make the first stage power-

hungry. [43] suggests that for a fold over factor greater than 5, the output baseband noise is dominated by the fold over component of the wideband thermal noise. CHS; however, does not suffer from foldover noise since there is no sampling of the signal. [52] suggests if the chopping frequency is ten times higher than the corner of the flicker noise, i.e.  $f_{chop} > 10f_c$ , less than 10% increase in the total inband noise results because of the flicker noise fold over.

CHS based approaches suffer from residual offset and harmonics at the modulation frequency. However, this can be mitigated by low-pass filtering the CHS output. This low-pass filtering could be embedded in the SDM that follows the PAMP.

Therefore, CHS is selected in this case for mitigating the offset and flicker noise of the second-stage.

### 5.2.2 Offset Control and High-Pass Filtering Schemes

As mentioned above, the dc-bias resistor used to establish operating point at the high-impedance input node of PAMP gives rise to a low-frequency pole along with the effective node capacitance. To achieve consistent readout sensitivity in the audio band, this pole should be outside the audio band below 20Hz. This requires a high value resistance, i.e. above  $G\Omega$  for typical values of MCM capacitors. The approaches commonly used to implement this resistor, as shown in figure 5-2, are zero-biased diodes [32], subthreshold transistors [34] and pseudo-PMOS resistors [33]. The incremental resistance offered by these schemes is above  $G\Omega$  and the resulting pole lies in mHz range. However, to implement a high-pass filtering functionality that could be used to attenuate signals till 100Hz, this pole should lie above 100Hz. In other words, the value of bias resistor should be in  $M\Omega$  range. The lower bound on the value of capacitors is set by KTC noise since CHS will employ switching in the PAMP. Therefore, the value of capacitors cannot be decreased to increase the corner frequency of this pole. On the other hand, the above-mentioned approaches to implement the high-value resistor do not offer any mechanism to lower the resistance value in a controlled manner. Besides, these resistors are dependent on signal-swing across them; therefore, they limit the maximum gain-factor and swing at the output of PAMP.

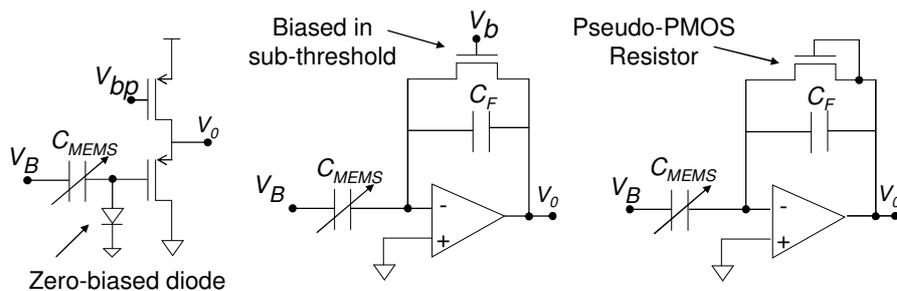


Figure 5-2 : Typical approaches to implement the high-value bias resistor for the PAMP

Figure 5-3a shows a scheme to achieve a pole inside acoustic band, around 100Hz, without using large bias resistors. This scheme utilizes miller effect due to which the feedback capacitor  $C_F$  appears multiplied with the gain of OTA at the virtual ground node as  $C_L$ . The nodal analysis of the circuit shows that the pole frequency  $\omega_p$  is dependent not only on  $R_B$  and  $C_F$  but also on gain of OTA  $A$ . Therefore, by using a low value resistor and high-gain OTA, a low-frequency pole can be achieved for a  $C_F$  of few pF.

Figure 5-3b shows the frequency response of the PAMP where  $A=60\text{dB}$ ,  $R_b=1\text{M}\Omega$  and  $C_F=1\text{pF}$ . The high-pass corner lies around 100Hz. A  $\text{M}\Omega$  resistor can be implemented using high-resistance poly, which gives us a linear resistor independent of the signal swing across it. Consequently, by controlling the value of this resistor or the feedback capacitor,  $\omega_p$  can be pushed up or down, thus implementing the required high-pass functionality for low-frequency hum. However, as the HPF corner moves to high-frequencies, the noise contribution of the bias resistance in the band increases, as shown in figure 5-3b, which should be taken care of.

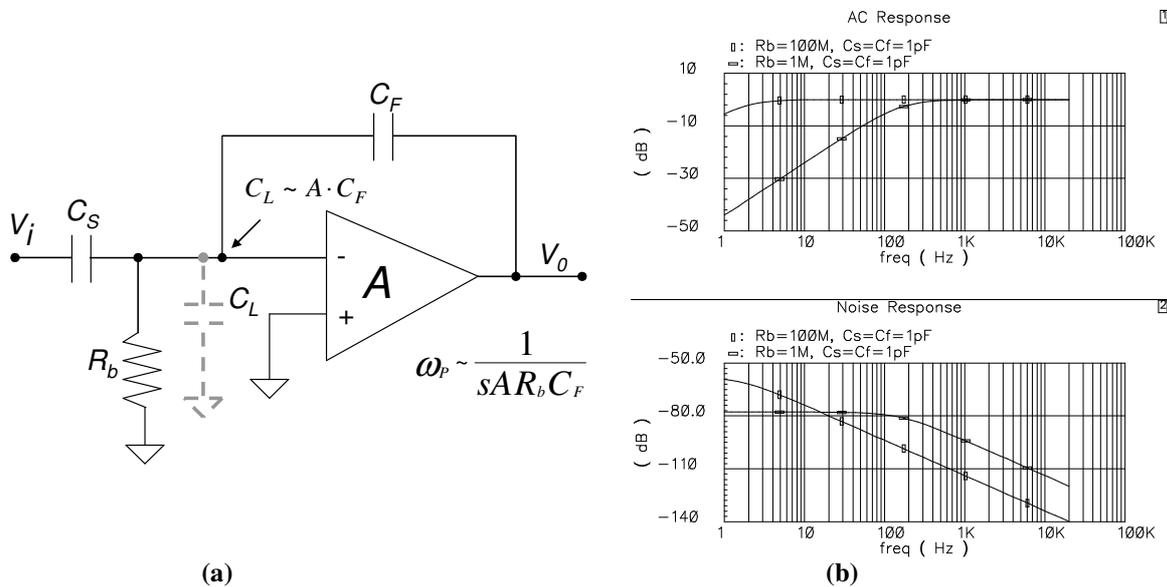
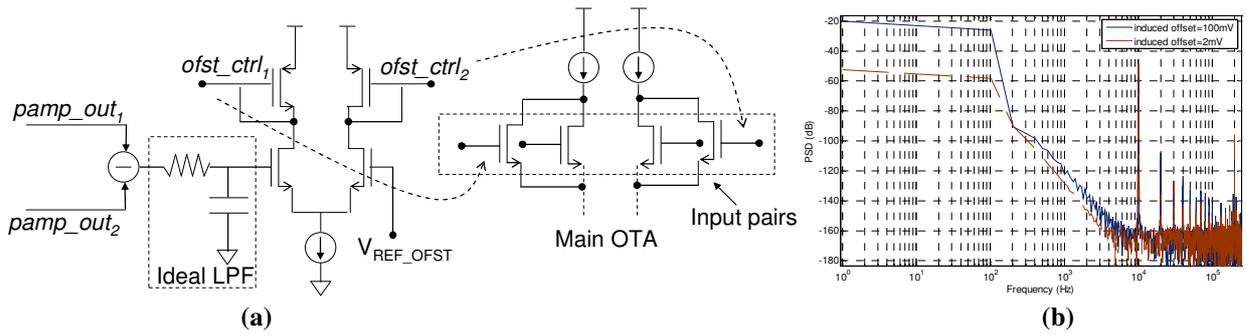


Figure 5-3 : (a) PAMP Scheme which utilizes Miller-effect to achieve low-frequency pole using low-value resistors, (b) Frequency Response of the scheme in (a)

The offset control scheme can be described as extracting the output offset, comparing it with a reference and then tweaking the PAMP to get the desired offset [40]. The critical part of this scheme is the implementation of offset extraction using a narrow-band low-pass gm-C filter [81-83]. Available approaches in the literature implement the required filter through a combination of two approaches. First, by reducing the gm through current scaling, current division and source-degeneration [81]. Second, by increasing the load capacitance through impedance boosting techniques [83].

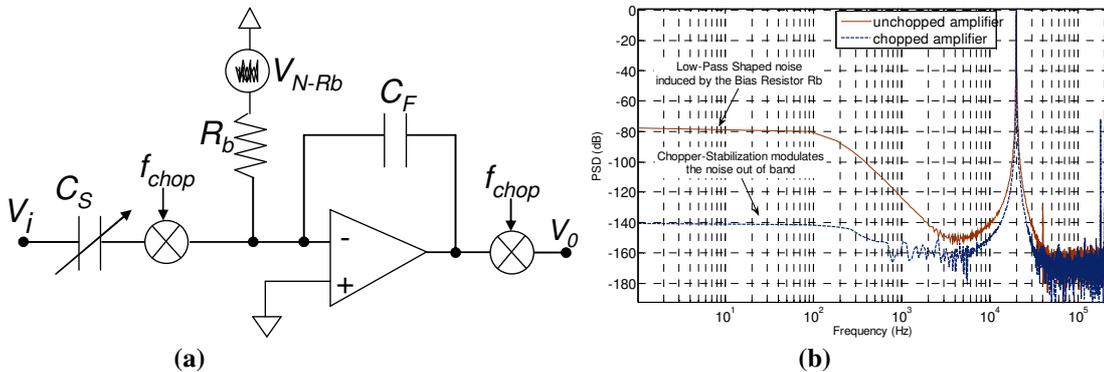
Figure 5-4a shows a semi-ideal setup for offset-control, where offset is extracted using an ideal narrow-band low-pass filter. The differential offset controlling signal is generated by a semi-ideal difference amplifier. The offset control signal is applied to a differential input of OTA which is connected in parallel with the main input pair. Figure 5-4b shows the output offset of the semi-ideal PAMP when an offset of 2mV and 100mV is induced through the offset-control circuit.



**Figure 5-4 : (a) Representation of the Offset Control Scheme, (b) Induced Offsets of 2mV and 100mV in the PAMP through Offset-Control-Circuit**

### 5.2.3 Chopper-Stabilizing the above-mentioned Scheme

Chopper stabilizing the above-mentioned scheme would modulate the OTA offset and low-frequency flicker noise outside the band. At the same time, modulation would also affect the noise from the bias resistor. The modulation scheme shown in figure 5-5a modulates the thermal noise  $V_{N-Rb}$  out of band as shown in figure 5-5b. However, the actual system is implemented in a slightly different manner, in which the demodulation switches are inside the capacitive feedback loop, as shown in figure 5-6a.  $V_{N-Rb}$  is first modulated out of band and then low-pass shaped. Therefore, the noise of bias resistor is not completely modulated out of band by our scheme and is discussed in detail in the following text.



**Figure 5-5 : (a) Application of Chopper Stabilization to the above-mentioned scheme using ideal VerilogA blocks for multiplication with carrier, (b) Modulated and Un-modulated outputs of the scheme in (a)**

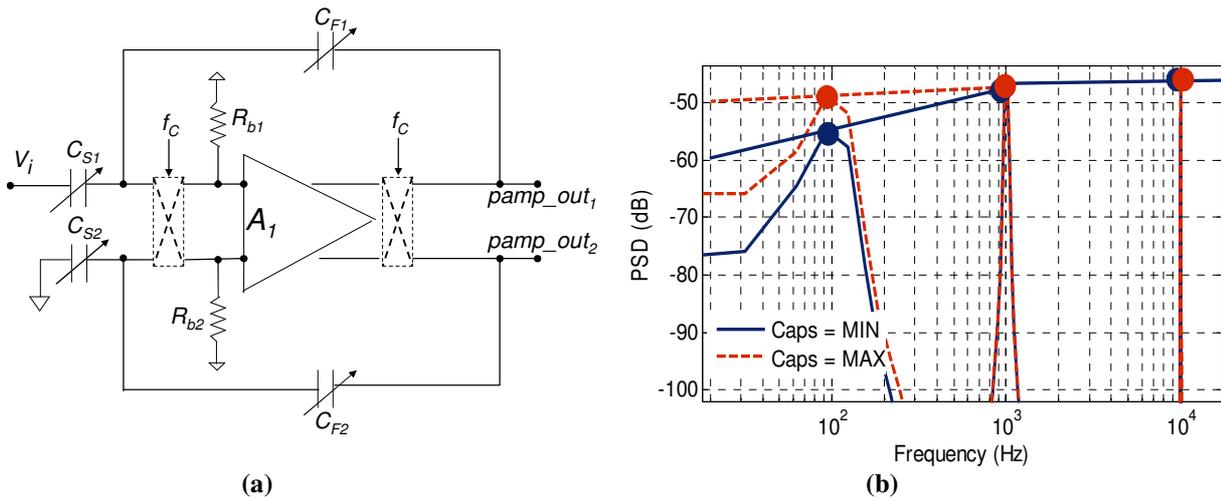


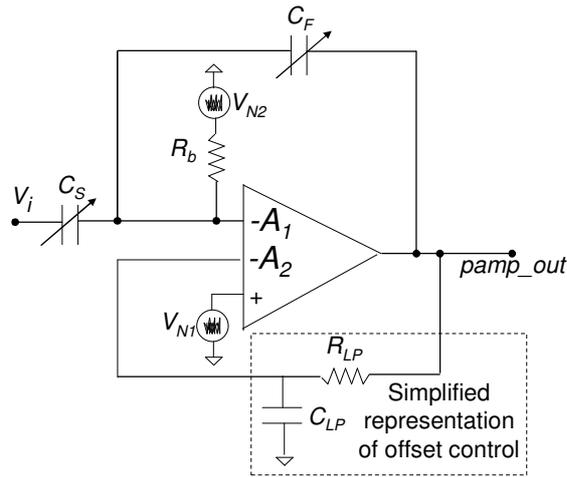
Figure 5-6 : (a) Actual Chopper Stabilization Scheme with switches, (b) High-Pass Filtering in the PAMP

Due to input-choppers, the signal at the virtual ground node is now modulated. Therefore, the high-pass filtering implemented through miller-effect does not affect the modulated signal. However, the switching due to the chopping sees  $R_b$  as a load through which the signal slowly leaks. Therefore, we still get the required high-pass functionality, as shown in the figure 5-6b, controlled by the integrating capacitors of the PAMP.

### 5.2.4 Noise Analysis of the Second-Stage of PAMP

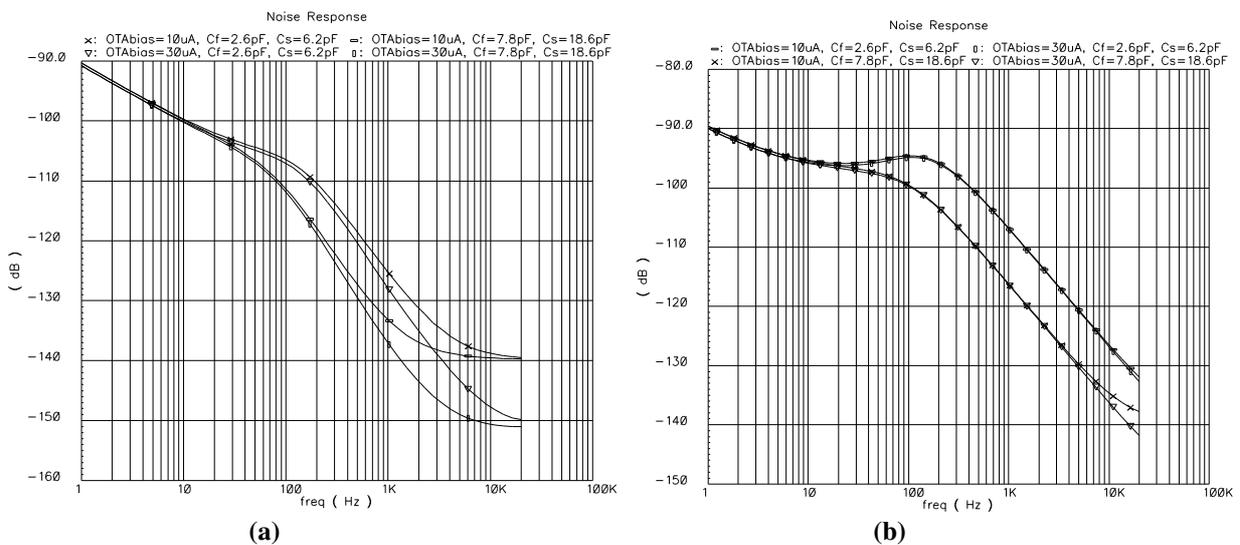
The second stage of the PAMP, along with its bias resistor  $R_b$  and the offset control circuitry, are represented as a simplified schematic in figure 5-7.  $V_{N1}$  is the input referred noise of the OTA while  $V_{N2}$  is the thermal noise injected by the miller bias resistance  $R_b$ . The offset control circuit (simplified as  $R_{LP}$  and  $C_{LP}$ ) is connected to the second input pair of the OTA which has reduced gm. The reason for having separate input pairs for main input and the offset-control feedback is to have different input-to-output gain-factors to minimize the effect of noise from the offset-control-circuit, as explained in detail in section 5.3.3. The two input-pairs of OTA are connected as follows

- The main input-pair is connected to the bias resistors  $R_b$  and the input capacitors  $C_s$ , represented by  $A_1$  in figure 5-7.
- The other input pair has a reduced gm than the main input pair and the output of the offset control circuit is connected to this input pair, represented by  $A_2$  in figure 5-7.



**Figure 5-7 : Simplified Representation of the Second-Stage with Chopping for Noise Analysis**

Figure 5-8 shows the simulated output noise of the simplified representation shown in figure 5-7 for different cases. Figure 5-8a shows the case when the bias resistor  $R_b$  is made noiseless and noise is plotted for different values of bias current and capacitors. Figure 5-8b shows the case when bias resistors also contribute to noise and it can be seen that the noise of the bias resistor is the dominant factor in the output noise, contributing 89% of the total noise. Since the thermal noise of the resistor has a flat wide-band shape, the shape of the output noise actually demonstrates the frequency-response of the closed-loop noise-transfer-function in PAMP. The dc-feedback due to the offset-control-circuit is very weak at frequencies above 100Hz due to its narrow-band characteristic. Therefore, the noise of bias resistor at the input of OTA gets multiplied with the high-gain low-pass transfer-function of the capacitive feedback configuration. The dc-gain for  $V_{N2}$  is set the ratio between  $R_B$  and  $R_{LP}$ , i.e.  $R_{LP}/R_B$ . As discussed later,  $R_{LP} \sim 300M\Omega$ , therefore the dc-gain for the  $V_{N2}$  is  $\sim 46dB$ , taking thermal noise  $V_{N2}$  ( $-136dB$ ) up to  $-90dB$  in figure 5-8b.



**Figure 5-8 : Simulated PAMP Output Noise, (a)  $R_b$  is noiseless, the contribution from the OTA and the Offset Control Circuit (i.e.  $V_{N1}$ ) is shown, (b)  $R_b$  also contributes to noise**

Figure 5-9 intuitively explains the behavior and the shape of the output noise with chopping. The noise at the input of the OTA (OTA’s noise + Bias resistor noise) is first modulated at the output and then it is multiplied with the closed-loop noise transfer function. The thermal noise of the bias resistor has flat wide-band spectra, therefore modulation does not affect it and its effective power in the audio-band remains the same. Therefore, when this modulated thermal noise is multiplied with the closed-loop NTF, the output noise is similar to the one shown in 5-8b.

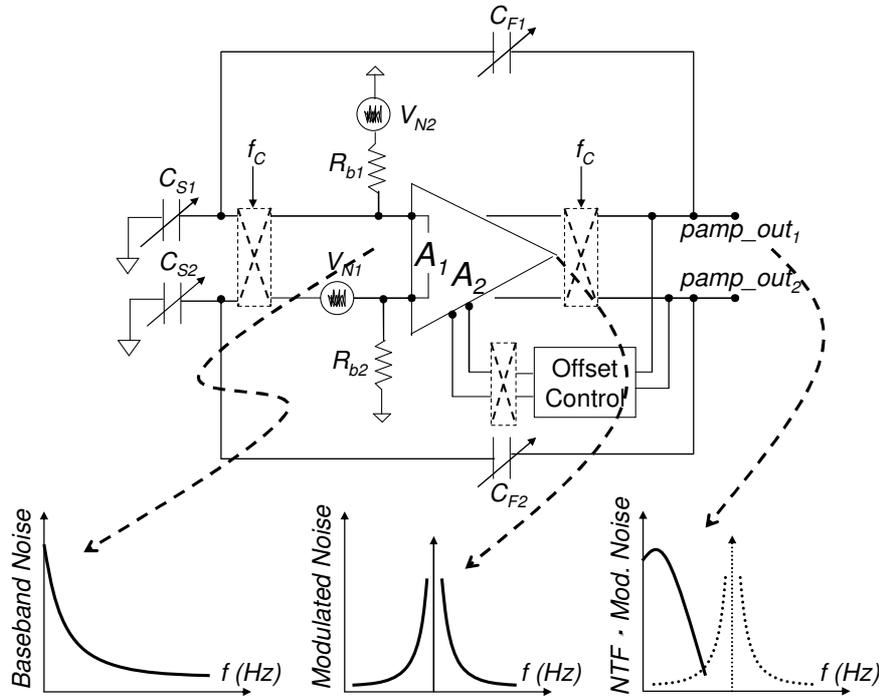


Figure 5-9 : Intuitive Explanation of the Noise at the output of the Chopper-Stabilized PAMP

The chopping frequency is selected as 200kHz. The switching in choppers gives rise to KTC noise. The KTC noise of the input capacitors  $C_s$  is critical because the signal swing around them is not as large as around  $C_f$ . The effect of KTC noise is checked by inducing a Matlab-generated thermal noise in the input-chopper switches. The noise-file is sampled in Cadence transient simulation at 1MHz. The total noise power of the induced noise is -96dB. The chopping takes place at 200kHz, therefore, the total power of the KTC noise is spread in a bandwidth of 200kHz. This is similar to oversampled noise spectra in which the total noise is spread over a larger bandwidth. Therefore, the KTC expression includes the OSR term as following:

$$KTC - noise_{AUDIOBAND} = \sqrt{\frac{k \cdot T}{C_L \cdot OSR}}, OSR = \frac{200kHz}{20kHz} = 10 \quad (\text{Eq. 5-1})$$

The resulting integrated output noise in audio band for the above-mentioned setup is -106 dB, which signifies a reduction by a factor of  $\sqrt{(OSR)} \sim 3$ , from -96 to -106dB. Therefore, the sizes of the input

capacitors can be relaxed by factor of 3. The sizes of input capacitors are kept larger than 5pF. This also implies that the KTC noise can be decreased by increasing the chopping frequency. However, this improvement will come at the cost of having a decreased gain of OTA at the chopping frequency, hence reduced miller effect for the bias resistors and increased power consumption.

### 5.3. CMOS Design Details

The complete PAMP is shown in figure 5-10 and the following text discusses the CMOS design details. The input and feedback capacitors of the second-stage ( $C_S$  and  $C_F$ ) can be digitally adjusted externally. The PAMP can be configured to have three different values of gain; 2.5X, 5X and 7.5X. The high-pass corner can also be controlled by adjusting the feedback capacitors. The offset at the output of PAMP can be controlled by controlling the reference offset voltage  $V_{REF\_OFST}$ . The underlying technology is 0.35 $\mu$ m 2P/3M twin-well CMOS technology and the targeted supply voltage is 1.8V. The capacitors are implemented using poly capacitors for an area efficient layout.

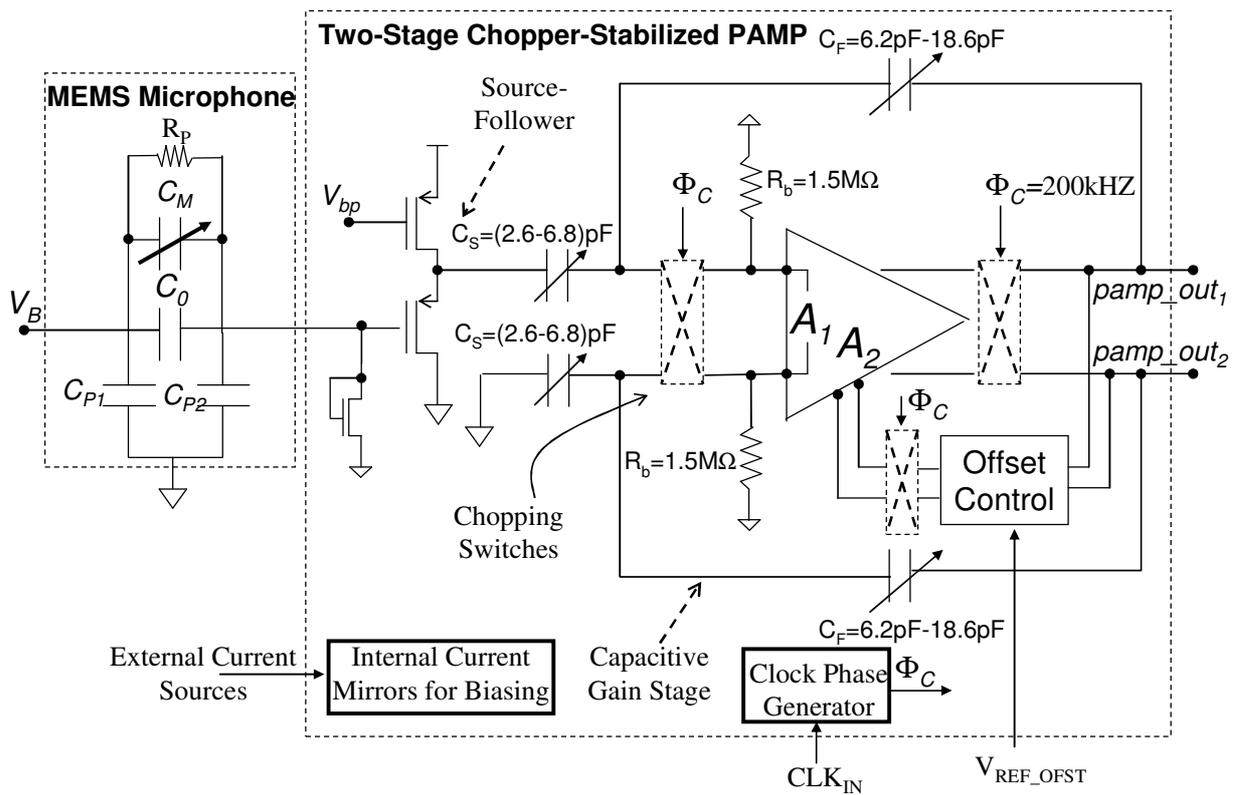


Figure 5-10 : Major Blocks of the Two-Stage PAMP

### 5.3.1 The Source Follower

The SF, shown in figure 5-11a, utilizes a PMOS input device since a PMOS device achieve lower flicker noise as compared to NMOS. The dimensions of input PMOS are achieved through several simulation-iterations to have a balance between flicker noise and the parasitic capacitor at the sensing node. The SF is biased with bias currents of 10uA – 20uA. The dc-biasing at the high-impedance input node of the SF is achieved through pseudo-PMOS resistor  $R_B$ . Figure 5-11b shows the frequency response of the SF with an input capacitor of 1pF.

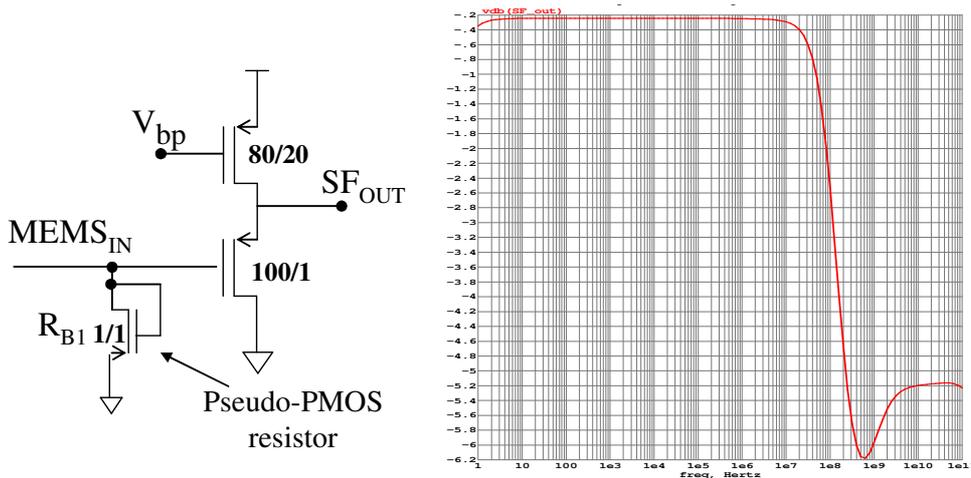


Figure 5-11 : Source -Follower First-Stage and its Frequency Response

Table 5-1 : Noise Details of the Source-Follower

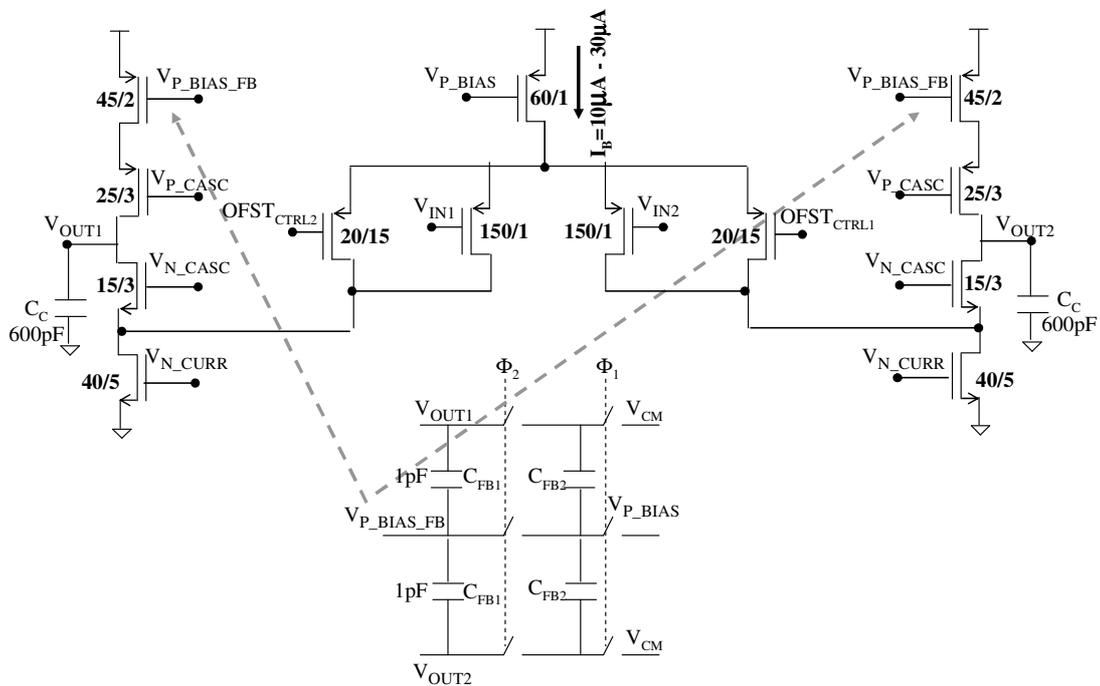
Noise Data for Source-Follower				
Bias Current	Integrated Noise (20-20kHz)	Flicker Noise	Integrated Noise (A-weighted)	Operational Region for Input Device
10uA	5.01uVrms	4.6uVrms	3.00uVrms	Weak inversion
20uA	4.75uVrms	4.5uVrms	2.97uVrms	Saturation

### 5.3.2 The OTA for Second-Stage of the PAMP

The designed folded-cascode OTA is shown in figure 5-12. The swing for the reference 1Pa signal for maximum gain (7.5X) is 150mVpp. Therefore, the maximum swing required for 10Pa for maximum gain is 1.5Vpp. The OTA is fully differential so this swing represents 750mVpp swing in one output branch, which the folded-cascode shown in figure 5-12 can meet. This OTA uses a PMOS input pair, which helps in achieving lower flicker noise although the achievable gm is lower; however, the targeted PAMP scheme does not require OTA to have high UGBW. Chopping will modulate the flicker noise out of audio band so the noise-specs of the OTA can be kept relaxed. The total noise of the OTA, including the flicker noise, in the audio band is kept 5uVrms – 10uVrms and is tabulated in table 5-2. The size of

input PMOS pair is kept high to keep the devices in weak-inversion to maximize the gm-to-bias-current ratio. The offset due to device-mismatch is maximized in weak inversion. However, chopping would modulate the offset out-of-band; therefore, weak-inversion region can be utilized to maximize the gm.

OTA has two input pairs. The main input pair is used for the main capacitive-feedback in the PAMP configuration. The second input pair has a reduced gm and is connected to the output of offset-control-circuit to control the offset at the output of PAMP. This is similar to a differential-difference-amplifier [32,84]. The advantage of keeping two different input pairs for capacitive feedback and dc-feedback from the offset-control-circuit is that both paths can have separate gain to the output independent to each other. As discussed later in detail, reduced gain for the second input pair helps in minimizing the impact of offset-control-circuit's noise.



**Figure 5-12 : Fully-Differential Folded Cascode OTA for the PAMP with SC-CMFB**

Table 5-2 shows that flicker noise (< 4kHz) adds up to 70%-80% of the total noise of OTA. This is also obvious from the A-weighted noise output, which shows considerable noise reduction. Hence, it can be assumed that due to the modulation of flicker noise through chopper-stabilization, the noise-specs of the OTA would be well below  $5\mu\text{Vrms}$ , which represents the targeted noise floor of -106dB.

Table 5-2 : Noise Details of the OTA

Noise Data for OTA				
$I_{bias}$	Integrated Noise (20Hz-20kHz) Input-Ref	Total Inband Noise (20-20kHz) Output-Ref	Flicker Noise Output-Ref	A-weighted Total Inband Noise Input-Ref
30uA	5.8uVrms	0.122Vrms	0.098Vrms	1.65uVrms
20uA	6.09uVrms	0.146Vrms	0.113Vrms	1.70uVrms
10uA	6.78uVrms	0.151Vrms	0.113Vrms	1.85uVrms

OTA can be biased with bias currents of 10uA – 30uA. The bias voltages for cascade-devices are generated by a cascade of diode-connected devices, which have the same size as the cascode itself. This is done to make the bias generating devices to closely track the process variations with the cascode device. The size of cascode devices is adjusted to get the required gain and keeping the non-dominant pole from deteriorating the phase margin. The critical part of OTA gain is the gain at chopping frequency since the OTA processes the modulated signal. Therefore, the UGBW of the OTA should be properly adjusted to achieve at least a gain of 40dB at 200kHz. The sizing of the PMOS and NMOS current sources are adjusted to minimize their gm and at the same time minimize their flicker noise contribution. The PMOS current source will be connected to the CMFB circuit so their sizes are adjusted to ensure that the CMFB loop has the same UGBW as the differential feedback loop. Figure 5-13 and table 5-3 show the gain and phase for different bias currents of OTA.

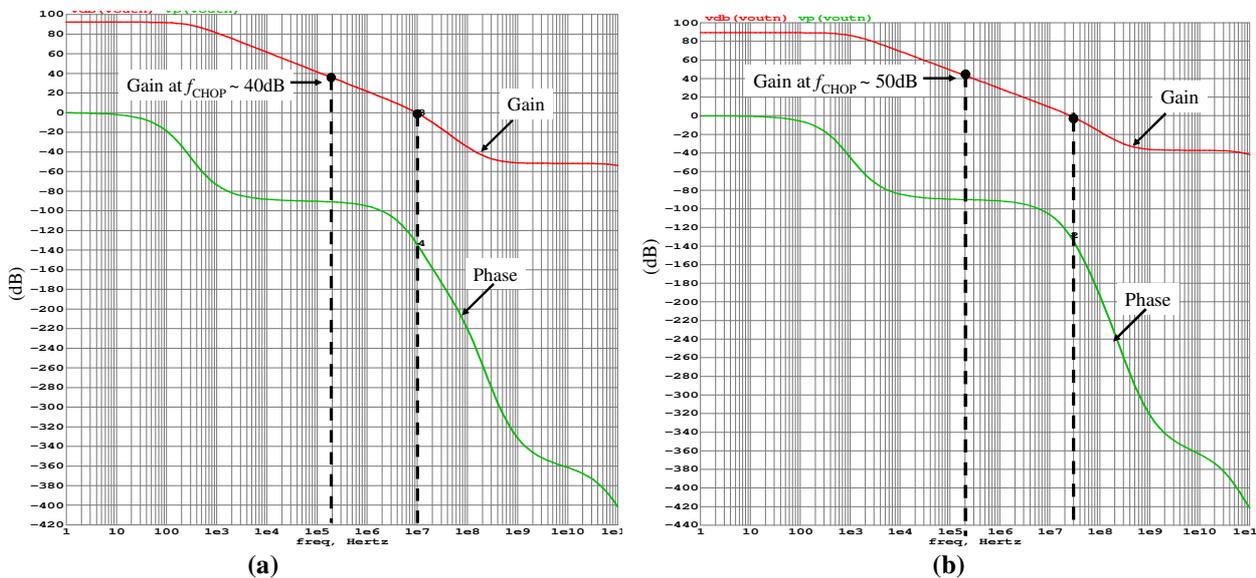
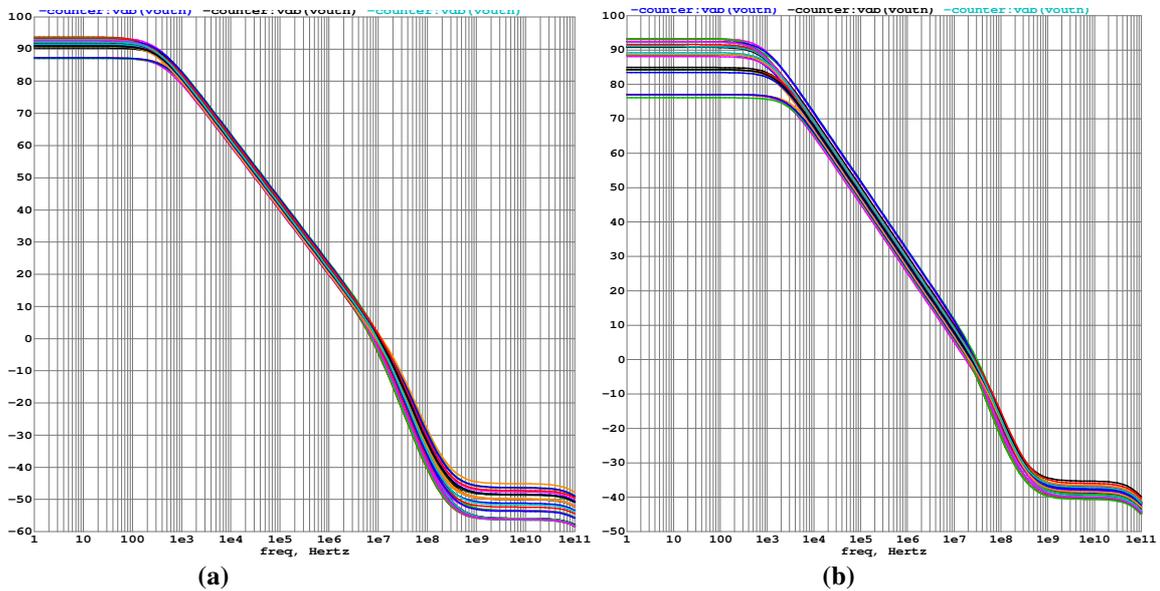


Figure 5-13 : Gain and Phase of the Folded-Cascode OTA, (a)  $I_{bias}=10\mu A$ , (b)  $I_{bias}=30\mu A$

**Table 5-3 : Gain and Phase of the OTA**

<b>Gain and Phase for Different Bias Currents</b>			
<b>Bias Current (<math>I_{bias}</math>)</b>	<b>Diff. DC Gain</b>	<b>Gain @ 200kHz</b>	<b>Phase</b>
10 $\mu$ A	90 dB	42 dB	58 $^{\circ}$
20 $\mu$ A	90 dB	46 dB	56 $^{\circ}$
30 $\mu$ A	90 dB	50dB	54 $^{\circ}$

The overall topology of the PAMP is a continuous-time chopper-based topology. However, a switched-capacitor CMFB is used to regulate the common-mode output voltage of OTA since a CT-CMFB is relatively complicated to stabilize and is power-hungry. The capacitor sizes in the SC CMFB are selected to keep the charge-injection and KTC noise low. The size of switches is kept minimal. This reduces their charge injection. Only the switches connected to the output of OTA are transmission gate switches since they experience large swing. SC-CMFB causes a switching noise component at its operational frequency, in our case; it is same as chopping frequency, i.e. 200kHz. This switching noise is outside audio-band. Either a low-pass filter at the output of PAMP or an inherent low-pass filtering in SDM can be utilized to attenuate these high-frequency switching peaks. OTA has a single-ended output swing of 1.3V (~0.2V to ~1.5V) and a slew-rate of ~4V/ $\mu$ S. Figure 5-14 shows the gain and phase of OTA for different corner cases, showing that OTA's gain remains above 40dB @ 200kHz for all cases.



**Figure 5-14 : Gain of the OTA for corner cases and different temperatures, (a)  $I_{bias}=10\mu$ A, (b)  $I_{bias}=30\mu$ A**

### Layout and its Considerations for OTA

The PMOS input differential pair, the main current bias for the input pair and the differential input pair for the offset control are all inter-digitated to make them immune to cross-chip gradients. The dif-

ferential output branches of the OTA are placed close to each other to minimize the mismatch due to gradients. The layout is shown in the following figure 5-15.

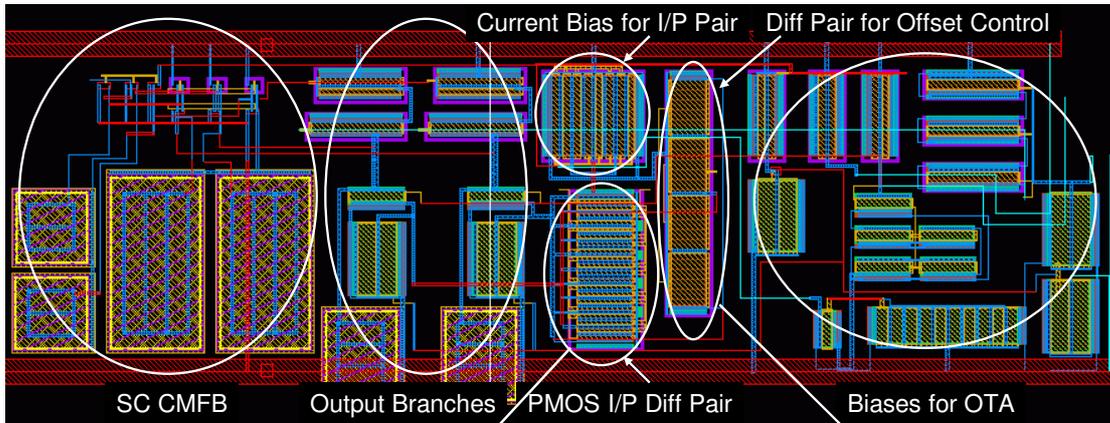


Figure 5-15 : Layout of the Folded-Cascode OTA

### 5.3.3 Offset Control Circuit

The offset control circuit (OCC) is based on a narrow-band low-pass gm-C filter, as shown in figure 5-16. To achieve a low-frequency corner, a low-gm OTA is implemented. The reduction in  $g_{m1}$  is achieved mainly by current-scaling. The  $g_{m1}$  is further reduced by keeping the W/L ratio of the input device of OTA low. PMOS devices are employed for input-pair since they achieve lower-gm than the NMOS counterparts. The OTA is loaded with another matching PMOS pair with the same gm to achieve a unity gain at dc. This load-pair provides a load resistance of  $1/g_{m2}$ . Hence the overall gain is defined by the ratio between  $g_{m1}$  of input pair and  $g_{m2}$  of the load. Ultimately, the outputs of the low-gm OTA ( $V_{LP1}$  and  $V_{LP2}$ ) are loaded with large caps (60pF). The frequency response of the OCC is shown in figure 5-18, showing a corner of LPF between 10Hz-100Hz of the low-gm LPF.

The externally dictated offset, i.e.  $V_{REF\_OFST}$ , is used to convey the required offset at the output of PAMP.  $V_{REF\_OFST}$  is referred to the common-mode voltage of the ASIC, i.e. 900mV. To compare the computed offset with  $V_{REF\_OFST}$ , the output common-mode of the low-gm OTA is maintained at 900mV. For this reason, a CT CMFB circuit, shown in figure 5-17a, is employed to control the CM output voltage of the low-gm OTA. A difference amplifier, shown in figure 5-17b, compares the offset at the output of OTA with  $V_{REF\_OFST}$ , generating a differential offset-control signal for the main OTA of the second-stage of the PAMP.

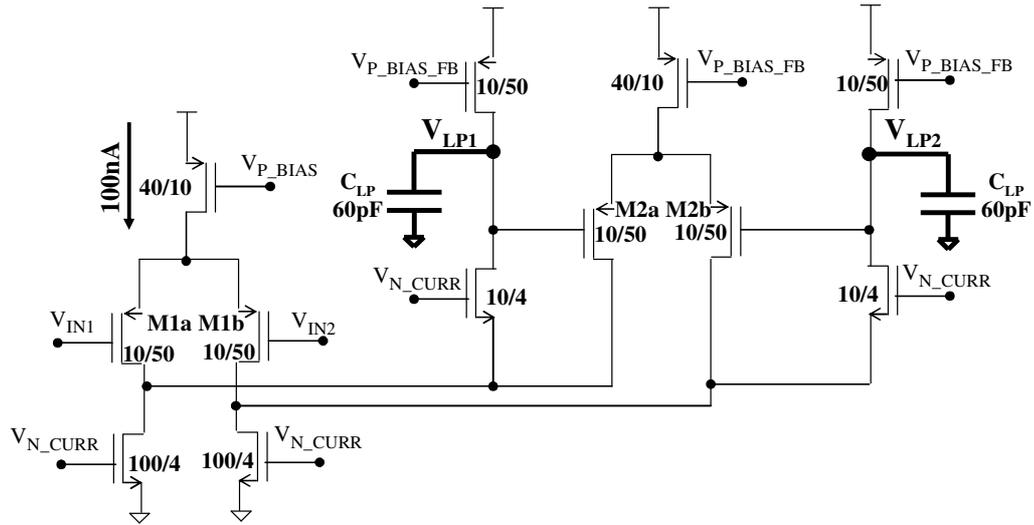
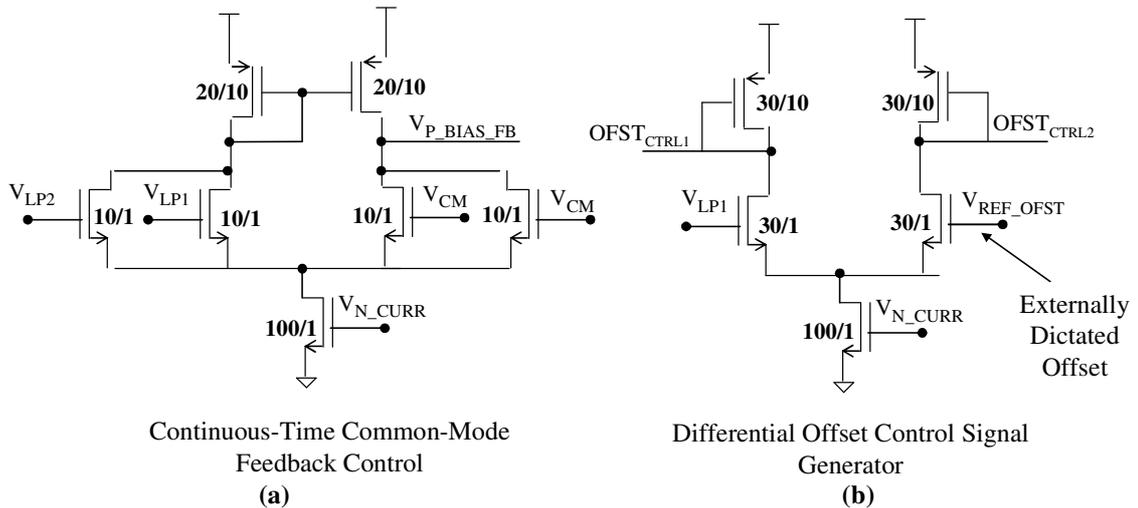


Figure 5-16 : Narrow-Band gm-C Filter with Unity DC-Gain



Continuous-Time Common-Mode Feedback Control (a)

Differential Offset Control Signal Generator (b)

Figure 5-17 : (a) CMFB Circuit for the OCC, (b) The Differential Offset Control Signal Generator for the OCC

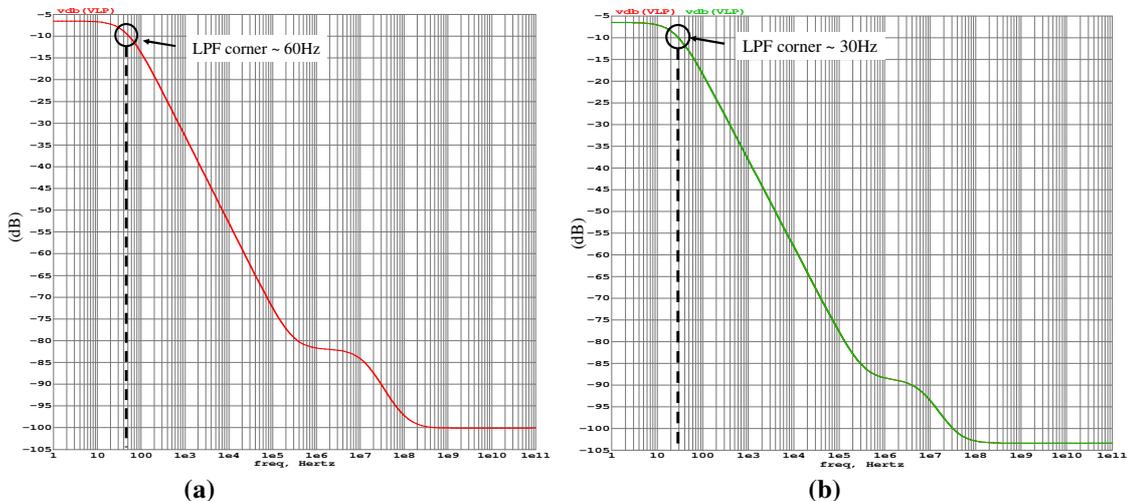


Figure 5-18 : Frequency Response of the OCC, (a)  $I_{bias}=100nA$ , (b)  $I_{bias}=50nA$

Table 5-4 : Characteristics of the Offset Control Circuit

Offset Control Circuit Characteristics			
Diff. Gain	LPF attenuation at 100Hz	$I_{bias}$	$C_L$
0 dB	-14 dB	50nA	64pF
0 dB	-8 dB	100nA	64pF

The integrated output-referred noise of the offset-control-circuit is  $50\mu\text{Vrms}$  in the audio-band. However, the output of the offset-control-circuit is connected to a separate input pair of OTA and not to the main input pair. This separate input pair has 100-times reduced gm than the main input-pair. Therefore, the output noise of the offset-control-circuit is attenuated by that factor, thereby falling within the targeted noise of  $5\mu\text{Vrms}$ . Since the OCC employs low bias current to achieve a narrow-band low-pass filtering, directly lowering its noise was difficult. Therefore, this attenuation factor provided by reduced gm of extra input pair of main OTA takes care of it. The resulting loss in the gain of the control loop, which should ideally have a gain of unity, is compensated by the difference-amplifier.

### Layout and its Considerations for Offset Control Circuit

The PMOS input pair, PMOS load pair and the current source are inter-digited to make them immune to cross-chip gradients. The layout of the OCC is shown in figure 5-19.

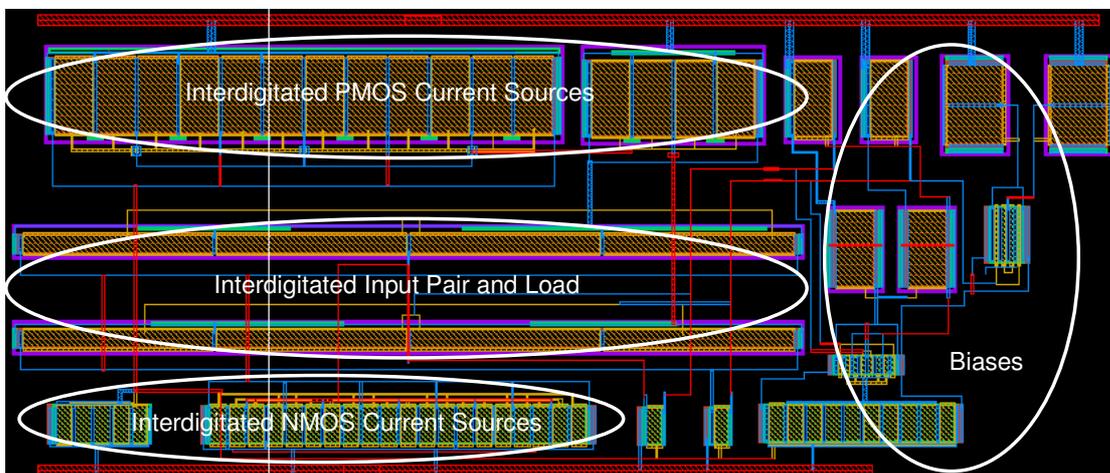


Figure 5-19 : Layout of the OCC

### 5.3.4 Adding Spare Devices as a Fail-Safe Mechanism

Some spare devices are added in the PAMP core as a fail-safe mechanism. In case the PAMP does not work, a spare device can be connected with other devices through focused-ion-beam (FIB) technique. The following text presents the criteria on which spare devices were added. There are three major components in the pre-amplifier; OTA and its biases, SF and its biases, Offset Control Circuit and its biases. For

OTA, a spare device for the input pair would only increase the gm and cannot affect the behavior in case of failure. The input pair current bias can cause current mismatch but not a failure. NMOS current source for the output branch is kept large enough to accommodate mismatches in the current flowing through them. Mismatch in PMOS current source for the output branches cannot cause a failure. However, the biases for the cascades-devices in the main OTA require spares. If their value is incorrect, OTA will not operate at all. Both of these biases can be adjusted by adding extra current to the stacked bias generation branch. For the SF, the input PMPS does not need a spare since that will not affect the behavior in case of a failure and the current bias cannot cause a failure. For OCC, the input pair and load will not affect the behavior in case of a failure. For the NMOS current source, enough margin is provided incase the PMOS source vary their current sourcing. CMFB control and Differential Control Generator also do not require spares. Therefore, only OTA requires two spare devices, i.e. for its cascode bias generation. At the system level, two spares for the bias resistor  $R_b$  are provided. This is to make sure that if the HPF corner goes higher than expected, the extra resistors can be used to bring it down by a factor of 2. Figure 5-20 shows the location of spares in the layout of the ASIC.

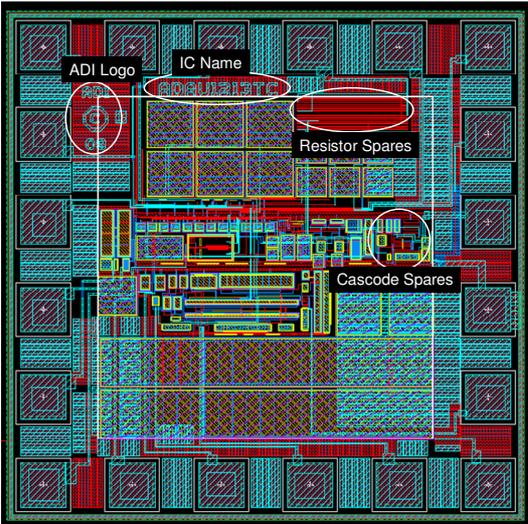


Figure 5-20 : Location of Spares in the Layout

## 5.4. Measurement Results

### 5.4.1 The Measurement Setup

Figure 5-21a shows the microphotograph of the ASIC with dimension  $950\mu\text{m} \times 950\mu\text{m}$ . Figure 5-21b shows the ASIC mounted on the PCB. Figure 5-22 shows the measurement setup. The differential output of the preamplifier is connected to an on-board instrumentation amplifier AD8250. The output of AD8250 is connected to the PC through the line-in of the sound card. The sound card has input imped-

ance around  $1k\Omega$  and here the instrumentation amplifier serves as the driving buffer for the preamplifier. SpectraLab software is used to analyze and post-process the measured output of the PAMP.

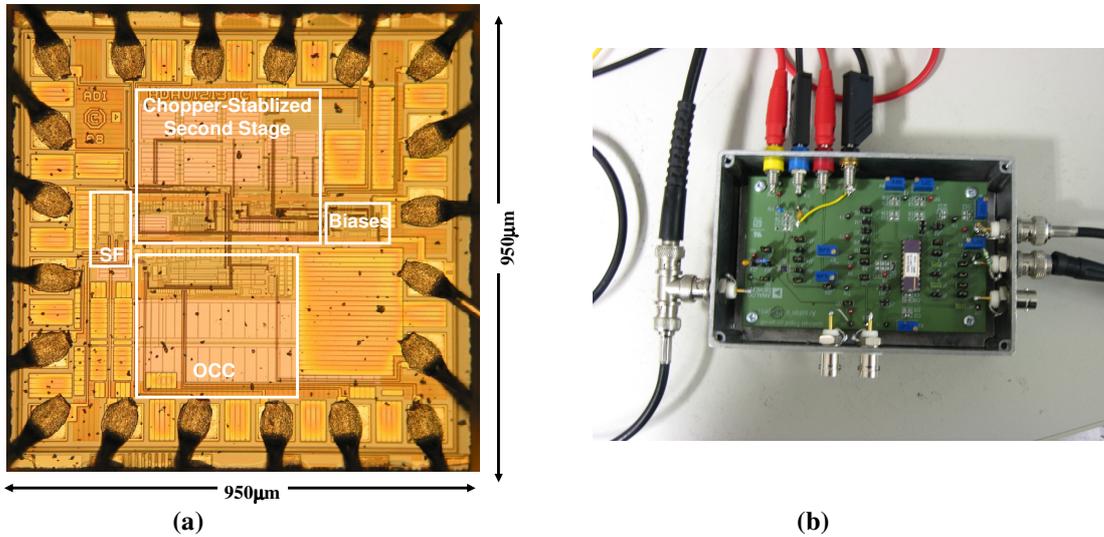


Figure 5-21 : (a) Microphotograph of the PAMP, (b) ASIC mounted on the PCB

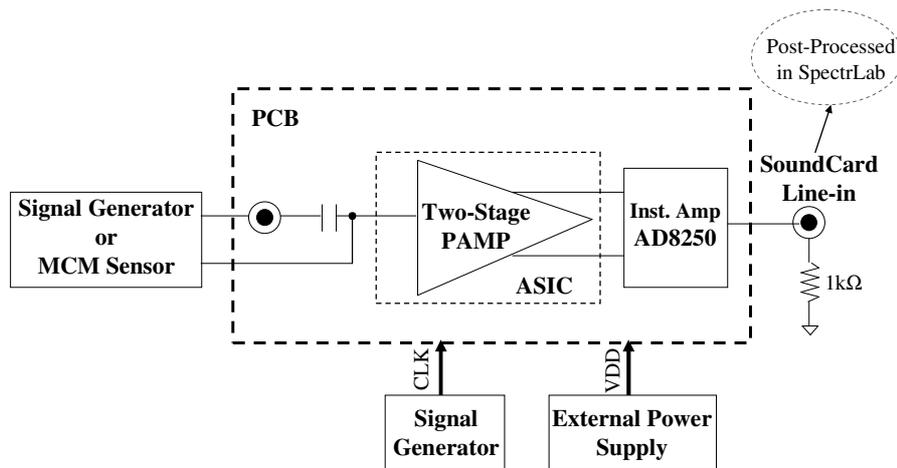


Figure 5-22 : The Measurement Setup

## 5.5. Measurement Results

### 5.5.1 Output of the Source-Follower

Figure 5-23 shows the measured noise at the output of the source-follower. The integrated noise in 20Hz-20kHz band is -93dB and -99dBA. The achieved SNDR at 1Pa is 53dB and 59dBA where the signal peak is at -40dB for an input signal of 10mVp, which represents equivalent voltage swing for a pressure of 1Pa. The source follower is biased by 20uA of bias current. The measured noise is higher than the expected noise and this is due to the fact that the instrumentation is hitting its measurement limits. The

sound-card employs 16-bit sampling. The AD8250 amplifier is used to amplify the output of the SF, to bring it to the dynamic-range of the PC's sound card. The AD8250 has a flicker noise corner of 100Hz starting at 80nVrms/rtHz (-141dB) and settling down to thermal noise of 20nVrms/rtHz (-154dB). The measured noise spectrum is dominated by the flicker noise till ~4kHz which can be seen by the 10dB/decade slope of the spectra. After 4kHz, the slope decreases and spectrum becomes relatively flatter. This signifies the dominance of thermal noise of sound-card. The slant above 4kHz is also due the loading of AD8250 by the 1kΩ sound-card impedance.

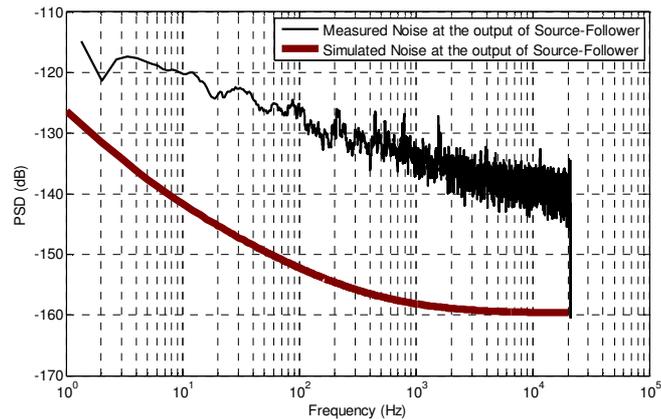


Figure 5-23 : Simulated and Measured Noise at the output of the Source-Follower

### 5.5.2 Output of the Second Stage of PAMP

Figure 5-24 shows the noise at the output of the preamplifier for two different cases. Table 5-5 lists the integrated noise and SNR for both cases and Figure 5-25 plots the SNR/SNDR versus the equivalent sound pressure level. The OTA bias current for OTA and OCC is 20μA and 100nA respectively.

- Case I : when the input and integrating caps are at their maximum, i.e.  $C_{FMAX}=7.6\text{pF}$  and  $C_{SMAX}=18.6\text{pF}$ .
- Case II : when the input and integrating caps are at their minimum, i.e.  $C_{FMIN}=2.6\text{pF}$  and  $C_{SMIN}=6.2\text{pF}$ .
- 

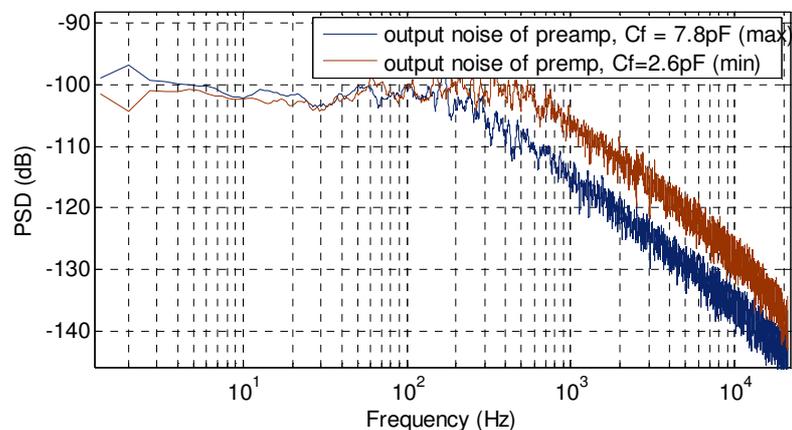


Figure 5-24 : Measured Noise at the output of the Second-Stage of the PAMP for minimum and maximum values of the Feedback-Capacitors controlled through external digital signals

Table 5-5 : Measured Noise of the Two-Stage Preamplifier

Parameter	Case I	Case II
Integrated A-weighted Noise	-72 dBA	-79 dBA
Signal peak at 1Pa	-35 dBA	-35 dBA
SNDR at 1Pa	39 dBA	44 dBA

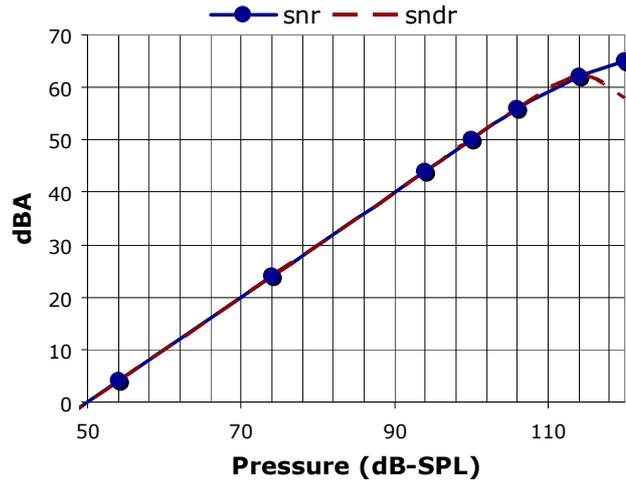


Figure 5-25 : SNR and SNDR at the output of PAMP versus the equivalent sound pressure level

Figure 5-26 plots the measured noise of PAMP for different values of OTA bias current. It can be seen that change in the bias current does not considerably affect the output noise. This implies that OTA noise  $V_{NI}$  is not the dominant noise at the output of the PAMP.

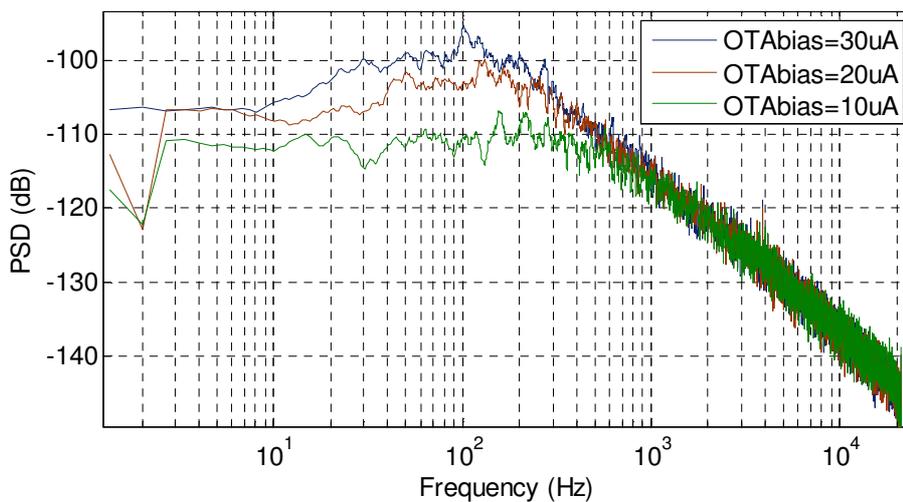
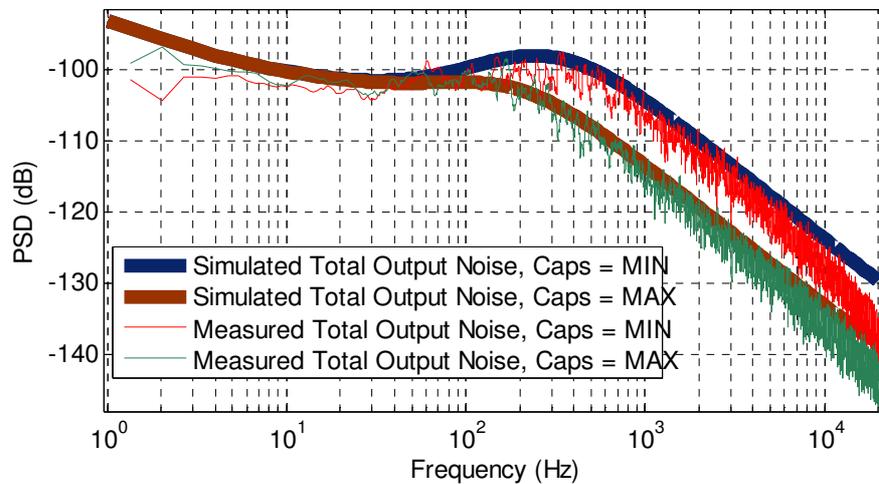


Figure 5-26 : Measured Noise of the PAMP for different bias currents of the OTA

Figure 5-27 plots the simulated noise and measured noise of the PAMP, for minimum and maximum capacitor values. It can be seen that a good agreement exists between simulations and measure-

ments. It can be concluded that noise of the bias resistors  $R_b$  is the dominant noise at the output of PAMP, as expected from the simulations.



**Figure 5-27 : Comparison between Simulated and Measured Noise of the PAMP for minimum and maximum value of the feedback capacitor**

The offset-control circuit serves as a dc-feedback for the preamplifier. This offset-control circuit is a low-pass filter implemented by a low-gm OTA and a high-load-capacitance. The frequency response of the offset-control circuit falls below -20dB after 200Hz, and thus the feedback becomes negligible for frequencies above this band. This is the required behavior since offset-control circuit should control the dc-offset at the output but should not disturb the low-frequency side of the audio-band. From DC to 50Hz, the offset control has approximately a dc-gain of -6dB. The offset control circuit provides a negative feedback with a gain of -6dB for frequencies below 50Hz and then its feedback decreases by 20dB/decade from there on. This feedback cancels the uplifting slope of the output noise, hence the output noise becomes flat below 100Hz. Between 100Hz-300Hz, the gain of offset-control circuit is decreasing so the noise between that frequency finds a relatively open loop NTF and thus rises up. However, around 300Hz, the pole in the NTF makes the noise ramp down by 20dB/decade. This rise and fall-down effect creates a little bump in the noise spectrum at the output of the PAMP between 100Hz and 300Hz.

### 5.5.3 Offset Control

Table 5-6 lists the residual offset at the output of the preamplifier, when the offset-control-circuit is turned off. This means, that there is no dc feedback in the PAMP in this case. The fact that this offset is almost the same for different samples highlights that it could be the residual offset and not the mismatches in OTA or PAMP capacitors. Bias currents for all the components are kept the same and at their maximum value for all the samples. This is done to keep the gm of the OTA at its maximum value, which lets us see the maximum effect of the residual offset. The gm of the OTA for all the samples is almost

same, indicated by the same output swing, i.e. 48mVpp-49mVpp for an input signal of 20mVpp signifying a gain of 2.5X. The output offsets are within 136mV-140mV. This consistency in gm and offset advocates the fact that it is the residual offset due to the input chopping switches. Since there is no dc-feedback in the circuit in this case, the residual offset appears at the output multiplied by the gain of OTA.

**Table 5-6 : Residual Offset at the output of the Preamplifier with maximum gm of OTA**

Residual Offset at the Output of Preamplifier with maximum gm of OTA	
Sample #	Residual Offset at the output of the preamplifier
1	140mV
2	136mV
3	139mV
4	140mV

To further validate that this offset at the output is the residual offset, the gm of the OTA is reduced by reducing its bias current and loading the output with 100pF caps. The output offsets reduce to 23mV-25mV as listed in Table 5-7. The signal swing at the output also decreases which signifies reduction of OTA's gm.

**Table 5-7 : Residual Offset at the Output of PAMP with reduced gm of OTA**

Residual Offset at the Output of PAMP with reduced gm of OTA	
Sample #	Residual Offset at the output of the preamplifier, with reduced gm of OTA
1	24mV
2	25mV
3	21.5mV
4	25mV

When the offset-control circuit is turned on, different samples give different offsets at the output of PAMP. To test the control-sensitivity of the offset-control circuit, a counter-balancing offset is created by the externally adjustable reference-offset pin ( $V_{REF\_OFST}$ ) to zero the output offsets. Different offsets at the output of PAMP, when the offset-control-circuit is on, imply that there is mismatch within the offset-control-circuit. However, once the offsets are zeroed by external adjustment of the reference-offset, the offset-control sensitivity can be checked. Nominally, the gain of the offset control circuit is -6dB, which means that if an offset of 10mV is dictated externally, 20mV of offset should appear at the output of PAMP. Table 5-8 lists the offsets appearing at the output of different samples when 10mV offset is dictated externally.

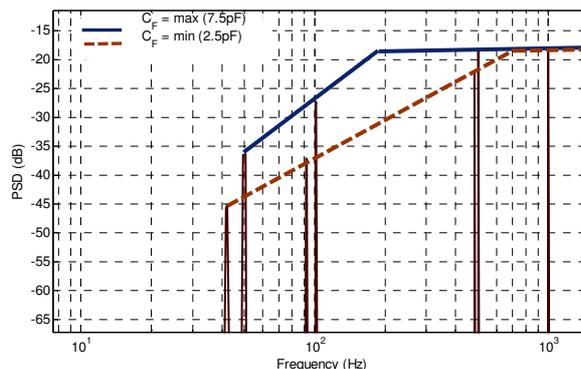
**Table 5-8 : Measured Control-Sensitivity of the Offset-Control-Circuit**

Measured Behavior of the Offset-Control-Circuit		
Sample #	Offset at the output of preamplifier when an input offset of 10mV is dictated by the external reference-offset	Offset-Control-Sensitivity (nominal is 2x)
1	20.6mV	2x
2	29.5mV	3x
3	17.2mV	1.9x
4	30.4mV	3x
5	23.7mV	2.1x

The difference in the offset-control-sensitivity for different samples points to the fact that the dc-gain of the offset-control-circuit is variable for different samples, which implies that there is a mismatch in the input pair and the active load of the OCC. Although the input pair of the offset-control-circuit and the active-load is inter-digitated but they are inter-digitated separately, therefore, they can suffer from significant mismatch, giving rise to variable dc gain. At the same time, samples demonstrated different offsets, which points to device mismatches in the difference-amplifier of the OCC that generates the differential offset-control signal for the main OTA. The devices in this difference amplifier are not inter-digitated and the device sizes are small. Therefore, this difference amplifier can also suffer from significant mismatch.

### 5.5.4 High-Pass Filtering Functionality

Figure 5-28 shows that by controlling the integrating caps, the HPF corner can be adjusted. These results are performed with  $OTA-I_{bias}=20\mu A$ , increasing the  $OTA-I_{bias}$  further shifts the corner to lower-frequencies, lowering the chopping frequency brings about the same effect. The gain of PAMP is kept to 2.5X in both cases. A considerable attenuation factor (~20dB) can be achieved for signals below 100Hz by using the minimum value of feedback capacitors.



**Figure 5-28 : Measured High-Pass Filtering functionality of the PAMP,  $f_{CHOP}=200kHz$**

### 5.5.5 Controllable Gain

Figure 5-29a shows the output swing for a gain of 2.5X and figure 5-29b shows the swing for 5X for an input signal of 20mVpp. These results are performed with OTA biased with 20µA of current.

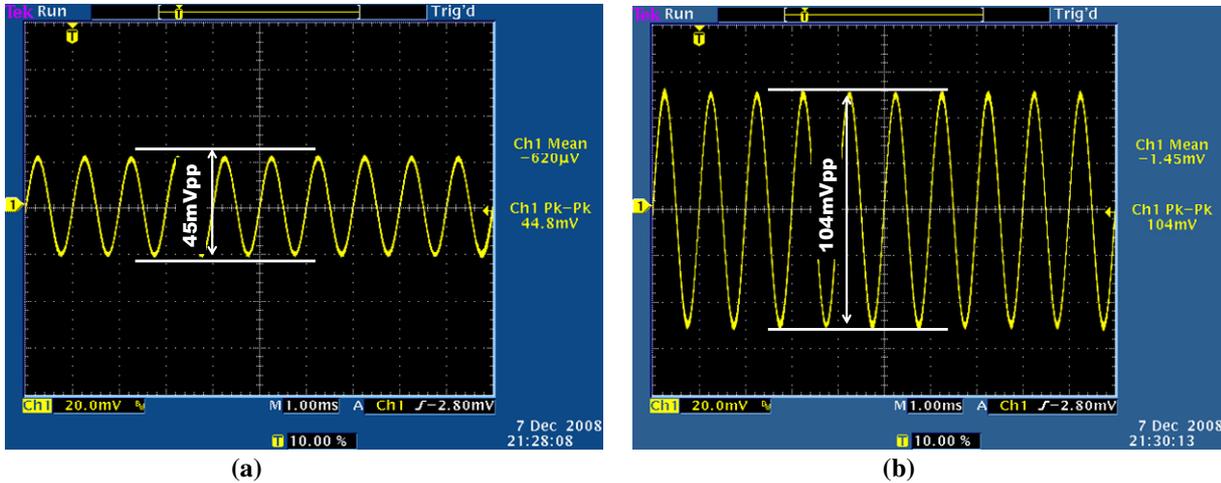


Figure 5-29 : (a) Controllable Gain at the output of the PAMP for an input signal of 20mVpp (equivalent 1Pa), (a) 2.5x and (b) 5x

### 5.5.6 Total Power Consumption of the PAMP

Total Current Consumption, including the global current biases, is 500uA – 510uA (for different samples). However, most of this current goes to the global current biases that are placed inside the chip to scale-down this current to the required level for the PAMP, where the actual PAMP core consumes 50uA-60uA of total current. The current division is shown in table 5-9.

Table 5-9 : Current Distribution inside the Pre-amplifier Core

Current Distribution inside the core	
Current Externally Fed	Expected Scaled down Current
200uA to OTA	20uA
200uA to SF	20uA
100uA to OFST_CONTROL	100nA
Expected Total = 50uA – 60uA @ 1.8V	

## 5.6. Conclusion

This chapter presented the design details and measurement results for a multi-function two-stage chopper-stabilized preamplifier for MCM. The development of this PAMP was an attempt to embed extra-features, such as controllable gain and offset, which would eventually improve a complete integrated readout interface with respect to performance, area and cost. This PAMP also employed chopper-stabilization to mitigate the low-frequency noise and offset, which is not commonly used for MCM PAMPs mainly to avoid the switching-spurs from affecting the MCM linearity. However, the two-stage topology of this PAMP demonstrated that a source-follower based first-stage can be used to shield the MCM from switching spurs while the second-stage employs a chopper-stabilized capacitive gain stage to improve noise performance. The PAMP implemented a digitally controllable high-pass filtering functionality to filter-out low-frequency signal below 100Hz, which could be there because of low-noise wind-hum. The PAMP employed chopper-stabilization in the second-stage to modulate offset and flicker noise out of the audio band and converted the single-ended input from MEMS microphone into a differential output. The second-stage of the PAMP can be used to provide a digitally-controlled gain-factor to adjust the output of PAMP within the desired area of subsequent SDM's DR. This PAMP utilized the miller-effect to achieve a consistent frequency response in the audio band without using a  $G\Omega$  biasing resistor, as was the case in previous interfaces. The  $M\Omega$  resistors were implemented using high-resistance poly-layer, which results in linear and stable resistors as compared to the schemes that are used to implement the  $G\Omega$  resistors. At the same time, using the  $M\Omega$  bias resistors enabled the PAMP to have a controllable high-pass filtering capability. The offset-control feature of the PAMP could be useful to modulate the idle-tones out of the audio-band in subsequent SDM. However, the offset control circuit employed large capacitors ( $\sim 60\text{pF}$ ) and it also suffered from device-mismatches, demonstrating variable offset-control sensitivity in different samples. More efficient approaches could be utilized for offset-control; however, due to limited design and implementation time, the designed offset-control-circuit consumed a relatively larger area and suffered from mismatch errors. This PAMP was implemented in 0.35mm CMOS technology and area with the pads was  $950\mu\text{m} \times 950\mu\text{m}$ , consuming a total current of  $50\mu\text{A}$  at 1.8V of single supply. The PAMP achieved SNDR of 44dBA/Pa.

## Chapter 6

### **Brief discussion on the results, issues faced and conclusions**

This dissertation demonstrated the feasibility of three novel schemes for low-noise, low-power, area and cost –effective readout for MEMS Capacitive Microphones in CMOS technology by presenting their detailed design descriptions and measurement results as application-specific ICs (ASIC) developed to exploit their application scope in consumer electronics and hearing aids. The design issues and implementation methodology for the readout ASICs were discussed and documented in detail to highlight the viability of the presented approaches. The following text summarizes the results achieved throughout this activity to underline its contribution to the state-of-the-art on MCM readout interface.

The first readout interface consisted of a preamplifier, a sigma-delta modulator, integrated biasing and digital control. The preamplifier in this interface employed a modified bootstrapping scheme to achieve a parasitic-insensitive readout, termed as two-terminal bootstrapping. This bootstrapping scheme brought about two important advantages. First, the readout signal was made insensitive to the MCM parasitic capacitors. Second, it relaxed the required gain factor at the input of the subsequent sigma-delta modulator, which reduced power consumption. The dummy-branch scheme that this preamplifier employed to convert the single-ended output of the MCM into a pseudo-differential output was relatively area and power hungry. This interface was bonded with IRST MCM in a single-package and it consumed  $460\mu\text{A}$  of total current for a single supply of 1.8V. The total area of the readout ASIC was  $750\mu\text{m} \times 140\mu\text{m}$ . The electrical measurements of the interface achieved a SNDR of 55dBA/Pa at the output of pre-amplifier and 80dBA of dynamic range at the digital output. The electrical and acoustic results of this interface demonstrated a reasonable resemblance; however, the sensitivity of the integrated system was  $\sim 14\text{dB}$  less than expected most likely due to a reduced sensitivity from the MCM. The measured SNDR for acoustic measurements of the integrated system was 33dBA/Pa and the reduction in SNDR can be ascribed mainly to the reduced sensitivity and higher thermal noise floor shown by the MCM sensor. Furthermore, the package of the integrated acoustic system was not specifically designed for audio-applications and therefore, the frequency response of the integrated system on the higher-frequency side of the audio band was dominated by Helmholtz-resonance, obscuring the true sensitivity of the system [20].

The measurement results achieved through the first interface highlighted that the performance of the complete acoustic system is strongly affected by the characteristics of MCM. Therefore, the second readout interface employed force-feedback, which can be used to enhance the linearity and stability of the MCM and to make it immune to the drift in its mechanical parameters. Force-feedback is not as commonly employed by MCM as by other MEMS capacitive sensors, such as accelerometers. This is due to

the single-ended structure of the MCM sensor. This interface converted the MCM into a pseudo-differential sensor by using a dummy capacitive structure in the ASIC, which was more area and power-efficient than the approach employed in the previous interface; hence, making it compatible with FFB application. This interface consisted of a preamplifier, a sigma-delta modulator and force-feedback logic and it utilized the digital PDM output of the SDM for bias voltage modulation of the MCM as a counterbalancing electrostatic feedback, termed as digital force feedback. Unfortunately, due to the unavailability of MCM sensor, the effect of the force-feedback could not be tested on a MCM. However, the results achieved through behavioral simulations and MCM models can be used to advocate the point that a CMOS compatible force-feedback is highly viable for MCMs. The PAMP in this interface achieved parasitic-insensitive readout through a high-gain OTA in a capacitive feedback configuration. The employed force-feedback logic was relatively area and power-hungry since it used a bank of large poly capacitors ( $\sim 5\text{pF}$  each) and it incurred charging (and discharging) of these capacitors at the rate of modulator clock. This interface was designed in  $0.35\mu\text{m}$  CMOS technology and consumes a total current of  $300\mu\text{A}$  for a single supply of  $3.3\text{V}$ . The total area of the readout ASIC was  $1930\mu\text{m} \times 1630\mu\text{m}$ . It achieved  $40\text{dBA}$  of SNDR at the output of the preamplifier and  $76\text{dBA}$  of DR at the digital output.

The third readout interface focused on the development of a multi-function two-stage chopper-stabilized preamplifier for MCM. The preamplifiers for the first two interfaces implemented a straightforward C-to-V conversion. The reason for keeping the MCM preamplifier simple is to achieve a robust low-noise translation of the MCM capacitive variations with minimal loading of the sensor. However, embedding functionalities in the PAMP such as controllable gain and offset, does eventually improve a complete integrated readout interface with respect to performance, area, cost and flexibility, as demonstrated by this preamplifier. This preamplifier also employed chopper-stabilization to mitigate low-frequency noise and offset, which is not commonly used with MCM preamplifiers mainly to avoid the exposure of the MEMS sensor to the switching spurs. However, the two-stage topology of this preamplifier demonstrated that a source-follower based first-stage can be used to shield the MCM from switching spurs while the second-stage employs a chopper-stabilized digitally-controlled capacitive gain-stage. This preamplifier also implemented a controllable high-pass filtering functionality to filter-out low-frequency noise signals below  $100\text{Hz}$ , which could be there because of low-frequency hum such as wind-hum. This preamplifier converted the single-ended input from MEMS microphone into a fully differential output using a dummy capacitive branch, which was more area efficient than previous approaches. This PAMP utilized miller-effect along with  $\text{M}\Omega$  resistors to achieve a consistent frequency response in the audio band without using  $\text{G}\Omega$  biasing resistors. This scheme not only removed the necessity of having  $\text{G}\Omega$  bias resistances but it also enabled the PAMP to have a high-pass filtering characteristics for signals below  $100\text{Hz}$ . Furthermore, the  $\text{M}\Omega$  resistors were implemented using high-resistance poly-layer, which resulted in more linear and stable resistors as compared to the schemes that are used to implement the  $\text{G}\Omega$  resistors. However, the output noise of the PAMP was dominated by thermal noise of these bias resistors due the particular topology of the PAMP resulting in a high-gain noise-transfer-function. This preamplifier

employed offset control by using an on-chip narrow-band low-pass gm-C filter, which could be useful to modulate the idle-tones in subsequent SDM out of the audio-band. However, this offset control circuit utilized large on-chip capacitors ( $\sim 60\text{pF}$ ) and it also suffered from device-mismatches and demonstrated variable offset-control sensitivity mainly due to the issues in its layout. More area-efficient approaches available in literature could be employed for offset-control; however, this was not evaluated due to limited design and implementation time under this activity. Eventually, it would be more efficient to combine the biasing and the offset-control for the second-stage of the PAMP through a feedback loop, which would ultimately improve the noise and area of the PAMP. This preamplifier was implemented in  $0.35\mu\text{m}$  CMOS technology and the total area was  $950\mu\text{m} \times 950\mu\text{m}$ , consuming a total current of  $50\mu\text{A}$  at  $1.8\text{V}$  of single supply, achieving a SNDR of  $44\text{dBA/Pa}$ .

In order to better evaluate the contribution of this work to the state-of-the-art MCM readout interfaces, it is suitable to paraphrase the R&D nexus this activity was situated in. The related R&D space had not only been vastly open but it also had been instigating an adaptive trend to follow the growing applications of MCM as an evolving sensor. At the same time, the involvement of major industrial players clearly hinted at the scope and practical boundaries for the targeted objectives. This activity was driven by the motivation to assess the feasibility of novel approaches that have not so far been employed for the case of MCM sensors while targeting the state-of-the-art specifications supported by industrial applications. For that matter, this research considers itself to have introduced certain novelties, demonstrated by the above-mentioned results. The adaptation of bootstrapping technique to a two-terminal bootstrapping for a MEMS sensor is demonstrated for the first time in the literature by this activity and it has also received a European patent [95]. The application of digital force-balancing to a single-ended MCM sensor can also be considered as a novel aspect on MCM readout interfaces; however, detailed acoustic characterization of a force-balanced MCM utilizing above-mentioned scheme remains to be part of the future activities. The concept of a multifunction preamplifier for MCM sensor developed during this activity can be definitely considered as a direct contribution to the state-of-the-art MCM readout interfaces as it was developed under industrial supervision from ADI. The other perspective to judge the contribution of this work is to compare the outcomes with the state-of-the-art performance pointers from commercially available readout interfaces for MCM. Therefore, from this perspective, the first integrated digital interface designed during this activity is still comparable to commercial interfaces from the power consumption and area point of view; however, it lags the required performance by almost a factor of  $6\text{dB}$  in the SNDR. The multifunctional preamplifier also meets the power consumption criteria at the same time providing additional functionalities, which are not typically present in commercial preamplifiers; however, it falls behind in the targeted SNDR by a factor of  $14\text{dB}$ . The lag in performance for the above-mentioned systems can be partially attributed to the fact that all of the performance bottlenecks could not be predicted solely from the simulations and were eventually found out in the first prototypes; i.e. the designed readout interfaces in this activity. Certain complications and delays can be attributed to the lack of awareness and resources at particular stages of this activity, which however was part of the student's learning curve. Nev-

ertheless, the degree of novelty together with close proximity of the results with state-of-the-art specification highlight the feasibility of design methodology and schemes presented in this dissertation, which possibly may lead to an optimal system through some design iterations.

Each of the three readout interfaces presents a slightly distinct application perspective within the targeted application domains due to its relative strong and weak points. The first interface is more suited to an integrated solution with digital output and integrated biasing, which can also minimize the impact of sensor parasitics. However, if peculiarities in the under consideration MCM sensor are the main bottleneck in the targeted performance, the force-feedback loop in the second interface is more suitable to improve the linearity of the system. If adding flexibility to the front-end of the interface is the main application goal; to make the system adaptable to different operating conditions, the multifunction preamplifier is the more suitable approach to employ.

Just like any other work, this activity also had its own share of issues, divided among risks and opportunities. One of the major issues during this research activity was the unavailability of relevant specifications on MCM. A parallel ongoing research activity by a fellow PhD student [20] on MCM characterization and modelling did help considerably in behavioural modelling and simulations of the MCM. Nevertheless, the unavailability of the MCM sensor for the readout interface with force-feedback hampered the complete characterization of the interface and digital force-balancing for MCM. The first readout interface was integrated with MCM in single package and acoustic tests were performed on the integrated system. However, the frequency response of the integrated system for the higher frequency-side of the audio band ( $>10\text{kHz}$ ) was dominated by the package resonance obscuring the true sensitivity of the integrated acoustic system, due to the fact that the package was not specifically designed for audio-applications. Another secondary issue was the lack of instrumentation and the experience to make very low noise measurements. With the passage of time during the research activity and exposure attained from different sources, a reasonably adequate measurement setup was eventually achieved in the end of the activity; however, the instrumentation setup still limits some measurements. Especially, for the acoustic testing of the integrated system, a better measurement environment was needed. This activity also involved working with different R&D groups, who were using different design tools customized to their environment. This helped the student to learn about different design tools and to get opinions from experienced designer about the considered approaches. However, on the other hand, due to the limited design time, sometimes it was arduous to fully understand and exploit the tools for the design.

The evidence borrowed from increasing applications of the MCM reveal that there is a vast opportunity of applied research on MCM based acoustic applications. The sensor is gradually improving with respect to sensitivity and mechanical properties. The desire of extra functionalities in a compact low-cost system is always high. The possibility to employ different topologies and technologies in the readout interface is wide-open. The batteries of the system are improving as well, which might redefine the power constraints for the acoustic systems. Therefore, this dynamic scenario is going to change the specifications of the MCM readout interface in the future. The foreseen future directions of the activities on MCM

readout interface, based on the specific experience attained during this research, are briefly sketched in the following paragraphs.

Discrete-time implementation of audio-band sigma-delta modulators has been the favoured approached for quite some time. However, continuous-time sigma-delta modulators have been demonstrating promising results for audio applications with respect to power consumption. The issues with continuous-time sigma-delta modulator such as clock-jitter sensitivity and spread in the loop-filter coefficients should be addressed for their application in MCM applications. Hybrid sigma-delta modulator approaches, which employ both continuous-time and discrete-time loop filters, are also very interesting prospects for MCM readout interface. In these hybrid sigma-delta modulators, the first continuous-time stage can be utilized directly as a preamplifier, utilizing the sensor directly in the noise-shaping loop. Hybrid sigma-delta modulator approaches are more compatible with the application of force-feedback to the MCM. However, the role of MCM parasitics should be evaluated in detail for the hybrid SDMs with respect to their contribution in total power consumption and readout sensitivity. Some adaptability can be embedded in the front-end of the readout electronics, which is typically the part of the backend DSP. The backend digital signal processing is normally more efficient and flexible than the analog front-end signal processing and the future CMOS technologies are optimized for digital design; however, some configurability in the front-end can make the overall system more flexible and efficient. An example of such configurability is to adapt hearing aids or mobile phone for different surrounding environments. Such adaptations can be based on identifying a particular band of signals-of-interest within the audio band to implement source-separation for scenarios such as cocktail party problem. Such adaptability can also be useful for arrays of MCM sensors to partition the audio band in several sub-bands of enhanced sensitivity and subsequently regenerating the complete band through backend post-processing. More effort is needed to evaluate better approaches to devise a multi-function PAMP for the MCM. A controllable band-pass filtering can be useful to favour a particular band of signal all throughout the readout interface, improving in-band SNR and DR. Now that differential MCMs are being pushed for, force-feedback would attract more attention to mitigate the dilemma between sensitivity, stability and linearity of the MCM. A controllable band-pass feedback loop can be used to linearize a particular band of signals without affecting other signals sensitivity. It is also possible to reduce the quantization noise floor using a high-gain in the force-feedback, compensating for the low-gain of MCM transfer function.

The presented results in this dissertation have not only attempted to highlight the feasibility of developing readout interfaces for MCMs in CMOS to achieve a monolithic miniaturized acoustic system, but also to underline the scope that is present for further research in this area. Based on the current indicators and future prospects for MCM sensors, it could be anticipated that MCMs would not only replace ECMs in some of the existing applications but also enter thoroughly new application-paradigms, which implies that the development of their readout interfaces would be an active area of research in the future.

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## Patents

Ungaretti T., Syed Arsalan J., Gottardi M., Baschiroto A., Readout-interface circuit for a capacitive microelectromechanical sensor, and corresponding sensor. European Patent, EP 1 988 366 A1, 2008.